

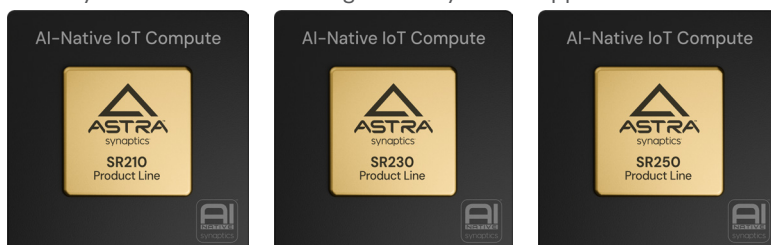


The Synaptics® Astra® SR200 Series introduces the xMCU™, a new class of high-performance, low-power, self-hosted multimodal Edge AI processors with extensible memory for next-generation wearables and battery-powered sensing devices, connected cameras and streamers, and industrial vision and voice systems. Powered by Synaptics Torq™ AI engine featuring the Coral NPU™ from Google Research, the SR200 Series delivers 400 GOPS of AI inference, and high-performance compute with Arm® Cortex®-M85 and Cortex®-M52. The SR200 Series of xMCUs combines heterogeneous, AI-native compute and acceleration with integrated SRAM and extensible custom DRAM scalable to hundreds of MB, enabling larger AI models and richer multimodal workloads to run entirely on-device. Its multi-die system-in-package architecture combines compute, mixed-signal power management, and high-bandwidth memory dies to improve design efficiency and reduce system power and cost.

Multimodal workloads are accelerated using built-in vision, display and audio pipelines. The vision subsystem supports dual MIPI CSI, hardware video codecs, and dual ISPs for human and machine AI vision. An integrated GPU accelerates rich 2D user interfaces with vector and raster rendering, anti-aliasing, transparency, and alpha blending, coupled with a high-performance display pipeline supporting single- and dual-display applications. Multiple I2S/TDM and PDM interfaces, hardware voice-activity detection and a Cadence® Tensilica® HiFi 5 DSP deliver full-stack audio for always-on wake-word listening, event detection, playback, beamforming, and call processing.

A multi-layered security architecture implements hardware isolation, cryptographic acceleration, lifecycle management, and secure boot, and conforms to PSA Level 3 and CC EAL4+ certification targets, providing protection against software and physical attacks.

Industrial product line variants of the SR200 Series feature gigabit Ethernet with IEEE 1588 TSN and dual CAN-FD controllers and deliver multimodal compute and acceleration for robotics and physical AI systems. Built-in serial I/O includes xSPI controllers, USB 2.0, I2C/I3C, SDIO, eMMC, UART and configurable GPIO arrays. Supporting Zephyr RTOS and the open-source Torq NPU compiler, the SR200 Series of xMCUs combines multimodal AI and intelligent sensing with scalable memory to enable advanced Edge and Physical AI applications.



### Benefits

- Run full-stack multimodal applications using integrated custom DRAM and transformer-capable NPU
- Cut down design complexity and system cost with a single-chip MCU solution for audio, display and vision AI
- Build always-on, battery-powered AI experiences leveraging ultra-low power process-node efficiencies and tiered power domains
- Process Industrial and Robotics workloads with serial I/O, GbE and CAN interfaces
- Advance developer freedom via open-source Zephyr RTOS and Torq™ Edge AI compiler



HIGH-PERFORMANCE  
MULTIMODAL AI COMPUTE



AUDIO, VISION & DISPLAY  
INTEGRATION



MULTI-DOMAIN POWER  
ARCHITECTURE



SCALABLE HIGH-BANDWIDTH,  
LOW-POWER CUSTOM DRAM



HARDWARE-ROOTED SECURITY



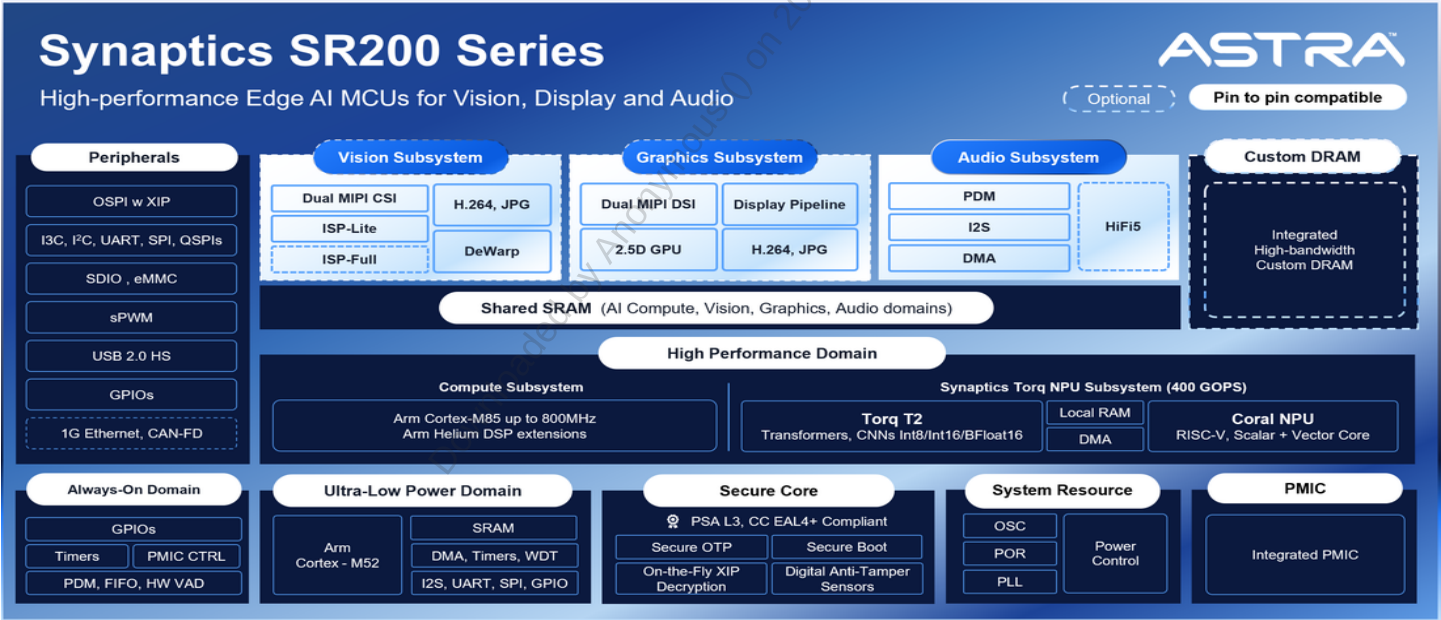
OPEN-SOURCE EDGE AI  
SOFTWARE

Features

- Compute & AI:** Arm® Cortex®-M85 at 800 MHz and Cortex®-M52 at 200 MHz with Arm Helium™ SIMD extensions for DSP/ML workloads
  - Torq AI engine with Coral NPU, supporting INT8, INT16, BFLOAT16 data types
  - Cadence Tensilica HiFi 5 DSP at 400 MHz
- Memory & Storage:** Up to 8 MB of shared SRAM • Hundreds of MB of custom DRAM with secure access • Over 700 KB of combined local memories across processors and DSP • Octal SPI for external NOR/PSRAM devices with XIP • eMMC 5.1 and SD 3.0 interfaces
- Vision & Imaging:** 2x MIPI CSI-2 interfaces with 2 lanes each, up to 2.5 Gbp/s per lane • Dual ISPs for AI vision and human vision • H.264/JPEG encoding
- Graphics & Display:** 2.5D GPU with integrated display pipeline
  - 2x MIPI-DSI interfaces with two data lanes each, 2.5 Gb/s per lane
  - Single 1920×1080 @60 Hz or dual 1920×1080 @30 Hz displays • H.264/JPEG hardware decoding
- Audio:** 2x I2S/TDM + 3x PDM interfaces for up to six digital mics • Always-on domain support • Dedicated hardware voice activity detection and mute pin
- Connectivity & I/O:** 6x UART • 6x I2C, 2x I3C controllers • 6x SPI, 2x QSPI interfaces • 2x SDIO 3.0 controllers • 140+ GPIOs • RISC-V-based I/O engine for custom peripherals • Dual-role USB 2.0 • 2x CAN-FD 2.0A/B controllers • 1x GbE MAC with RMII, RGMII with TSN, IEEE 802.3az
- Security:** PSA Level 3/CC EAL4 architecture • Secure debug • Crypto acceleration
- Power Management:** Integrated mixed-signal PMIC, DVFS • High Performance, Low Power, Ultra-Low Power, Always-On independent power domains

The SR200 Series of xMCUs offers three pin-compatible product lines—the SR210, SR230, and the SR250—supported by a common hardware foundation and an open-source SDK.

| Specification         | Astra SR210                        | Astra SR230                         | Astra SR250                        |
|-----------------------|------------------------------------|-------------------------------------|------------------------------------|
| High-Performance Core | Arm Cortex-M85 @400 MHz, 4 MB SRAM | Arm Cortex-M85 @600 MHz, 5 MB SRAM  | Arm Cortex-M85 @800 MHz, 6 MB SRAM |
| High-Efficiency Core  | Arm Cortex-M52 @100 MHz, 1MB SRAM  | Arm Cortex-M52 @150 MHz, 1.5MB SRAM | Arm Cortex-M52 @200 MHz, 2MB SRAM  |
| NPU                   | 200 GOPS                           | 300 GOPS                            | 400 GOPS                           |
| Package               | FCBGA                              | FCBGA                               | FCBGA                              |
| Grade                 | Consumer, Industrial               | Consumer, Industrial                | Consumer, Industrial               |



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