



Application Note

SL-Series SoC Schematic Design Checklist

Abstract: This application note provides a checklist for SL-Series SoC schematic designs.

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1. Overview

Item	Comment	Checklist
1	GPIO Assignment, PINMUX Mapping, and Level-Shifting	<input checked="" type="checkbox"/>
2	PMIC for Vcore, Vcpu, and Power Rail (Max Current)	<input checked="" type="checkbox"/>
3	Power-Up Sequencing	<input type="checkbox"/>
4	Reset Logic Control	<input type="checkbox"/>
5	Boot & Strap Pin Strapping	<input type="checkbox"/>
6	DDR Memory Configuration	<input checked="" type="checkbox"/>
7	Interfaces	<input type="checkbox"/>

1.1. GPIO Assignment, PINMUX Mapping, and Level-Shifting

1. Ensure GPIO/alternate functions follow SoC-specific Pinmux modes.
2. Select SM_GPIO for controllable GPIO when the system is in standby.
3. GPIO_X[n] is the secondary pin location for GPIO[n]. Only one physical pin can be mapped to GPIO[n] at a time.
4. It is recommended to use GPIO pins configured in Mode 0 for I/O control, as they default to input with high-impedance (Hi-Z) characteristics.
5. Update the GPIO_Pin-Mux table and list the differences from the Astra Machina reference design so that hardware review and software bring-up can be performed.
6. Consider 1.8 V-to-3.3 V level shifting with an external component (3.3 V I/O).

1.2. PMIC for Vcore, Vcpu, and Power Rail (Max Current)

1. Select PMICs from the QVL.
2. Support DVFS (dynamic voltage/frequency scaling).
3. Ensure the third-party PMIC meets the following requirements:

PMIC	Requirement
Max current	> 6 A (SL1680); > 4 A (SL1640/SL1620/SL2610)
Ramp-Up Rate	< 18 mV/us
Fastest slew rate; adjustable	6.25 mV/step or 5 mV/step
Default Voltage	0.8 V
Status	MP status; no EOL planned in the short term

1.3. Power-Up Sequencing

1. The SoC and DDR power-up sequences are listed in the reference design or datasheet.
2. The ramp rate must follow the datasheet.

1.4. Reset Logic Control

1. The SoC includes internal POR (Power-On Reset) logic; keep the POR_EN pin at its default logic-high level.
2. No additional external reset IC is required.

1.5. Boot & Strap Pin Strapping

1. Select the correct pull-up or pull-down resistors for both boot_src[1] and boot_src[0].
2. Reserve a USB-Boot button and an SD-Boot header if needed.
3. Keep the same default values (PU/PD resistors) as in the reference design.

1.6. DDR Memory Configuration

1. Use the reference design topology and termination, including VTT generation.
2. Decouple all power rails appropriately.
3. Verify DQx mapping.
4. Note that while data (DQ) bits within a byte lane can often be swapped to ease routing, clock (CLK) and strobe (DQS) pairs must remain intact and are never swappable.
5. Copying the reference design is recommended; otherwise, the DHL library may also need to be customized.

1.7. Interfaces

1. UART
 - a. Use UART0 as the default console interface. It should be connected to an external UART-to-USB debug board.
 - b. Add a level shifter (1.8 V to 3.3 V) if needed.
2. I2C
 - a. Select SM_TW* for accessible I2C when the system is in standby.
 - b. For I2C (TW1A/TW1B, TW2A/TW2B), only one pair (A or B) should be used at a time for each bus.

- c. Use the correct pull-up resistor on SCL/SDA.
 - d. Add a level shifter (1.8 V to 3.3 V) if needed.
 - e. Ensure devices have different I2C addresses on a single I2C bus.
3. SPI/xSPI
 - a. Keep a 12-pin SPI header with a 2.0 mm pitch for board bring-up if there is no on-board SPI device.
 - b. Select SM_SPI* for accessible SPI when the system is in standby.
 - c. Select a different SPI_SS*n signal for each SPI device.
4. JTAG
 - a. Use test pads instead of a 12-pin header with a 1.27 mm pitch if the header is not needed.
5. eMMC
 - a. External pull-up resistors are not required for CMD and DATA[7:0].
 - b. To prevent voltage fluctuations on the VDDI pin, it is recommended to place 4.7 uF and 0.1 uF decoupling capacitors in parallel.
6. I2S/PDM/MICs
 - a. Ensure the codec/microphone matches the SoC 1.8 V I/O voltage levels.
 - b. Match sample rates and bit depths between SoC and external codec.
 - c. Configure the proper master/slave relationship.
 - d. I2S transmitters and receivers support I2S mode, left-justified mode, right-justified mode, TDM mode, PCM mono mode, and PDM mode.
7. HDMI
 - a. Level shifters are needed on both EDDC and CEC.
 - b. Maximum capacitance between the SDA/SCL/CEC lines and ground must be no greater than 50 pF.
 - c. Use 2.2 kOhm pull-up resistors on the HDMI-Tx side and 47 kOhm pull-up resistors on the HDMI-Rx side for SDA/SCL.
 - d. A 27 kOhm resistor and a diode are needed on the CEC line.
 - e. ESD and common-mode choke components are needed.

8. USB

- a. The USB*_VBUS pin is not 5 V tolerant and must not be connected directly to the 5 V VBUS voltage on the USB port. It must be isolated by an external 30 kOhm resistor so that it sees a lower voltage.
- b. For USB2_ID with OTG support, leave the pin floating for USB device mode or connect it to GND for USB host mode.
- c. ESD and common-mode choke components are needed.

9. SDIO

- a. For a single SDIO interface on SL16x0-series SoCs, only one function is available: either SD card or SDIO Wi-Fi.
- b. Ensure proper voltage compatibility for SD card 1.8 V and 3.3 V signals. SL1620/SL1640/SL2610 devices require an external level shifter and switchable voltage between the SoC and SD card.

10. MIPI_DSI, MIPI_CSI

- a. Ensure correct lane number and lane mapping.
- b. Differential pairs P/N must not be swapped.
- c. Ensure correct logic levels for control signals required by external devices, such as RESET, GPIO, TE, MCLK, and I2C (pull-up resistors).

11. SPDIF

- a. Use a 1.8 V logic level on the SoC side.
- b. Add a level shifter for SPDIF_Optical input/output if needed.
- c. Add external circuitry to meet the SPDIF coaxial electrical specification in IEC 60958-3.

12. FAN

- a. A fan is optional when a heat sink is used.

2. Revision History

Revision	Description
A	Initial release.

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PN: 506-001688-01 Rev A

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