Application Note

SL-Series SoC PCB Design Checklist

Abstract: This application note provides a checklist for SL-Series SoC PCB designs.

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1. Overview

This application note provides a collection of basic layout rules. However, it may not always be possible to follow every rule. The design engineer, using this design guide, must determine which rules can be relaxed, where they can be relaxed, for which signals, and when doing so is necessary.

Item	Comment	Checklist
1	General Requirements	☒
2	PCB Stack-Up and Thickness	☐
3	High-Speed Signal Design (Insertion Loss/Crosstalk and Return Loss)	☐
4	Signal Integrity and Return Path Continuity	☐
5	Strategic Component Placement	☐
6	DDR (Copying the reference design is highly recommended)	☒
7	Power Integrity (Power Plane, Inductance RLC, and IR Drop)	☐

2. General Requirements

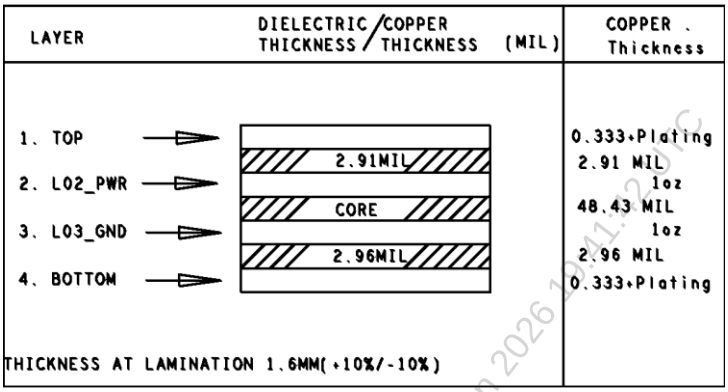
To minimize signal reflections in high-speed designs, ensure impedance matching between the source, transmission line, and sink. Follow all impedance guidelines defined in the *SL-Series High-Speed Interface Design Guide* for compliant layout and routing of high-speed interfaces.

Interface	Impedance Requirement
USB 2.0	90 ohm ±10%
USB 3.0	90 ohm ±10%
eMMC	50 ohm to 60 ohm
RGMII	50 ohm to 60 ohm
GETH	100 ohm ±10%
DDR	Diff: 85 ohm; SE: 50 ohm ±10%; may be 55 ohm ±10% in BGA breakout area
SDIO	50 ohm to 60 ohm
HDMI TX	100 ohm ±10%
HDMI RX	100 ohm ±10%
PCIe0	100 ohm ±10%
PCIe1	100 ohm ±10%
CSI0	100 ohm ±10%
CSI1	100 ohm ±10%
DSI	100 ohm ±10%

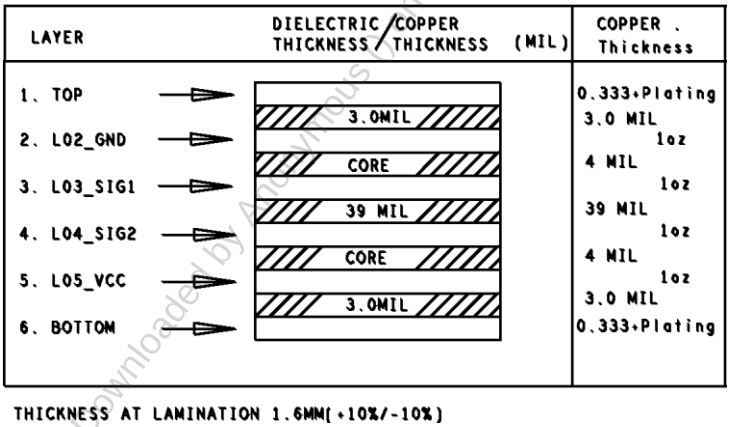
3. PCB Stack-Up and Thickness

The stack-ups presented in the following subsections are intended as reference examples and may serve as a starting point for evaluating and selecting an appropriate PCB stack-up. If a different stack-up is required, recalculate the trace dimensions accordingly. Work closely with your PCB manufacturer to select a stack-up solution that meets the specific electrical and mechanical requirements of your design.

3.1. 4-Layer Stack-Up



3.2. 6-Layer Stack-Up



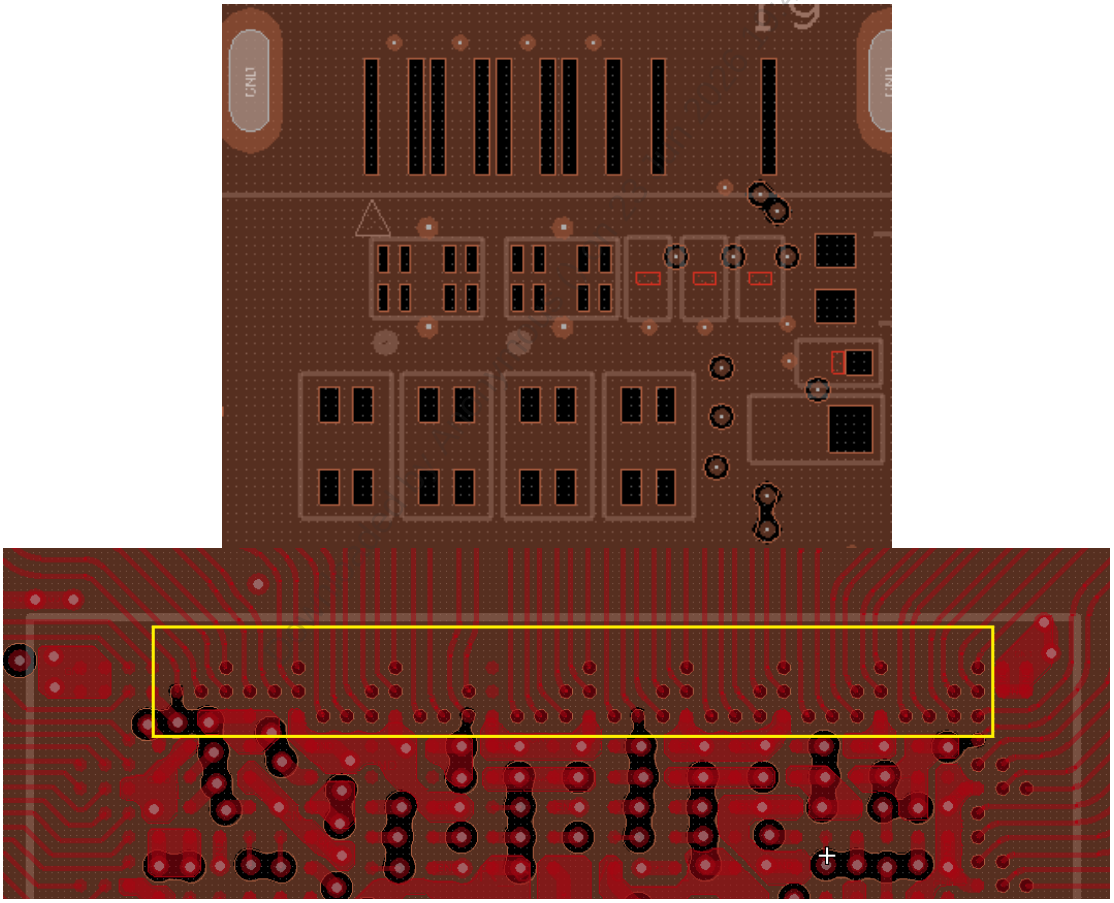
Note: Ensure that the dielectric thickness between Layer 3 (L03) and Layer 4 (L04) is at least 30 mils to minimize crosstalk between high-speed signals.

4. High-Speed Signal Design (Insertion Loss/Crosstalk and Return Loss)

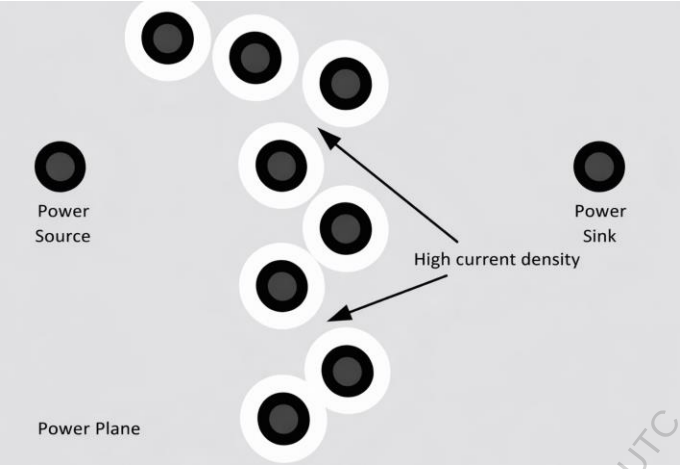
4.1. Reference Plane Guidelines

The impedance of a trace depends on its width and the distance between the trace and its reference plane. A wide trace has lower impedance than a narrow trace at the same distance. The same effect also applies to connector and component pads. A large pad has significantly lower impedance than the trace connected to it. This impedance discontinuity can cause reflections and reduce signal integrity. Therefore, place a plane cutout under large connector and component pads. In this case, use an active reference plane on another layer and stitch it to the normal reference plane with vias.

For high-speed signals such as HDMI, USB 2.0, USB 3.0, PCIe, and DSI/CSI, create a reference-plane cutout directly under series components (e.g., common-mode chokes, series resistors, capacitors, ESD protection components, and connectors).



Note: Avoid power plane hot spots under the SoC area.

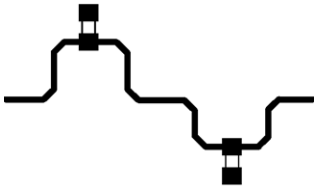


4.2. Differential Pair Routing and Length Matching

Interface	Trace Length Match (p-to-n)	Inter-Pair Match	Notes
USB 2.0	±40 mil	—	—
USB 3.0	±5 mil	—	—
PCIe	±5 mil	—	—
Ethernet	±25 mil	—	—
MIPI DSI/CSI	±10 mil	±50 mil	—
HDMI	±10 mil	±40 mil	—
eMMC / SDIO	—	±50 mil	—

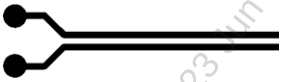
4.2.1. Additional Rules

- The spacing between differential pairs must be at least 3× the dielectric thickness between the signal and its reference layer.
- Avoid creating stubs on high-speed signal traces when adding test pads or resistors. The suggested placement example is shown below. As a rule of thumb, stubs longer than one-tenth of the wavelength should be considered problematic.



- Series resistors, capacitors, and vias in differential pairs should be placed symmetrically.

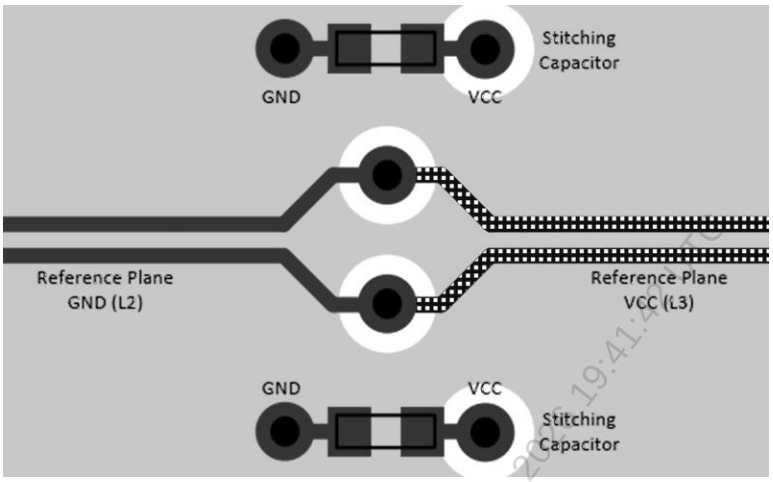
- Maintain a symmetric breakout for all differential-pair signals.



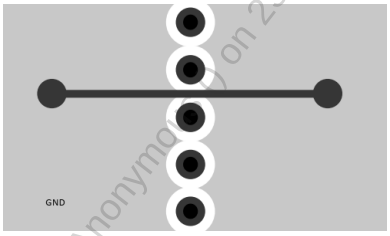
5. Signal Integrity and Return Path Continuity

Review the following:

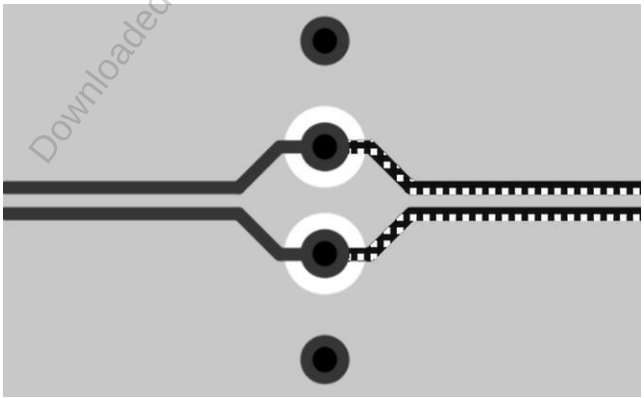
- Always consider the signal return path during layout.
- If a signal crosses between two different reference planes (e.g., GND to VCC), place a stitching capacitor (10 nF to 100 nF) between the planes near the crossover point.



- When vias are placed close together, they may cut off the reference plane; avoid creating voids under high-speed signals.



- Add GND vias whenever a signal trace switches layers. For differential signals, place ground vias symmetrically.



- Maintain an air gap greater than 15 mils between the high-speed signal and the GND shape.

6. Strategic Component Placement

Review the following:

- Place common-mode chokes and ESD protection devices as close as possible to the connectors.
- Use at least eight vias for VCORE and VCPU connections to ensure sufficient current-carrying capacity.
- Remove all dangling traces and vias to prevent floating copper and EMI issues.
- Keep power inductors away from sensitive signal traces.

7. DDR Layout Implementation

Review the following:

- Length matching.
- Differential-Pair Symmetry: Route DQS and CLK as tightly coupled differential pairs, ensuring equal trace lengths and symmetrical via placement to prevent phase skew.
- VTT and VREF Isolation: Route VTT and VREF as shielded traces (isolated by GND), and place VTT termination resistors at the end of the bus. Use a dedicated narrow plane for heat/noise management.

8. Power Integrity (Power Plane, Inductance RLC, and IR Drop)

Review the following:

- Low-Impedance Power Planes: Use wide, solid copper pours (planes) instead of narrow traces for high-current rails (VCORE, VDDM). Ensure that the Power-GND pair is on adjacent layers to maximize planar capacitance.
- IR Drop: Perform DC analysis to ensure that the voltage drop from the PMIC to the SoC load is within ±2% to ±3%. Check for neck-downs (narrow copper areas) near vias that can cause localized heating.
- Via Inductance Reduction: Use multiple stitching vias for power and ground transitions between layers. Use via-in-pad technology for high-speed processors to significantly reduce the inductive loop.

9. Revision History

Revision	Description
A	Initial release.

Contact Us

Visit our website at www.synaptics.com to locate the Synaptics office nearest you.

PN: 506-001689-01 Rev A