

# SRW1500 Series AI-Native MCU with Integrated Wireless Connectivity

AI-Native Connected MCU with 2.4/5/6 GHz Single-Chip IEEE 802.11ax 1x1 MAC, Baseband, and Radio, plus Integrated Bluetooth 6.0 and 802.15.4



## Description

The SRW1500 Series is an advanced AI-native MCU platform purpose-built for intelligent IoT systems that demand real-time inference, low-latency responsiveness, and advanced wireless connectivity. At its core, the SRW1500 Series integrates a high-efficiency Arm® Cortex®-M52 processor with an Arm® Ethos™-U55 NPU, delivering optimized edge AI performance for always-on sensing, contextual awareness, and on-device decision-making. This tightly coupled MCU + AI architecture enables advanced workloads such as voice trigger detection, sound event classification, and AI-enhanced Wi-Fi® sensing for presence and motion detection. Designed for intelligent edge applications, the SRW1500 Series balances compute efficiency, low power consumption, and system cost optimization, while integrating multi-protocol wireless connectivity within a single device. The SRW1500 Series SDK supports FreeRTOS™ and Zephyr® and provides a developer-friendly environment with pre-integrated firmware and middleware for AI-accelerated connectivity stacks.

Downloaded by Anonymous () on 06/11/2025 10:00:00 AM

# Contents

Description.....	1
1. Block Diagram.....	6
1.1. SRW1500 Series .....	7
2. Features .....	8
2.1. Key Features.....	8
2.1.1. MCU subsystem.....	8
2.1.2. Memory.....	8
2.1.3. Security.....	8
2.1.4. Connectivity – Wi-Fi.....	9
2.1.5. Connectivity – Bluetooth .....	9
2.1.6. Peripherals.....	9
2.2. Package Information .....	9
3. Pin Information.....	10
3.1. GPIO Alternative Signal Functions .....	11
3.1.1. SoC Pinmux.....	11
3.1.2. MCU Pinmux .....	15
4. AC and DC Characteristics.....	18
4.1. Absolute Maximum Ratings.....	18
4.2. Environmental Ratings.....	18
4.3. Recommended Operating Conditions and DC Characteristics.....	19
4.4. Two-Wire Serial Interface (TWSI) Timing – I2C Compatible Timing.....	20
4.4.1. TWSI Standard and Fast Mode Timing.....	20
4.4.2. TWSI High Speed – Transfer Rates up to 3.4 Mb/s.....	21
4.5. OSPI (xSPI) Output to Target Input Timing.....	22
4.6. SPI Timing.....	24
4.7. UART Timing.....	27
4.8. I2S Timing.....	27
4.8.1. I2S Host Mode Timing .....	27
4.8.2. I2S Target Mode Timing.....	28
4.9. Timer Counter Smart Pulse-Width Modulator (PWM) Timing .....	29
4.10. USB 2.0 Timing.....	30
4.10.1. USB 2.0 DC Characteristics.....	30
4.11. Pulse Density Modulation Timing Characteristics.....	34
4.12. SDIO v3.0 Interface.....	36
4.12.1. SDIO v3.0 Interface Overview .....	36
4.12.2. SDIO Pins.....	36
4.12.3. SDIO Timing .....	37
4.12.4. SDIO Bus Timing Specifications in SDR Modes .....	38
4.13. JTAG Interface.....	44
4.13.1. JTAG Timing .....	44
5. Power Supplies and Power Management.....	45
5.1. Power Supply Topology.....	45
5.2. Power Topology.....	47
5.3. Power Off Shutdown.....	47
5.4. Power-up, Power-down, and Reset Circuits.....	48
5.5. Internal Regulator Electrical Specifications .....	49
5.5.1. PMU.....	49
5.5.2. Analog Switching Regulator.....	49
5.5.3. CLDO & CHLDO .....	50
5.5.4. BTLDO3P3.....	51
5.5.5. RFLDO3P3 .....	52
5.6. Sequencing of Reset and Regulator Control Signals.....	53

6.	Frequency References .....	55
6.1.	Crystal Interface and Clock Generation.....	55
6.2.	External 32.768 kHz Low-Power Oscillator .....	56
7.	Security .....	57
7.1.	Core Security Features .....	57
8.	MCU Subsystem .....	58
8.1.	M52 Subsystem .....	59
8.2.	NPU .....	60
8.3.	SynaPROT.....	60
8.4.	OTP .....	61
8.5.	Interfaces Summary .....	61
8.6.	Boot Option.....	63
9.	WLAN Global Functions and Interfaces.....	64
9.1.	WLAN CPU and Memory Subsystem.....	64
10.	Bluetooth Subsystem.....	65
10.1.	Overview.....	65
10.2.	Bluetooth Subsystem Summary .....	65
10.3.	Firmware and Patch Support.....	65
11.	Wi-Fi RF Specifications.....	66
11.1.	Wi-Fi Introduction .....	66
11.2.	2.4 GHz Band General RF Specifications.....	67
11.3.	Wi-Fi 2.4 GHz Receiver Performance Specifications.....	67
11.4.	Wi-Fi 2.4 GHz Transmitter Performance Specifications .....	68
11.5.	Wi-Fi 5 GHz/6 GHz Receiver Performance Specifications.....	68
11.6.	Wi-Fi 5 GHz/6 GHz Transmitter Performance Specifications.....	70
12.	Bluetooth RF Specifications .....	71
13.	Package Information .....	74
14.	Package Thermal Characteristics .....	75
14.1.	Junction Temperature Estimation and PsiJT versus ThetaJC .....	75
15.	Ordering and Part Marking Information .....	76
16.	Revision History.....	77

Downloaded by Anonymous (on 2026-10-06 09:17:17 UTC)

## List of Figures

Figure 1. Two-wire serial interface timing.....	21
Figure 2. xSPI Target Data Input Timing.....	23
Figure 3. xSPI CK to CS# Signal Timing.....	24
Figure 4. xSPI DS to CS# Signal Timing.....	24
Figure 5. Motorola SPI Mode 0/2 (SCPH = 0).....	25
Figure 6. Motorola SPI Mode 1/3 (SCPH = 1).....	26
Figure 7. I2S host mode timing.....	28
Figure 8. I2S target mode timing.....	29
Figure 9. PDM Timing - SDR Mode.....	34
Figure 10. PDM timing - DDR Mode.....	35
Figure 11. SDIO bus timing (default mode).....	37
Figure 12. SDIO clock timing (SDR modes).....	38
Figure 13. SDIO bus input timing (SDR modes).....	39
Figure 14. SDIO bus output timing (SDR modes up to 100 MHz).....	39
Figure 15. SDIO bus output timing (SDR modes 100 MHz to 150 MHz).....	40
Figure 16. $\Delta t_{OP}$ consideration for variable data window (SDR 104 mode).....	41
Figure 17. SDIO clock timing (DDR50 mode).....	42
Figure 18. SDIO data timing (DDR50 mode).....	42
Figure 19. Typical power topology: VBAT and VDDIO.....	45
Figure 20. Typical power topology: 1.8 V and 3.3 V.....	46
Figure 21. WLAN = ON, Bluetooth = ON.....	53
Figure 22. WLAN = OFF, Bluetooth = OFF.....	53
Figure 23. WLAN = ON, Bluetooth = OFF.....	53
Figure 24. WLAN = OFF, Bluetooth = ON.....	54
Figure 25. Recommended oscillator configuration.....	55

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## List of Tables

Table 1. SRW1500 Series Features .....	7
Table 2. SoC Pinmux.....	12
Table 3. MCU Pinmux .....	15
Table 4. Absolute maximum ratings .....	18
Table 5. Environmental ratings.....	18
Table 6. Recommended operating conditions and DC characteristics .....	19
Table 7. TWSI Standard and Fast Mode Timing.....	20
Table 8. OSPI (xSPI) Control Output to Target Input Timing .....	22
Table 9. xSPI Relative Timing of the CS#, DS, and CK Signals.....	23
Table 10. SCLK Cycle Time Configurable Range.....	24
Table 11. Motorola SPI Mode 0/2 Timing .....	25
Table 12. Motorola SPI Mode 1/3 Timing.....	26
Table 13. UART Timing .....	27
Table 14. I2S Host Mode Timing.....	27
Table 15. I2S Target Mode Timing.....	28
Table 16. Smart Pulse Width Modulator (PWM) Timing .....	29
Table 17. USB 2.0 DC Electrical .....	30
Table 18. USB High-speed Source Electrical Characteristics.....	32
Table 19. USB Full-speed Source Electrical Characteristics .....	32
Table 20. Pulse Density Modulation (Classic PDM) Timing Parameters – SDR Mode .....	34
Table 21. Pulse Density Modulation (Half Cycle PDM) Timing Parameters – DDR Mode .....	34
Table 22. SDIO pin descriptions .....	36
Table 23. SDIO bus timing1 parameters (default mode) .....	37
Table 24. SDIO bus clock timing parameters (SDR modes).....	38
Table 25. SDIO bus input timing parameters (SDR modes).....	39
Table 26. SDIO bus output timing parameters (SDR modes up to 100 MHz) .....	40
Table 27. SDIO bus output timing parameters (SDR modes 100 MHz to 150 MHz) .....	40
Table 28. SDIO bus clock timing parameters (DDR50 mode) .....	42
Table 29. SDIO bus timing parameters (DDR50 mode) .....	43
Table 30. JTAG timing characteristics .....	44
Table 31. Power-up, power-down, and reset control signals .....	48
Table 32. CHIP_PAD_REG_ON electrical specification .....	48
Table 33. PMU Electrical specification .....	49
Table 34. Analog switching regulator (ASR) electrical specification .....	49
Table 35. CLDO Electrical specification.....	50
Table 36. BTLDO3P3 Electrical specification.....	51
Table 37. RFLDO3P3 electrical specification.....	52
Table 38. Crystal oscillator requirements .....	56
Table 39. External 32.768 kHz sleep clock specifications .....	56
Table 40. Core Security Features .....	57
Table 41. SRW1500 Series MCU Interface Functional and Electrical Summary .....	61
Table 42. Boot option .....	63
Table 43. Bluetooth Subsystem Summary.....	65
Table 44. 2.4 GHz band general RF specifications .....	67
Table 45. Wi-Fi 2.4 GHz Receiver Performance Specifications .....	67
Table 46. Wi-Fi 2.4 GHz Transmitter Performance Specifications.....	68
Table 47. Wi-Fi 5 GHz/6 GHz Receiver Performance Specifications .....	68
Table 48. Wi-Fi 5 GHz/6 GHz transmitter performance specifications .....	70
Table 49. Bluetooth receiver RF specifications .....	71
Table 50. Bluetooth transmitter RF specifications .....	72
Table 51. Local oscillator performance .....	73
Table 52. Package thermal characteristics.....	75





## 1. Block Diagram

The Synaptics SRW1500 Series single-chip device includes an integrated general-purpose MCU with U55 NPU, 2.4/5/6 GHz IEEE802.11 a/b/g/n/ac/ax MAC/baseband/radio and Bluetooth® Low Energy (BLE).



## 1.1. SRW1500 Series

Table 1. SRW1500 Series Features

Product Line	SRW1560		SRW1570	
	SRW1561	SRW1563	SRW1571	SRW1573
Product Family				
Wi-Fi® Technology	Wi-Fi 6	Wi-Fi 6	Wi-Fi 7	Wi-Fi 7
MCU Core	Cortex-M52	Cortex-M52	Cortex-M52	Cortex-M52
Integrated Wireless	Yes	Yes	Yes	Yes
NPU	No	Optional	No	Optional
USB	No	Yes	No	Yes
<b>Grade &amp; Package</b>				
Package	8.6 mm × 10.5 mm 115-lead DR-QFN			
Consumer	Yes (T <sub>A</sub> : 0 °C to +70 °C / T <sub>J</sub> : -40 °C to +85 °C)			

## 2. Features

### 2.1. Key Features

#### 2.1.1. MCU subsystem

- Arm MCU: Cortex-M52
- Arm NPU: Ethos-U55
- SSE-300-based subsystem interconnect
- Anti-fuse OTP: 32 Kb
- Frequency up to 240 MHz
- PSA Level 3 security
- Class B safety compliance
- Power modes to support sleep and low-voltage retention
- Independent ON/OFF of WLAN, BT, and MCU
- Supports 0.8 V/0.9 V standard operating mode

#### 2.1.2. Memory

##### 2.1.2.1. MCU

- SRAM: 1 MB
- Tightly Coupled Memory (TCM): ITCM 128 KB, DTCM 128 KB

#### 2.1.3. Security

- Fully firewalled secure CPU
- Secure boot with ECC digital signature verification
- On-chip 32 Kb anti-fuse OTP
- True random number generator
- Hardware accelerators for AES, RSA, SHA, ECC and HASH
- JTAG® access control through authentication
- Memory and I/O space access control
- Secure Island SynaPROT support
- PSA Certified™ Level 3 RoT component
- Secure access for Arm Cortex®-M52
- Anti-tamper protection
- WLAN/BT subsystems implement isolated secure boot and trust only the Secure Island Processor
- Anti-rollback protection and certificate invalidation mechanisms
- Firmware encryption and AES-accelerated secure boot
- TZC/MPC/PPC-based memory isolation for WLAN/BT subsystems

### 2.1.4. Connectivity – Wi-Fi

- IEEE 802.11ax and 802.11be support
- Supports single spatial stream with PHY rate up to 114.7 Mb/s
- 20 MHz channels and up to 256-QAM support for 2.4 GHz, 5 GHz and 6 GHz bands
- Single 5/6 GHz RF port with on-chip T/R switch, power amplifier (PA) and LNA
- External PA/LNA support for 5/6 GHz band
- Single 2.4 GHz RF port with on-chip T/R switches and BT/Wi-Fi PAs
- Excellent sensitivity is achieved for both BT and Wi-Fi using a shared BT/Wi-Fi receive signal path
- Supports a multi-point external coexistence interface to optimize bandwidth utilization with collocated wireless technologies such as LTE and GPS
- Supports a standard SDIO® v3.0 (4-bit and 1-bit) host interface that is backward compatible with SDIO v2.0
- Full compatibility with IEEE 802.11a/b/g/n/ac legacy protocols with enhanced performance
- Client MU-MIMO support
- Integrated Arm® Cortex®-R4 processor and memory minimizes applications-processor use for standard Wi-Fi functions
- On-chip memory includes 960 KB SRAM and 1408 KB ROM
- This reduces power consumption while maintaining field-upgrade capability

### 2.1.5. Connectivity – Bluetooth

- BT Core Specification Version 6.0
- LE power control
- LE enhanced connection update
- LE channel classification
- Adaptive frequency hopping (AFH)
- Host Controller Interface (HCI) using a high-speed UART interface
- Programmable transmit output power to +20 dBm

### 2.1.6. Peripherals

- USB, UARTs, I<sup>2</sup>C® Host/Target, SPI, PWM, ADC, SDIO, xSPI
- Up to 32 GPIOs

## 2.2. Package Information

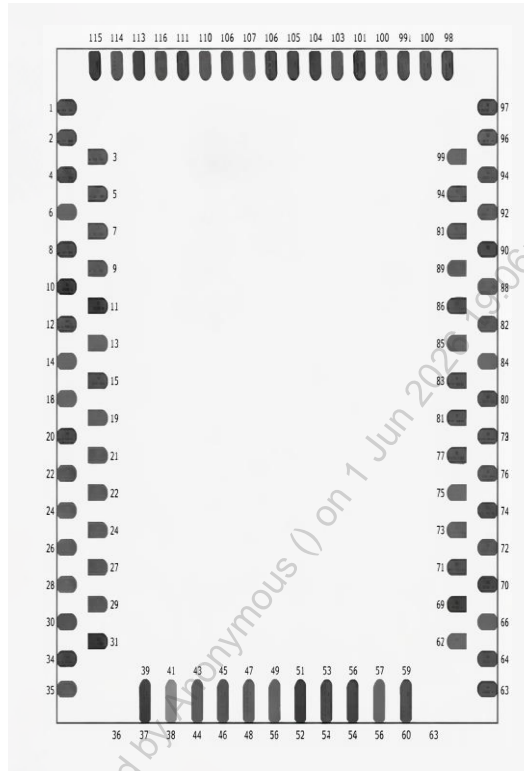
- Package: 8.6 mm × 10.5 mm × 0.9 mm, 115-lead DR-QFN

### 3. Pin Information

115	114	113	112	111	110	109	108	107
WRF_VDD_VIP8_BT	BT_VDD_VIPO2_PLL	BT_VDD_VIPO2	BTLE_RX_IN	BT_VDD_V3P3	WRF_VDD_V3P3_TX2G	WRF_2G_RXTX_INOUT	WRF_VDD_VIPO2_TX2G	WRF_VDD_VIP8

106	105	104	103	102	101	100	99	98
WRF_VDD_VIPO2_TX5G	WRF_5G_RXTX_INOUT	WRF_VDD_V3P3_PA5G	WRF_VDD_V3P3_PAD5G	GP_DAC_OUT	AU_DAC_OUT	GPADC_IN7	GPADC_IN6	GPADC_IN5

1	RF_SW_CTRL_2		
2	RF_SW_CTRL_1		
4	RF_SW_CTRL_3	3	RF_SW_CTRL_0
6	VDDIO	5	RF_SW_CTRL_4
8	RF_SW_CTRL_6	7	RF_SW_CTRL_5
10	GPIO_0	9	RF_SW_CTRL_7
12	VDD_TOP_AON	11	GPIO_1
14	BT_CLDO_VDD	13	BT_CLDO_VDD
18	VDDIO	15	VDD_TOP
20	VDD_TOP_AON	19	CHLDO_VDD
22	BT_I2S_DI	21	BT_HOST_WAKE
24	BT_I2S_DO	22	BT_I2S_DI
26	BT_UART_RXD	24	BT_I2S_DO
28	BT_UART_RTS_N	27	BT_UART_TXD
30	VDDIO	29	BT_UART_CTS_N
34	BT_CLK_REQ	31	MCU_GPIO_12
35	BT_DEV_WAKE		



6		97	GPADC_IN4
		96	AUX_AVDD
99	GPADC_IN6	94	GPADC_IN2
94	GPADC_IN2	92	GPADC_IN1
92	GPADC_IN1	90	WRF_VDD_D_VIPO2_SYNTH_V
89	XTAL_XON	88	XTAL_XOP
86	VDD_ANA_VOP	82	VDDIO
85	VDD_VIPO2_BB	84	VDD_TOP
83	VLDO_VDD	80	SDIO_DATA2
81	SDIO_DATA3	73	VDD_TOP_AON
77	SDIO_CMD	76	SDIO_CLK
75	CHLDO_VDD	74	PA_ON
73	VDD_TOP_AON	72	VDD_TOP
71	VDD_TOP_AON	70	GPIO_2
69	GPIO_3	66	GPIO_5
62	CHIP_PMU_REG_ON	64	GPIO_6
		63	GPIO_7

39	41	43	45	47	49	51	53	56	57	59
USB_VBUS	USB_DP	USB_VCC_A3P3	ASR_VLX	PMU_PVSSA	PMU_VDDIO_P	VDDOUT_SWCORE	PMU_VDDIO	VDDOUT_BT3P3	LDO_VDD_BATS	VDDOUT_RFP3P3

36	37	38	44	46	48	56	52	52	54	56	60	63
PCM_SYNC	PCM_CLK	PCM_OUT	USB_DM	ASR_VRX	PMU_VDDCORE_P	VDDOUT_BT3P3	VDDOUT_SWIP8	VDDOUT_SWIP8	VDDOUT_SWIP2	VDDOUT_BT3P3	VDDOUT_A3P3	GPIO_7

## 3.1. GPIO Alternative Signal Functions

### 3.1.1. SoC Pinmux

Table 2 lists the SoC Pinmux.

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

Table 2. SoC Pinmux

Pin #	Pin Name	30.13.31, 21.20.18, 09.10.24.23	Reset Value of Select (Pinx Mux)	HW Decided/ Power ON Default	Connectivity Dev.	GCI- Mode	Reserve										MCU Use-case (Generic)
	Pin	Straps [Yes/ No]		0			1	2	3	4	5	6	7	8	9	10	
0	GPIO_0	Yes	11	TRISTATE_IND	WL_HOST_WAKE / GPIO_0	GPIO_7	FAST_UART_CTS_IN	GCI_GPIO_0	GCI_GPIO_5	NA	SDIO_SEP_INT_OD	RFFE_SCLK=2	NA	SDIO_SEP_INT	MCU_GPIO_30		
1	GPIO_1	Yes	11	TRISTATE_IND	WL_DEV_WAKE / GPIO_1	GPIO_6	FAST_UART_RTS_OUT	GCI_GPIO_1	GCI_GPIO_6	NA	NA	RFFE_SDATA=2	RF_DISABLE_L	JTAG_N_SW	MCU_GPIO_31		
2	GPIO_2	NA	0	JTAG_SEL_TCK <sup>1</sup>	GPIO_2	GPIO_5	FAST_UART_RX	GCI_GPIO_2	GCI_GPIO_7	UART_DBG_RX	GSIO_SDI	BT_I2S_CLK	TCK	MUXED_RF_SW_CTRL0	MCU_GPIO_22		
3	GPIO_3	NA	0	JTAG_SEL_TMS <sup>2</sup>	GPIO_3	GPIO_4	FAST_UART_TX	GCI_GPIO_3	GCI_GPIO_5	UART_DBG_TX	GSIO_SDO	BT_I2S_WS	TMS	MUXED_RF_SW_CTRL1	MCU_GPIO_23		
4	GPIO_4	NA	0	JTAG_SEL_TDI <sup>3</sup>	GPIO_4	GPIO_3	FAST_UART_CTS_IN	GCI_GPIO_4	GCI_GPIO_6	NA	GSIO_CSN	BT_I2S_DI	TDI	MUXED_RF_SW_CTRL2	MCU_GPIO_24		
5	GPIO_5	NA	0	JTAG_SEL_TDO <sup>4</sup>	GPIO_5	GPIO_2	FAST_UART_RTS_OUT	GCI_GPIO_0	GCI_GPIO_5	NA	GSIO_CLK	BT_I2S_DO	TDO	MUXED_RF_SW_CTRL3	MCU_GPIO_25		
6	GPIO_6	NA	11	TRISTATE_IND	WL_LED1 / GPIO_6	GPIO_1	FAST_UART_RX	GCI_GPIO_1	GCI_GPIO_6	UART_DBG_RX	NA	NA	TRST_L	MUXED_RF_SW_CTRL4	MCU_GPIO_28		
7	GPIO_7	NA	11	TRISTATE_IND	WL_LED0 / GPIO_7	GPIO_0	FAST_UART_TX	GCI_GPIO_2	GCI_GPIO_7	UART_DBG_TX	SDIO_SEP_INT_OD	NA	PMU_TEST_O	SDIO_SEP_INT	MCU_GPIO_29		
8	RF_SW_CTRL_0	NA	11	RF_SW_CTRL_0	RF_SW_CTRL_0	NA	NA	NA	GCI_GPIO_5	NA	GSIO_SDI	NA	NA	NA	MCU_GPIO_26		
9	RF_SW_CTRL_1	NA	0	RF_SW_CTRL_1	RF_SW_CTRL_1	NA	NA	NA	GCI_GPIO_6	NA	GSIO_SDO	NA	NA	NA	MCU_GPIO_27		
10	RF_SW_CTRL_2	NA	0	RF_SW_CTRL_2	RF_SW_CTRL_2	NA	NA	NA	GCI_GPIO_7	NA	GSIO_CSN	NA	NA	NA	MCU_GPIO_26		
11	RF_SW_CTRL_3	NA	11	RF_SW_CTRL_3	RF_SW_CTRL_3	NA	NA	NA	GCI_GPIO_4	NA	GSIO_CLK	NA	NA	NA	MCU_GPIO_27		
12	RF_SW_CTRL_4	NA	0	RF_SW_CTRL_4	RF_SW_CTRL_4 (dLNA)	NA	NA	NA	GCI_GPIO_5	NA	GSIO_CLK	NA	NA	NA	MCU_GPIO_20		
13	RF_SW_CTRL_5	Yes	11	RF_SW_CTRL_5	RF_SW_CTRL_5	NA	NA	NA	GCI_GPIO_5	NA	GSIO_CSN	NA	NA	NA	MCU_GPIO_21		
14	RF_SW_CTRL_6	Yes	11	RF_SW_CTRL_6	RF_SW_CTRL_6	NA	GPIO_0	NA	GCI_GPIO_6	UART_DBG_RX	GSIO_SDO	NA	PALDO_FU	NA	MCU_GPIO_20		
15	RF_SW_CTRL_7	Yes	11	RF_SW_CTRL_7	RF_SW_CTRL_7	NA	GPIO_1	NA	GCI_GPIO_7	UART_DBG_TX	GSIO_SDI	NA	PALDO_PD	NA	MCU_GPIO_13		
16	SDIO_CLK	NA	0	TRISTATE_IND	SDIO_CLK	NA	NA	NA	NA	NA	NA	NA	SDIO_AOS_CLK	NA	MCU_GPIO_14		
17	SDIO_CMD	NA	0	TRISTATE_IND	SDIO_CMD	GPIO_1	NA	NA	GCI_GPIO_0	NA	NA	NA	SDIO_AOS_CMD	NA	MCU_GPIO_15		

<sup>1</sup> TCK (if JTAG enabled, otherwise tri-state)

<sup>2</sup> TMS (if JTAG enabled, otherwise tri-state)

<sup>3</sup> TDI (if JTAG enabled, otherwise tri-state)

<sup>4</sup> TDO (if JTAG enabled, otherwise tri-state)

Pin #	Pin Name	30,13,31 21,20,18, 09,10,24,23	Reset Value of Select (Pinx Mux)	HW Decided/ Power ON Default	Connectivity Dev.	GCI- Mode	Reserve										MCU Use-case (Generic)
	Pin	Straps [Yes/ No]		0	1	2	3	4	5	6	7	8	9	10	11		
18	SDIO_DO	NA	0	TRISTATE_IND	SDIO_DO	GPIO_2	NA	GCI_GPIO_1	NA	NA	NA	NA	SDIO_AOS_DO	NA	MCU_GPIO_16		
19	SDIO_D1	NA	0	TRISTATE_IND	SDIO_D1	GPIO_3	NA	GCI_GPIO_2	NA	NA	NA	NA	SDIO_AOS_D1	NA	MCU_GPIO_17		
20	SDIO_D2	NA	0	TRISTATE_IND	SDIO_D2	GPIO_4	NA	GCI_GPIO_3	NA	NA	NA	NA	SDIO_AOS_D2	NA	MCU_GPIO_18		
21	SDIO_D3	NA	0	TRISTATE_IND	SDIO_D3	GPIO_5	NA	GCI_GPIO_4	NA	NA	NA	NA	SDIO_AOS_D3	NA	MCU_GPIO_19		
22	BT_HOST_WAKE	NA	11	BT_HOST_WAKE	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_0		
23	BT_CLK_REQ	Yes	11	BT_CLK_REQ	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_9		
24	BT_DEV_WAKE	No	11	BT_DEV_WAKE	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_10		
25	BT_I2S_DI	Yes	11	BT_I2S_DI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_1		
26	BT_I2S_WS	Yes	11	BT_I2S_WS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_2		
27	BT_I2S_DO	Yes	11	BT_I2S_DO	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_3		
28	BT_I2S_CLK	Yes	11	BT_I2S_CLK	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_4		
29	BT_UART_RXD	NA	0	BT_UART_RXD	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_5		
30	BT_UART_TXD	NA	0	BT_UART_TXD	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_6		
31	BT_UART_RTS_N	NA	0	BT_UART_RTS_N	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_7		
32	BT_UART_CTS_N	NA	0	BT_UART_CTS_N	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_8		
44	MCU_GPIO_11	NA	0	TRISTATE_IND	MCU_GPIO_11	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_2		
45	MCU_GPIO_12	NA	0	TRISTATE_IND	MCU_GPIO_12	NA	NA	NA	NA	NA	NA	NA	NA	NA	MCU_GPIO_1		
Dedicated Functional Pins (no part of pin muxing)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
47	JTAG_SEL	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
48	XTAL_XOP	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
49	XTAL_XON	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
50	LPO_IN	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
51	USB+	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
52	USB-	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
53	USB_HS_VBUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
54	USB_HS_ID	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
55	Audio DAC	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
56	GP DAC	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		

Pin #	Pin Name	30,13,31, 21,20,18, 09,10,24,23	Reset Value of Select (Pinx Mux)	HW Decided/ Power ON Default	Connectivity Dev.			Reserve							MCU Use-case (Generic)
	Pin	Straps [Yes/ No]		0	1	2	3	4	5	6	7	8	9	10	11
57	GPADC_IN0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
58	GPADC_IN1	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
59	GPADC_IN2	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
60	GPADC_IN3	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
61	GPADC_IN4	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
62	GPADC_IN5	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
63	GPADC_IN6	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
64	GPADC_IN7	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
65	BTLE_RXTX_INOUT	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
66	WRF_2G_RXTX_INOUT	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
67	WRF_5G_RXTX_INOUT	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
68	WRF_GP AIO_OUTP	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
69	WRF_GP AIO_OUTN	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
70	PMU_GPIAO	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
NA	Package Option (not QFN pin)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
71	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
72	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
73	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
NA	Strap (Connectivity DVT vs. MCU)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
NA	Strap (DAP)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

**Note:** The above defines the status for all SRW1500 Series GPIOs based on the tri-state test mode.

### 3.1.2. MCU Pinmux

Table 3. MCU Pinmux

Pin Name	PAD Type	IO state@ cold boot	Package Pin	MODE_0	MODE_1	MODE_2	MODE_3	MODE_4	MODE_5	MODE_6	MODE_7	STRAP	WAKE UP source	Special Function	SoC pin function (informative)	
MCU_GPIO00	XSPI Data Strobe	IN	35	IO:XSPI_DQS	IO:GPIO00	NA	NA	NA	NA	NA	NA	NA	NA	NA	BT_HOST_WAKE	NA
MCU_GPIO01	XSPI Data 0	IN	22	IO:XSPI_DATA0	IO:GPIO01	NA	NA	NA	NA	NA	NA	STRAP3	NA	NA	BT_I2S_DI	NA
MCU_GPIO02	XSPI Data 1	IN	23	IO:XSPI_DATA1	IO:GPIO02	NA	NA	NA	NA	NA	NA	STRAP4	NA	NA	BT_I2S_WS	NA
MCU_GPIO03	XSPI Data 2	IN	24	IO:XSPI_DATA2	IO:GPIO03	NA	NA	NA	NA	NA	NA	STRAP8	NA	NA	BT_I2S_DO	NA
MCU_GPIO04	XSPI Data 3	IN	25	IO:XSPI_DATA3	IO:GPIO04	NA	NA	NA	NA	NA	NA	STRAP9	NA	NA	BT_I2S_CLK	NA
MCU_GPIO05	XSPI Data 4	IN	26	IO:XSPI_DATA4	IO:GPIO05	UART0_TX	NA	NA	NA	NA	NA	NA	NA	NA	BT_UART_RXD	NA
MCU_GPIO06	XSPI Data 5	IN	27	IO:XSPI_DATA5	IO:GPIO06	UART0_RX	NA	NA	NA	NA	NA	NA	WAKE3	NA	BT_UART_TXD	NA
MCU_GPIO07	XSPI Data 6	IN	28	IO:XSPI_DATA6	IO:GPIO07	UART0_RTS	NA	NA	NA	NA	NA	NA	NA	NA	BT_UART_RTS_N	NA
MCU_GPIO08	XSPI Data 7	IN	29	IO:XSPI_DATA7	IO:GPIO08	UART0_CTS	NA	NA	NA	NA	NA	NA	NA	NA	BT_UART_CTS_N	NA
MCU_GPIO09	XSPI CSNO	IN	34	O:XSPI_CS0	IO:GPIO09	NA	NA	NA	NA	NA	NA	STRAP5	NA	NA	BT_CLK_REQ	NA
MCU_GPIO10	XSPI CSN1	IN	35	O:XSPI_CS1	IO:GPIO10	NA	NA	NA	NA	NA	NA	NA	WAKE4	NA	BT_DEV_WAKE	NA
MCU_GPIO11	XSPI clock	IN	32	O:XSPI_CLK	IO:GPIO11	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
MCU_GPIO12	XSPI Clock - ve	IN	31	O:XSPI_CLKN	IO:GPIO12	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
MCU_GPIO13	NA	IN	9	IO:GPIO13	NA	NA	I:PDM_MUTE	O:PWM5	I:CAP2	IO:I2S_WS	NA	STRAP6	NA	NA	RF_SW_CTRL_7	NA
MCU_GPIO14	NA	IN	76	IO:GPIO14	I:SDO_CLK	O:UART1_TX	NA	IO:I2C_SLV_SDA	O:SPLV_MISO	I:UART0_CTS	NA	NA	NA	NA	SDIO_CLK	NA
MCU_GPIO15	NA	IN	77	IO:GPIO15	IO:SDO_CMD	I:UART1_CTS	I:DMQ_DATA	NA	I:SPLV_MOSI	O:UART0_TX	NA	NA	NA	NA	SDIO_CMD	NA
MCU_GPIO16	NA	IN	78	IO:GPIO16	IO:SDO_DO	O:UART1_RTS	IO:DMO_CLK	NA	I:SPLV_CLK	I:UART0_RX	NA	NA	NA	NA	SDIO_DO	NA
MCU_GPIO17	NA	IN	79	IO:GPIO17	IO:SDO_D1	I:UART1_RX	NA	IO:I2C_SLV_SCL	I:SPLV_CS	O:UART0_RTS	NA	NA	WAKE0	NA	SDIO_D1	NA
MCU_GPIO18	NA	IN	80	IO:GPIO18	IO:SDO_D2	NA	O:UART2_TX	NA	I:CAP0	O:I2S_SDO	NA	NA	NA	NA	SDIO_D2	NA
MCU_GPIO19	NA	IN	81	IO:GPIO19	IO:SDO_D3	NA	I:UART2_RX	NA	I:CAP1	NA	NA	NA	NA	NA	SDIO_D3	NA
MCU_GPIO20	NA	IN	5 & 8	IO:GPIO20	I:DMQ_DATA	IO:I2C_MST_SDA	O:UART0_TX	NA	I:CAP2	NA	NA	STRAP7	NA	NA	RF_SW_CTRL_4 & 6	NA
MCU_GPIO21	NA	IN	7	IO:GPIO21	IO:DMO_CLK	IO:I2C_MST_SCL	I:UART0_RX	NA	NA	NA	NA	STRAP0	NA	NA	RF_SW_CTRL_5	NA
MCU_GPIO22	NA	IN	70	IO:GPIO22	O:SPL_MSTR_MOSI	O:UART0_RTS	O:UART1_TX	IO:I2C_MST_SCL	NA	I:I2S_SD	NA	NA	NA	NA	GPIO_2	I:TCK (JTAG-A)
MCU_GPIO23	NA	IN	69	IO:GPIO23	O:SPL_MSTR_CLK	O:UART0_TX	O:UART1_RTS	O:PWMO	NA	IO:I2S_SCLK	NA	NA	NA	NA	GPIO_3	I:TMS (JTAG-A)

Pin Name	PAD Type	IO state@ cold boot	Package Pin	MODE_0	MODE_1	MODE_2	MODE_3	MODE_4	MODE_5	MODE_6	MODE_7	STRAP	WAKE UP source	Special Function	SoC pin function (informative)	
MCU_GPIO24	NA	IN	67	IO:GPIO24	O:SPL_MSTR_CS	I:UART0_RX	I:UART1_CTS	O:PWM1	NA	IO:I2S_WS	NA	NA	NA	NA	GPIO_4	I:TDI (JTAG-A)
MCU_GPIO25	NA	IN	66	IO:GPIO25	I:SPL_MSTR_MISO	I:UART0_CTS	I:UART1_RX	IO:I2C_MST_SDA	O:PWM4	I:PDM_MUTE	NA	NA	WAKE1	NA	GPIO_5	O:TDO (JTAG-A)
MCU_GPIO26	NA	IN	3 & 1	IO:GPIO26	O:PWMO	NA	IO:I2C_MST_SDA	IO:I2C_SLV_SDA	NA	NA	NA	NA	NA	NA	RF_SW_CTRL_0 & 2	NA
MCU_GPIO27	NA	IN	2 & 4	IO:GPIO27	O:PWM1	NA	IO:I2C_MST_SCL	IO:I2C_SLV_SCL	NA	I:PDM_MUTE	NA	NA	NA	NA	RF_SW_CTRL_1 & 3	NA
MCU_GPIO28	NA	IN	64	IO:GPIO28	IO:I2C_MST_SDA	IO:I2C_SLV_SDA	NA	NA	O:UART2_TX	NA	NA	NA	NA	NA	GPIO_6	I:TRST_L (JTAG-A)
MCU_GPIO29	NA	IN	63	IO:GPIO29	IO:I2C_MST_SCL	IO:I2C_SLV_SCL	NA	NA	I:UART2_RX	NA	NA	NA	NA	NA	GPIO_7	NA
MCU_GPIO30	NA	IN	10	IO:GPIO30	I:CAP2	O:SPL_MSTR_CS1	O:PWM2	I:DMO_DATA	O:UART2_RTS	I:I2S_SD	NA	STRAP2	WAKE2	NA	GPIO_0	NA
MCU_GPIO31	NA	IN	11	IO:GPIO31	NA	O:SPL_MSTR_CS2	O:PWM3	IO:DMO_CLK	I:UART2_CTS	IO:I2S_SCLK	NA	STRAP1	NA	NA	GPIO_1	NA
GPADC_IN0	NA	IN	91	GPADC_IN0	O:UART1_RTS	I:TCK (JTAG-B)	O:PWMO	O:UART2_TX	NA	IO:GPIO01	O:DBG_OUT0	NA	NA	NA	NA	I:TCK (JTAG-B)
GPADC_IN1	NA	IN	92	GPADC_IN1	I:UART1_CTS	I:TMS (JTAG-B)	O:PWM1	I:UART2_RX	NA	IO:GPIO02	O:DBG_OUT1	NA	NA	NA	NA	I:TMS (JTAG-B)
GPADC_IN2	NA	IN	94	GPADC_IN2	O:UART1_TX	I:TDI (JTAG-B)	O:PWM2	IO:I2C_SLV_SDA	IO:GPIO14	IO:GPIO03	O:DBG_OUT2	NA	NA	NA	NA	I:TDI (JTAG-B)
GPADC_IN3	NA	IN	93	GPADC_IN3	I:UART1_RX	O:TDO (JTAG-B)	O:PWM3	IO:I2C_SLV_SCL	IO:GPIO15	IO:GPIO04	O:DBG_OUT3	NA	NA	NA	NA	O:TDO (JTAG-B)
GPADC_IN4	NA	IN	97	GPADC_IN4	O:UART1_TX	I:TRST_L (JTAG-B)	O:PWM4	O:I2S_SDO	IO:GPIO16	IO:GPIO05	O:DBG_OUT4	NA	NA	NA	NA	I:TRST_L (JTAG-B)
GPADC_IN5	NA	IN	98	GPADC_IN5	O:UART1_RTS	O:SPL_MSTR_CS3	O:PWM5	I:PDM_MUTE	IO:GPIO17	IO:GPIO06	O:DBG_OUT5	NA	NA	NA	NA	NA
GPADC_IN6	NA	IN	99	GPADC_IN6	I:UART0_RX	NA	I:CAP0	NA	IO:GPIO18	IO:GPIO07	O:DBG_OUT6	NA	NA	WL_ON	NA	NA
GPADC_IN7	NA	IN	100	GPADC_IN7	I:UART0_CTS	NA	I:CAP1	NA	IO:GPIO19	IO:GPIO08	O:DBG_OUT7	NA	NA	BT_ON	NA	NA
AU_DAC_OUT	NA	NA	101	AU_DAC_OUT	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
GP_DAC_OUT	NA	NA	102	GP_DAC_OUT	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
USB_HS_VSSA	Analog VSS	NA	37	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
USB_HS_DN	Data N	NA	42	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
USB_HS_DP	Data P	NA	41	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
USB_HS_VCCCORE	Digital Core VDD (0.8)	NA	38	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
USB_HS_VBUS	VBUS for sensing only	NA	39	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
USB_HS_ID	ID Pin	NA	36	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

Pin Name	PAD Type	IO state@ cold boot	Package Pin	MODE_0	MODE_1	MODE_2	MODE_3	MODE_4	MODE_5	MODE_6	MODE_7	STRAP	WAKE UP source	Special Function	SoC pin function (informative)	
USB_HS_VCCA33	Analog VDD (3.3v)	NA	43	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
USB_HS_VCC18	NA	NA	40	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 4. AC and DC Characteristics

**Note:** Values in this datasheet are design goals and are subject to change based on the results of device characterization.

### 4.1. Absolute Maximum Ratings

**Caution:** The absolute maximum ratings in the table below indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 4. Absolute maximum ratings

Rating	Symbol	Value	Unit
DC supply for VBAT	VBAT	-0.5 to +5.25	V
DC supply voltage for	VDDIO	-0.5 to 1.98	V
DC supply voltage for RF	VDDIO_RF	-0.5 to 1.98	V
DC supply voltage for RF	—	-0.5 to 1.15	V
DC supply voltage for	—	-0.5 to 0.99	V
Maximum undershoot	$V_{undershoot}$	-0.5	V
Maximum overshoot	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction	$T_j$	125	°C

1. Duration not to exceed 25% of the duty cycle.

### 4.2. Environmental Ratings

Table 5. Environmental ratings

Characteristic	Value	Unit	Conditions
Ambient Temperature ( $T_A$ )	-30 to +85	°C	Functional operation <sup>1</sup>
Storage Temperature	-40 to +125	°C	—
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

1. Functionality is guaranteed across this temperature range. Optimal RF performance specified in the datasheet, however, is guaranteed only for -10 °C to +55 °C without derating performance.

### 4.3. Recommended Operating Conditions and DC Characteristics

**Caution:** Functional operation is not guaranteed outside of the limits shown in Table 4. Absolute maximum ratings, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 6. Recommended operating conditions and DC characteristics

Parameter	Value				
	Symbol	Minimum	Typical	Maximum	Unit
DC supply voltage for VBAT	VBAT	3.0 <sup>1</sup>	—	5.0	V
DC supply voltage for core	VDD	0.72	0.8	0.99	V
DC supply voltage for RF blocks in	VDDRF	0.85	0.9	0.95	V
DC supply voltage for digital I/O	VDDIO	1.71	1.8	1.89	V
DC supply voltage for analog I/O	VDDIOA, VDDIOP PMU_VDDIOA	1.71	1.8	1.89	V
DC supply voltage for RF switch I/Os	—	1.71	1.8	1.89	V
Internal POR threshold	Vth_POR	0.4	—	0.7	V
<b>Other Digital I/O Pins</b>					
For VDDIO = 1.8 V:					
Input high voltage	VIH	$0.65 \times VDDIO$	—	—	V
Input low voltage	VIL	—	—	$0.4 \times VDDIO$	V
Output high voltage @ 2 mA	VOH	$VDDIO - 0.40$	—	—	V
Output low voltage @ 2 mA	VOL	—	—	0.40	V
For VDDIO_RF = 1.8 V:					
Output high voltage @ 2 mA	VOH	$VDDIO\_RF - 0.40$	—	—	V
Output low voltage @ 2 mA	VOL	—	—	0.40	V

1. The SRW1500 Series is functional across this range of voltages. Optimal RF performance specified in the datasheet, however, is guaranteed only for  $3.2\text{ V} < VBAT < 4.8\text{ V}$ .

## 4.4. Two-Wire Serial Interface (TWSI) Timing – I2C Compatible Timing

### 4.4.1. TWSI Standard and Fast Mode Timing

Applies across the full range of values listed in Table 6 unless otherwise specified.

Table 7. TWSI Standard and Fast Mode Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F <sub>TWSI_SCL</sub>	SCL Clock Frequency	100 kHz	—	—	100	kHz
		400 kHz	—	—	400	
T <sub>TWSI_NS</sub>	Noise Suppression Time at SCL, SDA Inputs	100 kHz	—	—	80	ns
		400 kHz	—	—	80	
T <sub>TWSI_R</sub>	SCL, SDA Rise time	100 kHz	—	—	1000	
		400 kHz	—	—	300	
T <sub>TWSI_F</sub>	SCL, SDA Fall Time	100 kHz	—	—	300	
		400 kHz	—	—	300	
T <sub>TWSI_HIGH</sub>	Clock High Period	100 kHz	4000	—	—	
		400 kHz	600	—	—	
T <sub>TWSI_LOW</sub>	Clock Low Period	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
T <sub>TWSI_SU:STA</sub>	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700	—	—	
		400 kHz	600	—	—	
T <sub>TWSI_HD:STA</sub>	Start Condition Hold Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
T <sub>TWSI_SU:STO</sub>	Stop Condition Setup Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
T <sub>TWSI_SU:DAT</sub>	Data in Setup Time	100 kHz	250	—	—	
		400 kHz	100	—	—	
T <sub>TWSI_HD:DAT</sub>	Data in Hold Time	100 kHz	300	—	—	
		400 kHz	300	—	—	
T <sub>TWSI_BUF</sub>	Bus Free Time	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
T <sub>TWSI_DLY</sub>	SCL Low to SDA Data Out Valid	100 kHz	40	—	200	
		400 kHz	40	—	200	

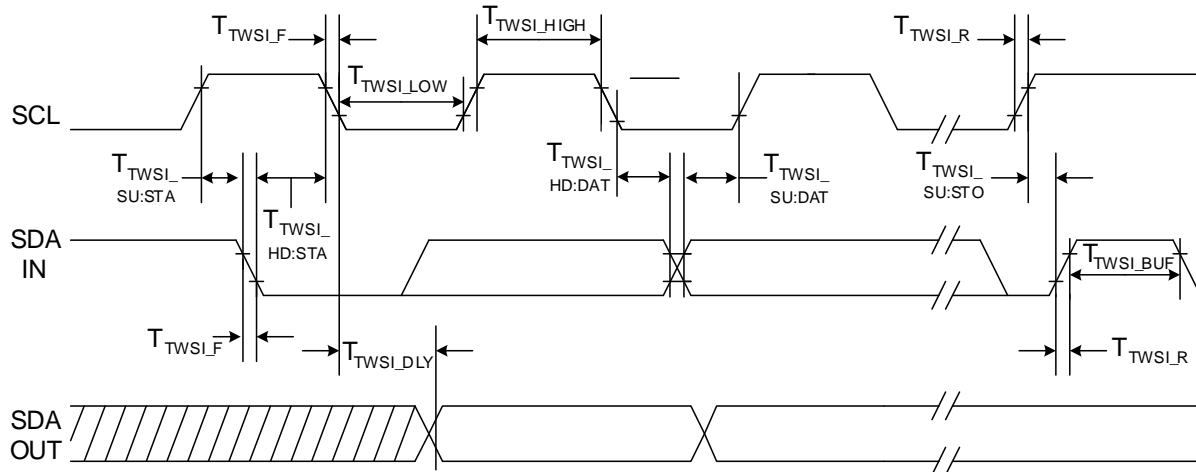


Figure 1. Two-wire serial interface timing

#### 4.4.2. TWSI High Speed – Transfer Rates up to 3.4 Mb/s

For timing information, refer to the I<sup>2</sup>C Bus Specification.

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 4.5. OSPI (xSPI) Output to Target Input Timing

Additional timing specifications are defined in JEDEC JESD251C (xSPI) standard, which references the JEDEC JESD84–B51 HS400 mode for electrical characteristics.

Table 8. OSPI (xSPI) Control Output to Target Input Timing

Parameter	Symbol	xSPI400		xSPI333		xSPI266		xSPI200		Unit	Comments
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
<b>Input CK</b>											
Cycle Time Data Transfer Mode	$t_{PERIOD}$	5	—	6	—	7.5	—	10	—	ns	200 MHz (max) between the rising edges with respect to VT.
Slew Rate	SR	1.125	—	0.94	—	0.75	—	0.56	—	V/ns	With respect to $V_{IH}/V_{IL}$ .
Duty Cycle Distortion	$t_{CKDCD}$	0.0	0.25	0.0	0.3	0.0	0.375	0.0	0.5	ns	Allowable deviation from an ideal 50% duty cycle with respect to VT. Includes jitter and phase noise.
Minimum Pulse Width	$t_{CKMPW}$	2.25	—	2.7	—	3.375	—	4.5	—	ns	With respect to $V_T$ .
<b>Input Signals (Referenced to CK)</b>											
Input Setup Time	$t_{ISUddr}$	0.5	—	0.6	—	0.8	—	1.0	—	ns	With respect to $V_{IH}/V_{IL}$ .
Input Hold Time	$t_{IHddr}$	0.5	—	0.6	—	0.8	—	1.0	—	ns	With respect to $V_{IH}/V_{IL}$ .
Slew Rate @ 1.2 V	SR	0.75	—	0.62	—	0.50	—	0.38	—	V/ns	With respect to $V_{IH}/V_{IL}$ and xSPI reference load.
Slew Rate @ 1.8 V	SR	1.125	—	0.94	—	0.75	—	0.56	—	V/ns	With respect to $V_{IH}/V_{IL}$ and xSPI reference load.

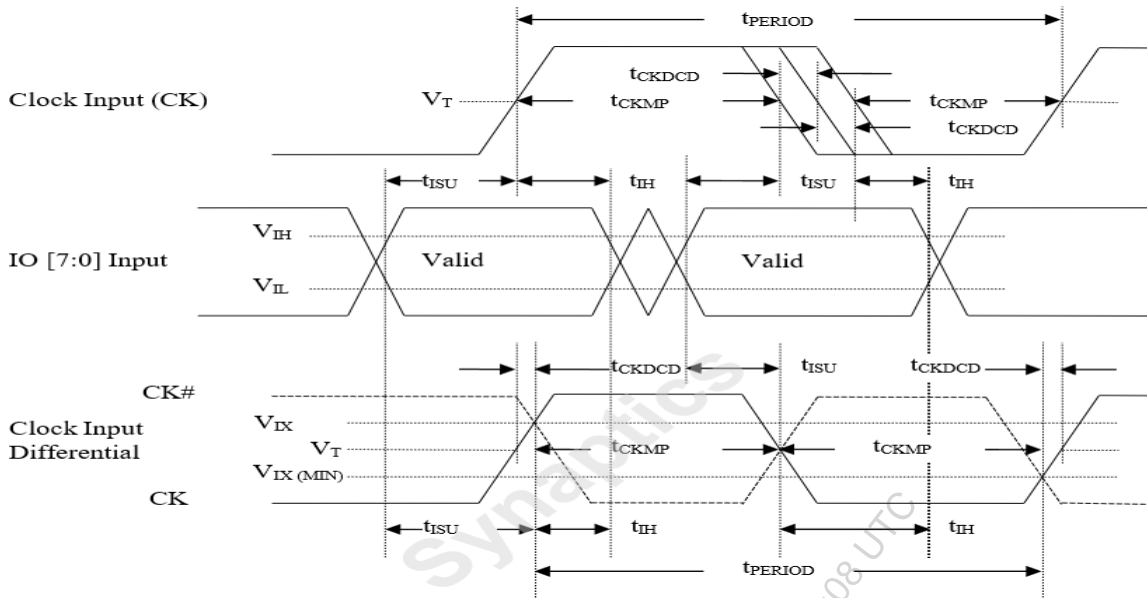


Figure 2. xSPI Target Data Input Timing

Table 9. xSPI Relative Timing of the CS#, DS, and CK Signals

Parameter	Symbol	xSPI400		xSPI333		xSPI266		xSPI200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock LOW to CS LOW	tCKLCSL	4	—	4.8	—	6	—	8	—	ns
CS LOW to Clock HIGH	tCSLCKH	4	—	4.8	—	6	—	8	—	ns
Clock LOW to CS HIGH	tCKLCSH	4	—	4.8	—	6	—	8	—	ns
CS HIGH to Clock HIGH	tCSHCKH	4	—	4.8	—	6	—	8	—	ns
DS LOW to CS HIGH	tDSLCSH	80% of tPERIOD	—	80% of tPERIOD	—	80% of tPERIOD	—	80% of tPERIOD	—	—
CS HIGH to DS Tri-State	tCSHDST	0	tPERIOD	0	tPERIOD	0	tPERIOD	0	tPERIOD	ns
CS LOW to DS LOW	tCSLDSL	0	—	0	—	0	—	0	—	ns
DS Tri-State to CS LOW	tDSTCSL	0	—	0	—	0	—	0	—	ns

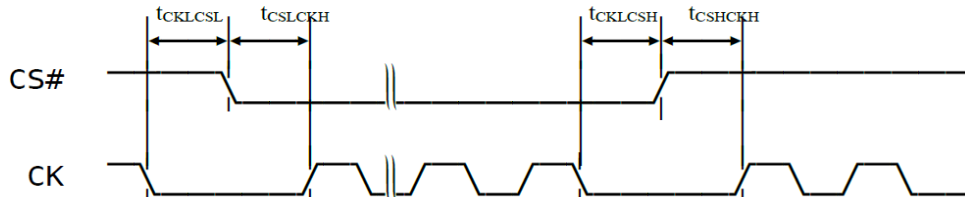


Figure 3. xSPI CK to CS# Signal Timing

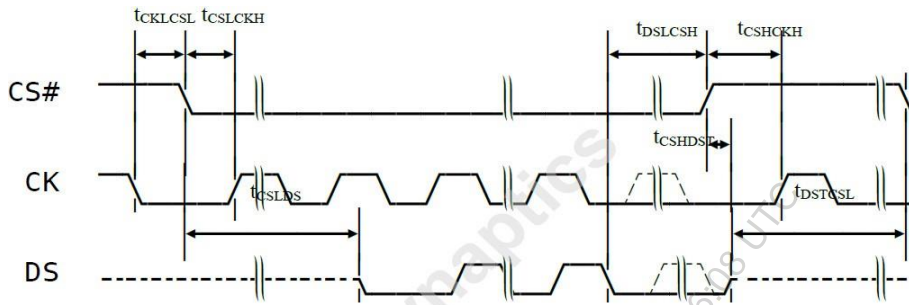


Figure 4. xSPI DS to CS# Signal Timing

### 4.6. SPI Timing

Applies across the full range of values listed in Table 6 unless otherwise specified.

Table 10. SCLK Cycle Time Configurable Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
TSCLK	SoC SPI SCLK cycle time	100 MHz SoC SPI controller input clock	20	—	655,340	ns

Table 11. Motorola SPI Mode 0/2 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T <sub>LS1</sub>	Time from SSn assertion to the first SCLK active edge	The first SPI cycle in a transfer	—	1.5	—	T <sub>sclk</sub>
		Subsequent SPI cycles	—	0.5	—	
T <sub>LS2</sub>	Time from the last SCLK inactive edge to SSn de-assertion	Other than the last SPI cycle	—	0.5	—	
		The last SPI cycle in a transfer	—	1.0	—	
T <sub>CH</sub>	SCLK high time	—	—	0.5	—	
T <sub>CL</sub>	SCLK low time	—	—	0.5	—	
T <sub>LH</sub>	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0.5	—	
		If Tx FIFO is empty	2	—	—	
T <sub>SET</sub>	Setup time MISO with regard to SCLK active edge	—	13.8	—	—	
T <sub>HOLD</sub>	Hold time MISO with regard to SCLK active edge	—	0	—	—	
T <sub>VAL1</sub>	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	T <sub>sclk</sub>
		Subsequent SPI cycles	—	0	—	
T <sub>VAL2</sub>	Time from SCLK inactive edge to MOSI data valid	—	0.12	—	1.28	ns

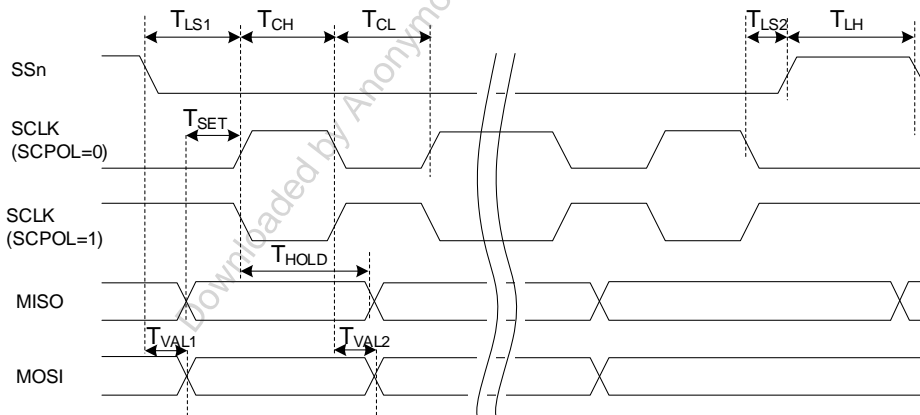


Figure 5. Motorola SPI Mode 0/2 (SCPH = 0)

Applies across the full range of values listed in Table 6 unless otherwise specified.

Table 12. Motorola SPI Mode 1/3 Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$T_{LS1}$	Time from SSn assertion to the first SCLK active edge	—	—	1.0	—	T <sub>sclk</sub>
$T_{LS2}$	Time from the last SCLK inactive edge to SSn de-assertion	—	—	1.0	—	
$T_{CH}$	SCLK high time	—	—	0.5	—	
$T_{CL}$	SCLK low time	—	—	0.5	—	
$T_{LH}$	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0	—	
		If Tx FIFO is empty	1.5	—	—	
$T_{SET}$	Setup time MISO with regard to SCLK active edge	—	—	30	—	ns
$T_{HOLD}$	Hold time MISO with regard to SCLK active edge	—	—	30	—	
$T_{VAL1}$	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	T <sub>sclk</sub>
		Subsequent SPI cycles	—	0	—	
$T_{VAL2}$	Time from SCLK inactive edge to MOSI data valid	—	—	0.5	—	ns

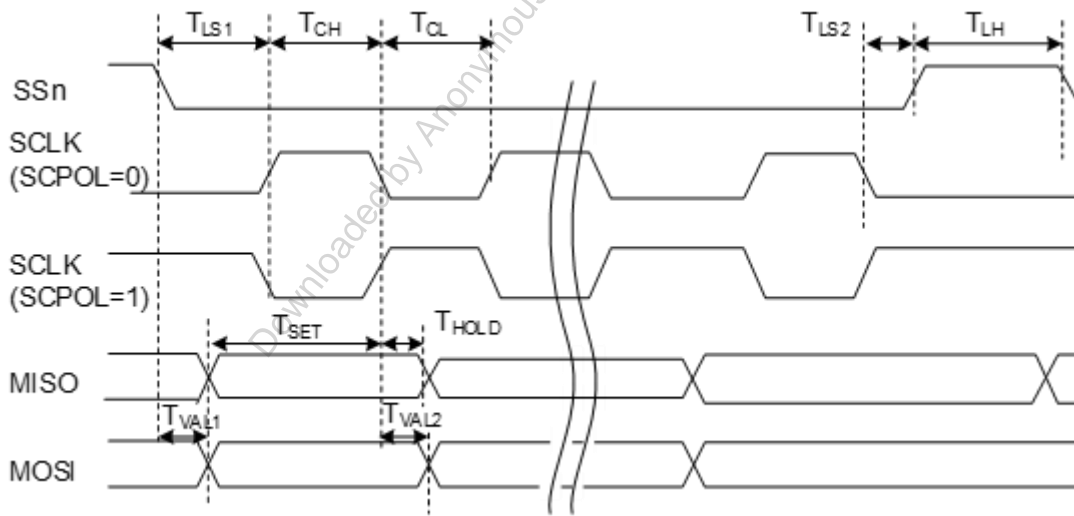


Figure 6. Motorola SPI Mode 1/3 (SCPH = 1)

## 4.7. UART Timing

Table 13. UART Timing

Symbol	Parameter	Condition	Min.	Typ. <sup>1</sup>	Max.	Units
—	Tx bit width	±5%	—	8.68	—	μs
—	Rx bit width	±5%	—	8.68	—	

1.The typical values are for 115.2 kbaud. Other baud rates may vary.

## 4.8. I2S Timing

### 4.8.1. I2S Host Mode Timing

Applies across the full range of values listed Table 6 unless otherwise specified.

Table 14. I2S Host Mode Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F <sub>BCLK</sub>	BCLK Frequency	—	16Fs	—	64Fs	Hz
F <sub>BCLK_PCM</sub>	BCLK Frequency in PCM Mono mode	—	8Fs	—	256Fs	
F <sub>BCLK_TDM</sub>	BCLK Frequency in TDM mode	—	16Fs	—	256Fs	
F <sub>S</sub>	—	—	8	—	192	kHz
D <sub>BCLK</sub>	BCLK duty cycle	—	—	50	—	%
T <sub>SDPD1</sub>	BCLK rising edge to SDATA output valid	—	—	2T <sub>AIOSYSCLK</sub>	—	ns
T <sub>LRPD</sub>	BCLK rising edge to LRCK valid	—	—	2T <sub>AIOSYSCLK</sub>	—	
T <sub>SDS</sub>	Set-up time SDATA input with regard to BCLK rising edge	—	—	-3T <sub>AIOSYSCLK2</sub>	—	
T <sub>SDH</sub>	Hold time SDATA Input with regard to BCLK rising edge	—	—	4T <sub>AIOSYSCLK2</sub>	—	
F <sub>MCLK</sub>	MCLK (not shown) output frequency	—	6.144	24.576	49.152	MHz
D <sub>MCLK</sub>	MCLK output duty cycle	—	—	50	—	%

1.BCLK may be inverted for more balanced setup and hold times.

2. Default AIOSYSCLK frequency is 300 MHz.

3. 2-channel 384 kHz.

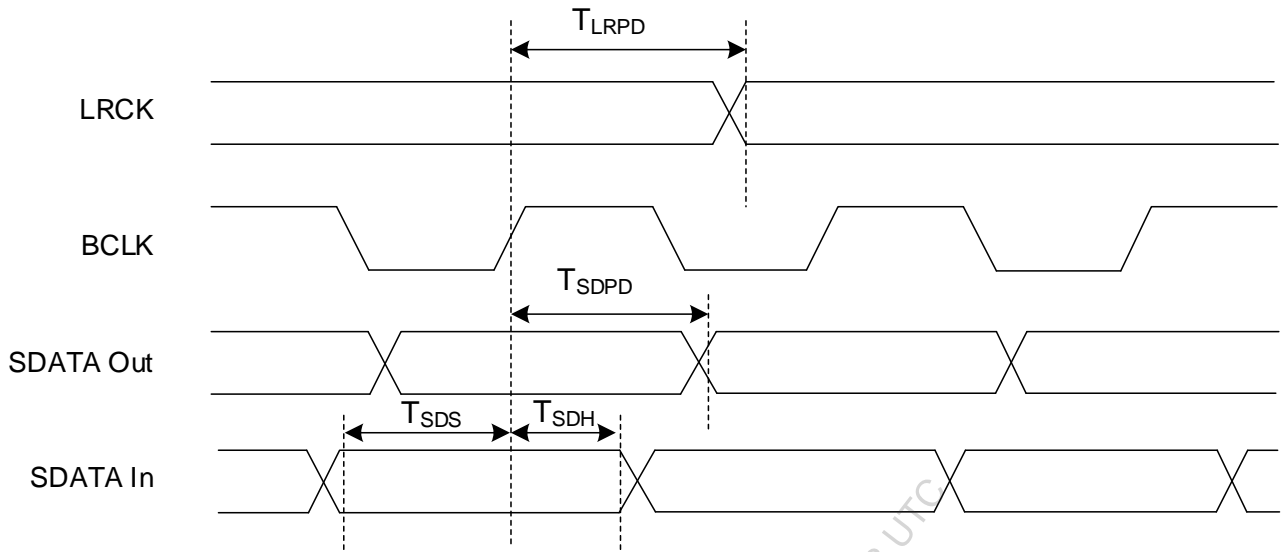


Figure 7. I2S host mode timing

### 4.8.2. I2S Target Mode Timing

Applies across the full range of values listed in Table 6. Recommended operating conditions and DC characteristics unless otherwise specified.

Table 15. I2S Target Mode Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$F_{BCLK}$	BCLK Frequency	—	16Fs	—	64Fs	Hz
$F_{BCLK\_PCM}$	BCLK Frequency in PCM Mono mode	—	8Fs	—	256Fs	
$F_{BCLK\_TDM}$	BCLK Frequency in TDM mode	—	16Fs	—	256Fs	
$F_s$	—	—	32	—	192	kHz
$D_{BCLK}$	BCLK duty cycle	—	—	50	—	%
$T_{LRS}$	Setup time LRCK input with regard to BCLK active edge	—	—	$-3T_{AIO\text{SYSCLK}1}$	—	ns
$T_{LRH}$	Hold time LRCK input with regard to BCLK active edge	—	—	$4T_{AIO\text{SYSCLK}1}$	—	
$T_{SDS}$	Setup time SDATA Input with regard to BCLK active edge	—	—	$-3T_{AIO\text{SYSCLK}1}$	—	
$T_{SDH}$	Hold time SDATA Input with regard to BCLK active edge	—	—	$4T_{AIO\text{SYSCLK}1}$	—	
$F_{MCLK}$	MCLK (not shown) input frequency	—	—	24.576	49.152	MHz
$D_{MCLK}$	MCLK input duty cycle	—	—	50	—	%

1.Default AIO\text{SYSCLK} frequency is 300 MHz.

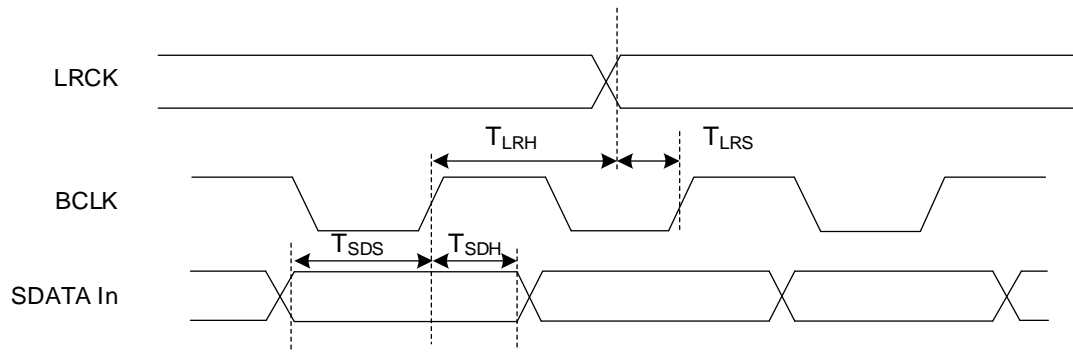


Figure 8. I2S target mode timing

### 4.9. Timer Counter Smart Pulse-Width Modulator (PWM) Timing

Table 16. Smart Pulse Width Modulator (PWM) Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$T_{PERIOD}$	PWM	16-bit counter	20 ns	—	16 days	—
		32-bit counter	20 ns	—	2824 years	—
—	PWM Duty Cycle	—	0	—	100	%
—	PWM Duty Cycle Resolution	—	10 ns	—	21 sec	—

1. Based on PWM clock is 100 MHz.

Downloaded by Anonymous () on 1 Jun 2026 19:16:08 UTC

## 4.10. USB 2.0 Timing

### 4.10.1. USB 2.0 DC Characteristics

Applies across the full range of values listed in Table 6 unless otherwise specified.

Table 17. USB 2.0 DC Electrical

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V <sub>IH</sub>	High (driven)	Note <sup>1</sup>	2.0	—	—	V
V <sub>IHZ</sub>	High (floating)		2.7	—	3.6	
V <sub>IL</sub>	Low		—	—	0.8	
V <sub>DI</sub>	Differential Input Sensitivity	$(D+) - (D-)$   Note <sup>1</sup>	0.2	—	—	V
V <sub>CM</sub>	Differential Common Mode Range	Includes V <sub>DI</sub> range Note <sup>1</sup>	0.8	—	2.5	
<b>Input Levels for High-speed</b>						
V <sub>HSSQ</sub>	High-speed squelch detection threshold (differential signal amplitude)	—	100	—	150	mV
V <sub>HSDSC</sub>	High-speed disconnect detection threshold (differential signal amplitude)	—	525	—	625	
V <sub>HSCM</sub>	High-speed data signaling common mode voltage range (guideline for receiver)	—	-50	—	500	
<b>Output Levels for Full-speed</b>						
V <sub>OL</sub>	Low	Note <sup>1</sup> , Note <sup>2</sup>	0.0	—	0.3	V
V <sub>OH</sub>	High (Driven)	Note <sup>1</sup> , Note <sup>3</sup>	2.8	—	3.6	
V <sub>OSEI</sub>	SEI	—	0.8	—	—	
V <sub>CRS</sub>	Output Signal Crossover voltage	Note <sup>4</sup>	1.3	—	2.0	
<b>Output Levels for High-speed</b>						
V <sub>HSOI</sub>	High-speed idle level	—	-10.0	—	10.0	mV
V <sub>HSOH</sub>	High-speed data signaling high	—	360	—	440	
V <sub>HSOL</sub>	High-speed data signaling low	—	-10.0	—	10.0	
V <sub>CHIRPJ</sub>	Chirp J level (differential voltage)	—	700	—	1100	
V <sub>CHIRPK</sub>	Chirp K level (differential voltage)	—	-900	—	500	
<b>Input Capacitance for Full-speed</b>						
C <sub>IND</sub>	Downstream Facing Port	Note <sup>5</sup>	—	—	150	pF
C <sub>INUB</sub>	Upstream Facing Port (without cable)	Note <sup>6</sup>	—	—	100	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C <sub>EDGE</sub>	Transceiver edge rate control capacitance	–	–	–	75	
<b>Terminations</b>						
R <sub>PU</sub>	Bus pull-up Resistor on Upstream facing port	1.5 kOhm ±5%	1.425	–	1.575	kOhm
R <sub>PD</sub>	Bus pull-down Resistor on Downstream Facing Port	15 kOhm ±5%	14.25	–	15.75	
Z <sub>INP</sub>	Input impedance exclusive of pullup/ pull-down (for full-speed)	–	300	–	–	
V <sub>TERM</sub>	Termination voltage for upstream facing port pull-up (R <sub>PU</sub> )	–	3.0	–	3.6	V
<b>Termination in High-speed</b>						
V <sub>HSTERM</sub>	Termination voltage in high-speed	–	–10	–	10	mV

**Notes:**

1. Measured at A or B connector.
2. Measured with RL of 1.425 kohm to 3.6 V.
3. Measured with RL of 14.25 kohm to GND.
4. Excluding the first transition from the idle state.
5. Measured at A receptacle.
6. Measured at B receptacle.

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

#### 4.10.1.1. USB 2.0 Source Electrical Characteristics

Applies across the full range of values listed Table 6 unless otherwise specified.

Table 18. USB High-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>Driver Characteristics</b>						
T <sub>HSR</sub>	Rise Time (10%–90%)	—	500	—	—	ps
T <sub>HSF</sub>	Fall Time (10%–90%)	—	500	—	—	
Z <sub>HSDRV</sub>	Driver Output Resistance (which also serves as high-speed termination)	—	40.5	—	49.5	Ohm
<b>Clock Timings</b>						
T <sub>HSDRAT</sub>	High-speed Data Rate	—	479.760	—	480.240	Mb/s
T <sub>HSFRAM</sub>	Microframe Interval	—	124.9375	—	125.0625	μs
T <sub>HRSRFI</sub>	Consecutive Microframe Interval Difference	—	—	—	4 high-speed bit times	—

Table 19. USB Full-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>Driver Characteristics</b>						
T <sub>FR</sub>	Rise Time	—	4	—	20	ns
T <sub>FF</sub>	Fall Time	—	4	—	20	
T <sub>FRFM</sub>	Differential Rise and Fall Time Matching	T <sub>FR</sub> /T <sub>FF</sub> Note <sup>1</sup>	90	—	111.11	%
Z <sub>DRV</sub>	Driver Output Resistance for driver which is not high-speed capable.	—	28	—	44	Ohm
<b>Clock Timings</b>						
T <sub>FDRATHS</sub>	Full-speed Data Rate for hubs and devices which are high speed capable.	Average bit rate	11.9940	—	12.0060	Mb/s
T <sub>FDRATE</sub>	Full-speed Data Rate for devices which are high-speed capable.	Average bit rate	11.9700	—	12.0300	
T <sub>FRAME</sub>	Frame Interval	—	0.9995	—	1.0005	ms
T <sub>RFI</sub>	Consecutive Frame Interval Jitter	No clock adjustment	—	—	42	ns
<b>Full-speed Data Timings</b>						
T <sub>DJ1</sub>	Source Jitter Total (including frequency tolerance): To Next Transition	Note <sup>1</sup> , Note <sup>2</sup> , Note <sup>3</sup> , Note <sup>4</sup>	–3.5	—	3.5	ns
T <sub>DJ2</sub>	For Paired transitions		–4	—	4	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$T_{FDEOP}$	Source Jitter for Differential Transition to SEO Transition	Note <sup>3</sup>	-2	—	5	
$T_{JR1}$	Receiver jitter: To Next Transition	Note <sup>3</sup>	-18.5	—	18.5	
$T_{JR2}$	For Paired Transitions	—	-9	—	9	
$T_{FEOPT}$	Source SEO interval of EOP	—	160	—	175	
$T_{FEOPR}$	Receiver SEO interval of EOP	Note <sup>5</sup>	82	—	—	
$T_{FST}$	Width of SEO interval during differential transition	—	—	—	14	

**Notes:**

1. Excluding the first transition from the idle state.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. For both transitions of differential signaling.
5. Must accept as valid EOP.

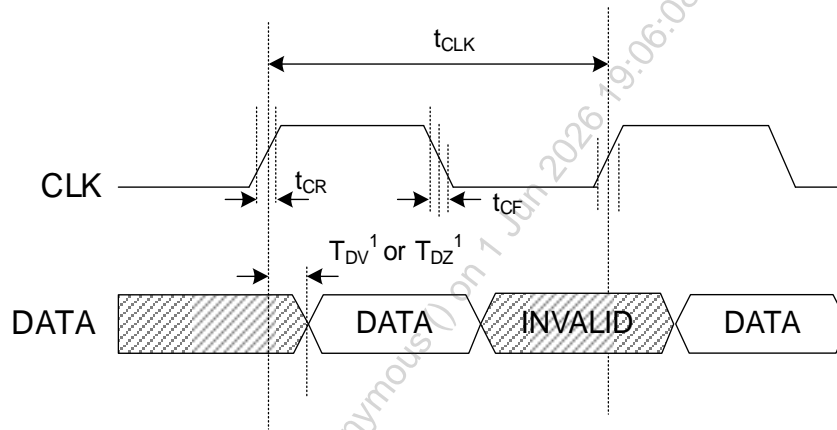
Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

### 4.11. Pulse Density Modulation Timing Characteristics

Table 20. Pulse Density Modulation (Classic PDM) Timing Parameters – SDR Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t <sub>CLK</sub>	PDM Clock	—	—	—	F <sub>Aiosysclk</sub> /41	MHz
t <sub>D</sub>	Clock Duty Cycle	—	—	50	—	%
t <sub>CR</sub>	Clock Rise Time	10–90%	—	—	T <sub>Aiosysclk</sub>	ns
t <sub>CF</sub>	Clock Fall Time	90–10%	—	—	T <sub>Aiosysclk</sub>	

1.Default F<sub>Aiosysclk</sub> is 300 MHz.



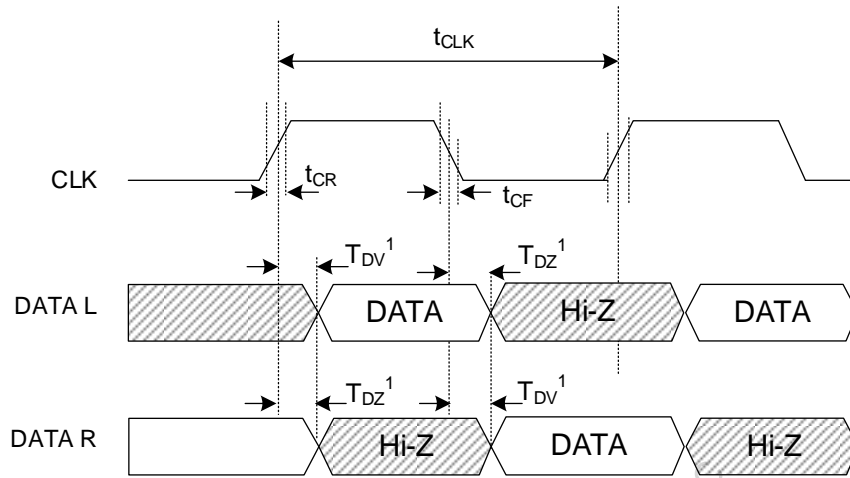
1. PDM data sampling point is configurable across the  $t_{CLK}$  period.

Figure 9. PDM Timing – SDR Mode

Table 21. Pulse Density Modulation (Half Cycle PDM) Timing Parameters – DDR Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t <sub>CLK</sub>	PDM Clock	—	—	—	F <sub>Aiosysclk</sub> /41	MHz
t <sub>D</sub>	Clock Duty Cycle	—	—	50	—	%
t <sub>CR</sub>	Clock Rise Time	10–90%	—	—	T <sub>Aiosysclk</sub>	ns
t <sub>CF</sub>	Clock Fall Time	90–10%	—	—	T <sub>Aiosysclk</sub>	

1.Default F<sub>Aiosysclk</sub> is 300 MHz.



1. PDM data sampling point is configurable across the  $t_{CLK}$  period.

Figure 10. PDM timing – DDR Mode

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 4.12. SDIO v3.0 Interface

### 4.12.1. SDIO v3.0 Interface Overview

The SRW1500 Series WLAN section provides support for SDIO version 3.0 at 1.8 V signaling, including the new UHS-I modes:

DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes.

- SDR12: SDR up to 25 MHz
- SDR25: SDR up to 50 MHz
- SDR50: SDR up to 100 MHz
- SDR104: SDR up to 150 MHz
- DDR50: DDR up to 50 MHz

**Note:** The SRW1500 Series is backward compatible with SDIO v2.0 host interfaces. The SDIO interface can also map the interrupt signal to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled by strapping options.

### 4.12.2. SDIO Pins

Table 22. SDIO pin descriptions

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

**Note:** Per Section 6 of the SDIO specification, pull-ups in the 10 k $\Omega$  to 100 k $\Omega$  range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

### 4.12.3. SDIO Timing

#### 4.12.3.1. SDIO Default Mode Timing

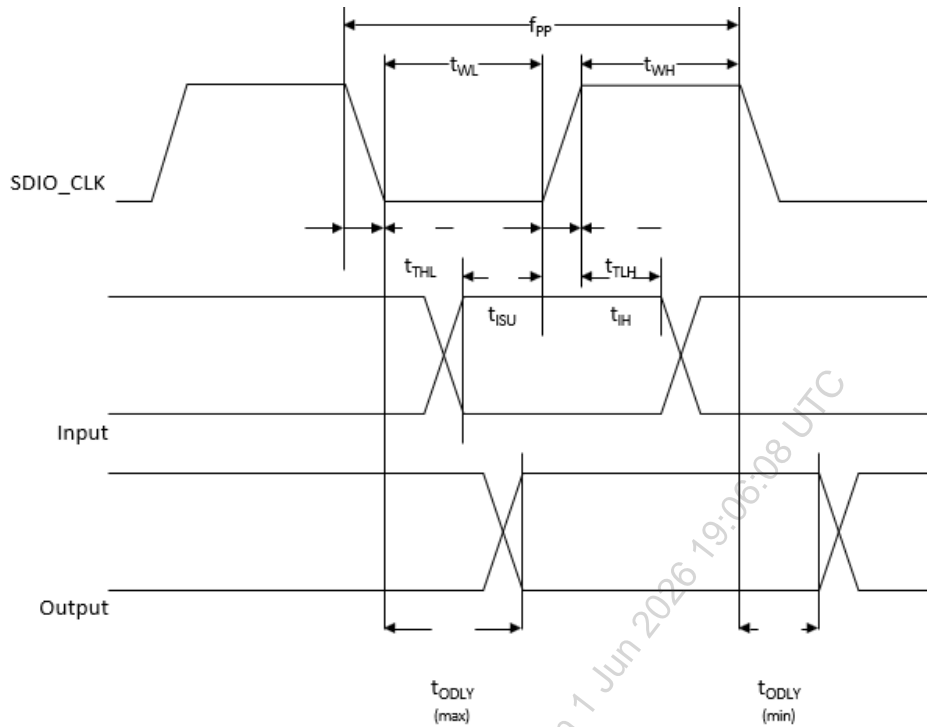


Figure 11. SDIO bus timing (default mode)

Table 23. SDIO bus timing1 parameters (default mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
<b>SDIO CLK (All values are referred to minimum VIH and maximum VIL<sup>2</sup>)</b>					
Frequency – Data Transfer mode	f <sub>PP</sub>	0	–	25	MHz
Frequency – Identification mode	f <sub>OD</sub>	0	–	400	kHz
Clock low time	t <sub>WL</sub>	10	–	–	ns
Clock high time	t <sub>WH</sub>	10	–	–	ns
Clock rise time	t <sub>TLH</sub>	–	–	10	ns
Clock low time	t <sub>THL</sub>	–	–	10	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
Input setup time	t <sub>ISU</sub>	5	–	–	ns
Input hold time	t <sub>IH</sub>	5	–	–	ns
<b>Outputs: CMD, DAT (referenced to CLK)</b>					
Output delay time – Data Transfer mode	t <sub>ODLY</sub>	0	–	14	ns
Output delay time – Identification mode	t <sub>ODLY</sub>	0	–	50	ns

1. Timing is based on CL ≤ 40 pF load on CMD and Data.

2. Minimum (Vih) = 0.7 × VDDIO and maximum (Vil) = 0.2 × VDDIO.

### 4.12.4. SDIO Bus Timing Specifications in SDR Modes

#### 4.12.4.1. Clock Timing

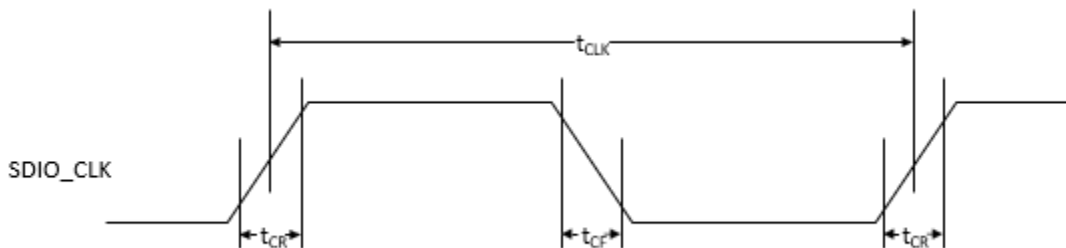


Figure 12. SDIO clock timing (SDR modes)

Table 24. SDIO bus clock timing parameters (SDR modes)

Parameter	Symbol	Minimum	Maximum	Unit	Symbol
-	$t_{CLK}$	40	—	ns	SDR12 mode
		20	—	ns	SDR25 mode
		10	—	ns	SDR50 mode
		6.6	—	ns	SDR104 mode (up to 150 MHz)
-	$t_{CR}, t_{CF}$	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (maximum) @100 MHz, CCARD = 10 pF
Clock duty	-	30	70	%	-

### 4.12.4.2. Device Input Timing

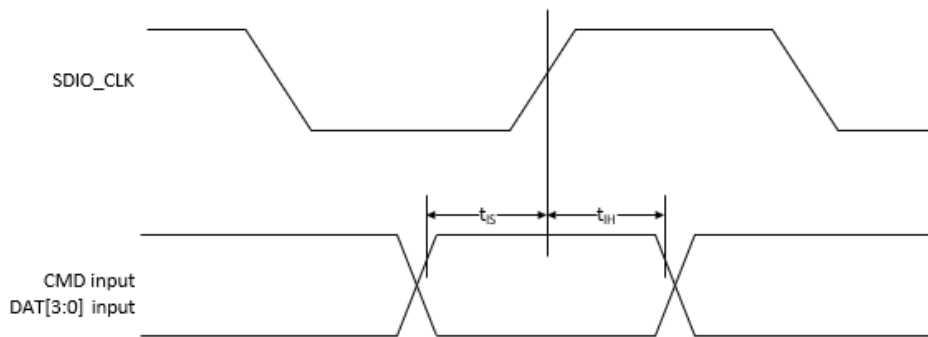


Figure 13. SDIO bus input timing (SDR modes)

Table 25. SDIO bus input timing parameters (SDR modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
$t_{is}$	1.4	—	ns	CCARD = 10 pF, VCT = 0.975V
$t_{ih}$	0.80	—	ns	CCARD = 5 pF, VCT = 0.975V
SDR50 Mode				
$t_{is}$	3.00	—	ns	CCARD = 10 pF, VCT = 0.975V
$t_{ih}$	0.80	—	ns	CCARD = 5 pF, VCT = 0.975V

### 4.12.4.3. Device Output Timing—SDR Modes up to 100 MHz

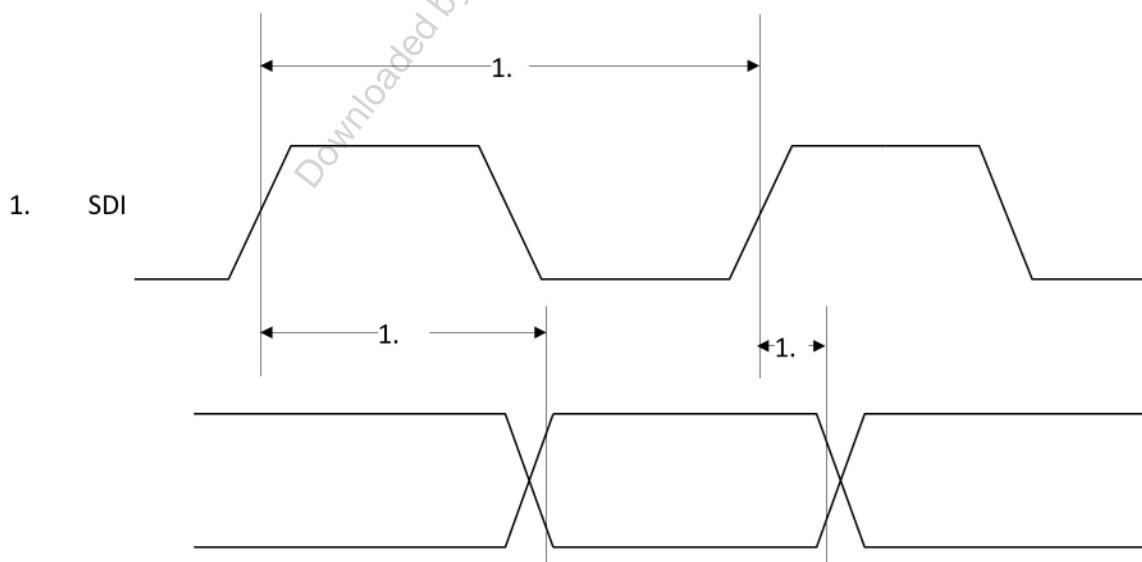


Figure 14. SDIO bus output timing (SDR modes up to 100 MHz)

Table 26. SDIO bus output timing parameters (SDR modes up to 100 MHz)

Symbol	Minimum	Maximum	Unit	Comments
$t_{ODLY}$	—	7.5	ns	$t_{CLK} \geq 10$ ns CL= 30 pF using driver type B for SDR50
$t_{ODLY}$	—	14.0	ns	$t_{CLK} \geq 20$ ns CL= 40 pF using for SDR12, SDR25
$t_{OH}$	1.5	—	ns	Hold time at the $t_{ODLY}$ (min) CL= 15 pF

#### 4.12.4.4. Device Output Timing—SDR Modes 100 MHz to 150 MHz

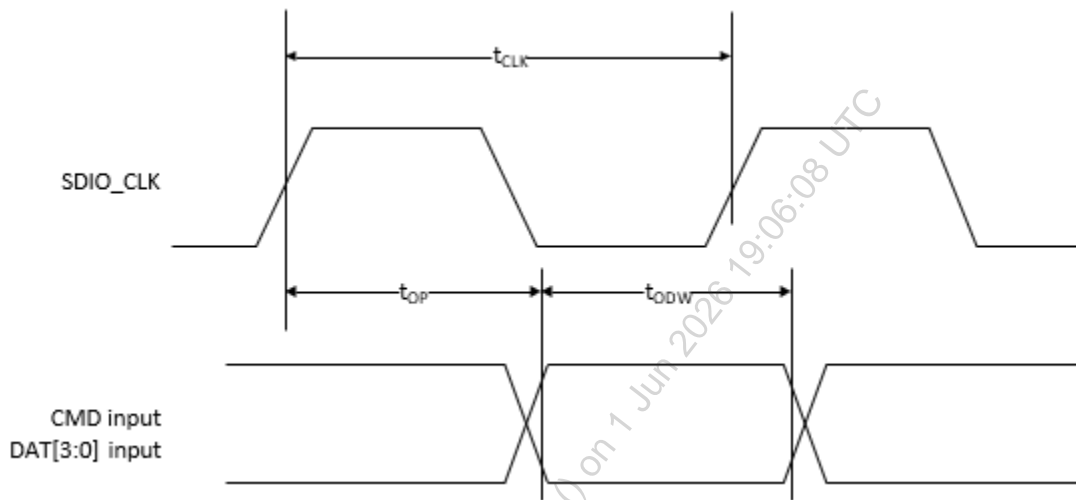


Figure 15. SDIO bus output timing (SDR modes 100 MHz to 150 MHz)

Table 27. SDIO bus output timing parameters (SDR modes 100 MHz to 150 MHz)

Symbol	Minimum	Maximum	Unit	Comments
$t_{OP}$	0	2	UI	Card output phase
$\Delta t_{OP}$	-350	+1550	ps	Delay variation due to temperature change after tuning
$t_{ODW}$	0.60	—	UI	$t_{ODW} = 4$ ns @ 150 MHz

**Notes:**

1.  $\Delta t_{OP} = +1550$  ps for junction temperature of  $\Delta t_{OP} = 90$  degrees during operation.
2.  $\Delta t_{OP} = -350$  ps for junction temperature of  $\Delta t_{OP} = -20$  degrees during operation.
3.  $\Delta t_{OP} = +2600$  ps for junction temperature of  $\Delta t_{OP} = -20$  to  $+125$  degrees during operation.

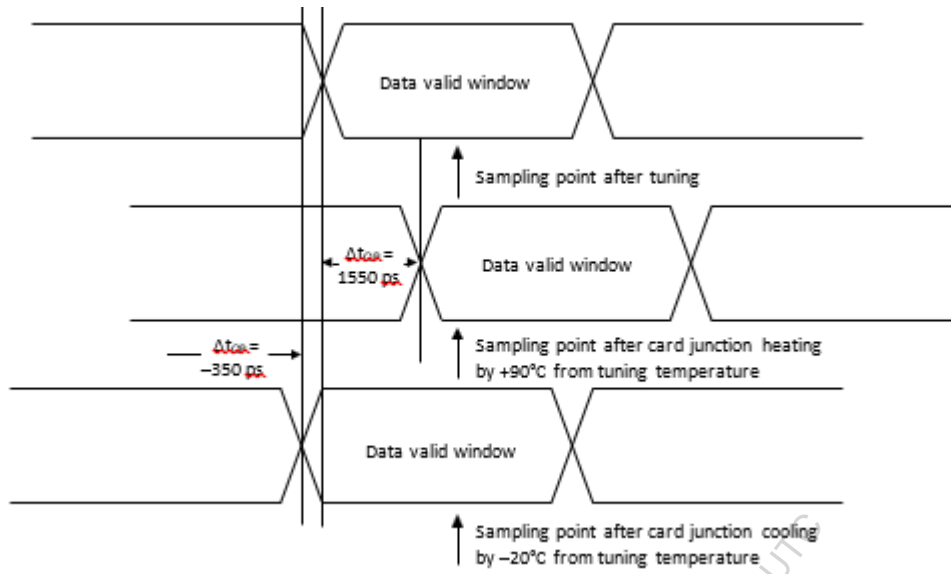


Figure 16.  $\Delta t_{OP}$  consideration for variable data window (SDR 104 mode)

Downloaded by Anonymous () on 1 Jun 2026 19:00:08 UTC

### 4.12.4.5. SDIO Bus Timing Specifications in DDR50 Mode

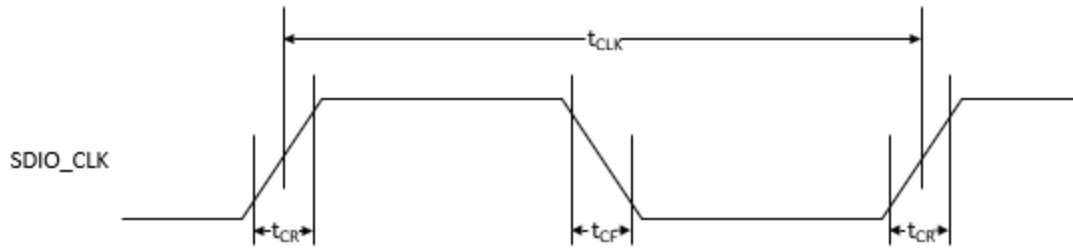


Figure 17. SDIO clock timing (DDR50 mode)

Table 28. SDIO bus clock timing parameters (DDR50 mode)

Parameter	Symbol	Minimum	Typical	Maximum	Comments
—	$t_{CLK}$	20	—	ns	DDR50 mode
—	$t_{CR}, t_{CF}$	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @ 50 MHz, CCARD = 10 pF
Clock duty	—	45	55	%	—

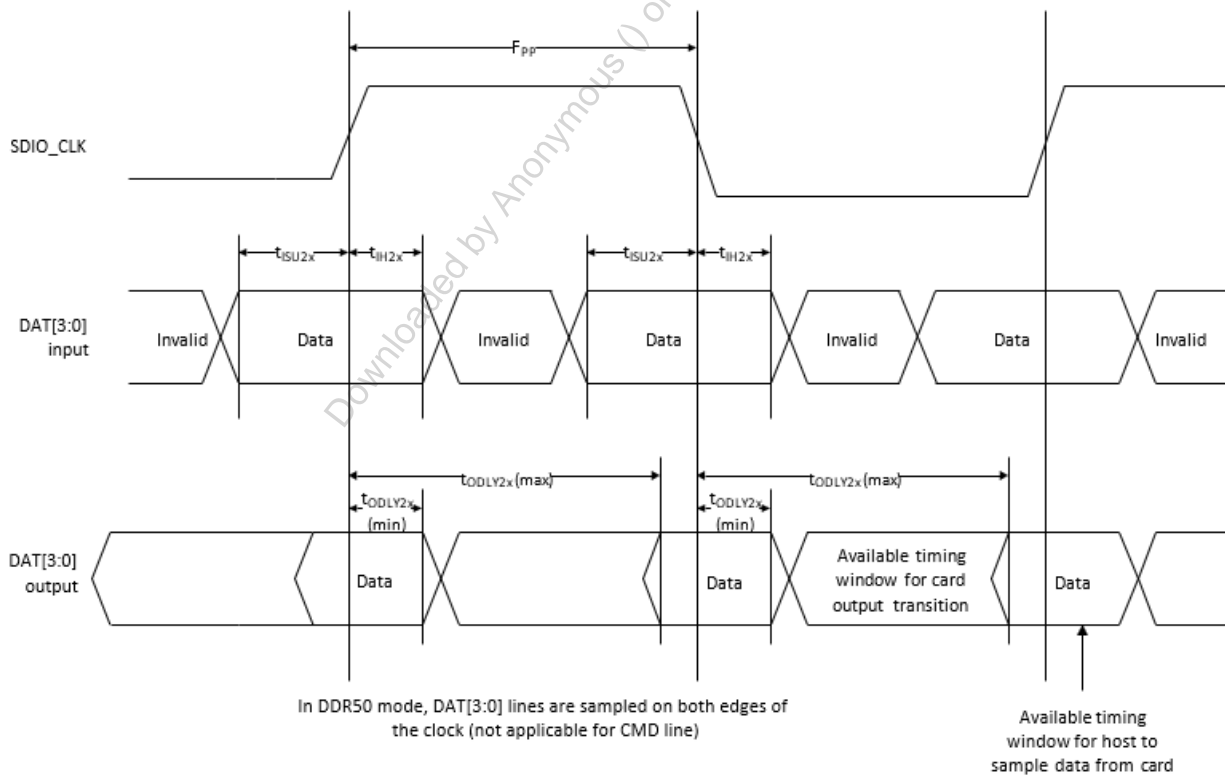


Figure 18. SDIO data timing (DDR50 mode)

Table 29. SDIO bus timing parameters (DDR50 mode)

Parameter	Symbol	Min.	Typ.	Max.	Comments
<b>Input CMD</b>					
Input setup time	tISU	6	–	ns	CCARD < 10 pF (1 Card)
Input hold time	tIH	0.8	–	ns	CCARD < 10 pF (1 Card)
<b>Output CMD</b>					
Output delay time	tODLY	–	13.7	ns	CCARD < 30 pF (1 Card)
Output hold time	tOH	1.5	–	ns	CCARD < 15 pF (1 Card)
<b>Input DAT</b>					
Input setup time	tISU2x	3	–	ns	CCARD < 10 pF (1 Card)
Input hold time	tIH2x	0.8	–	ns	CCARD < 10 pF (1 Card)
<b>Output DAT</b>					
Output delay time	tODLY2x	–	7.5	ns	CCARD < 25 pF (1 Card)
Output hold time	tODLY2x	1.5	–	ns	CCARD < 15 pF (1 Card)

Downloaded by Anonymous () on 1 Jun 2026 19:15:08 UTC

## 4.13. JTAG Interface

The SRW1500 Series supports IEEE 1149.1 JTAG boundary scan to access the chip's internal blocks and backplane for system bring-up and debugging. This interface allows Synaptics to assist customers with proprietary debug and characterization test tools. It is highly recommended that access is provided by using either test points or a header on all PCB designs.

In addition to the Arm debug interface, an internal JTAG host on the DAP allows access to test access points (TAPs) in the SRW1500 Series for hardware debugging.

### 4.13.1. JTAG Timing

Table 30. JTAG timing characteristics

Signal Name	Period	Output Max	Output Min	Setup	Hold
TCK	125 ns	—	—	—	—
TDI	—	—	—	20 ns	0 ns
TMS	—	—	—	20 ns	0 ns
TDO	—	100 ns	0 ns	—	—

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 5. Power Supplies and Power Management

### 5.1. Power Supply Topology

The SRW1500 Series contains a power management unit (PMU) featuring one buck regulator and several LDO regulators. All regulators are programmable via the PMU registers. The PMU is powered by the 3.0–5.0 V and 1.71–1.89 V external supplies. All other voltages are provided by internal SRW1500 Series regulators.

A single control signal, `CHIP_REG_ON`, is used to power-up the regulators and take the respective sections out of reset as per power-up sequence. All regulators are powered down only when control signals are de-asserted.

The SRW1500 Series features multiple low-power consumption modes. Most supply domains and LDOs could be shut down while the buck regulator runs in LP PFM mode and maintains the minimum voltage required, thus reducing leakage current.

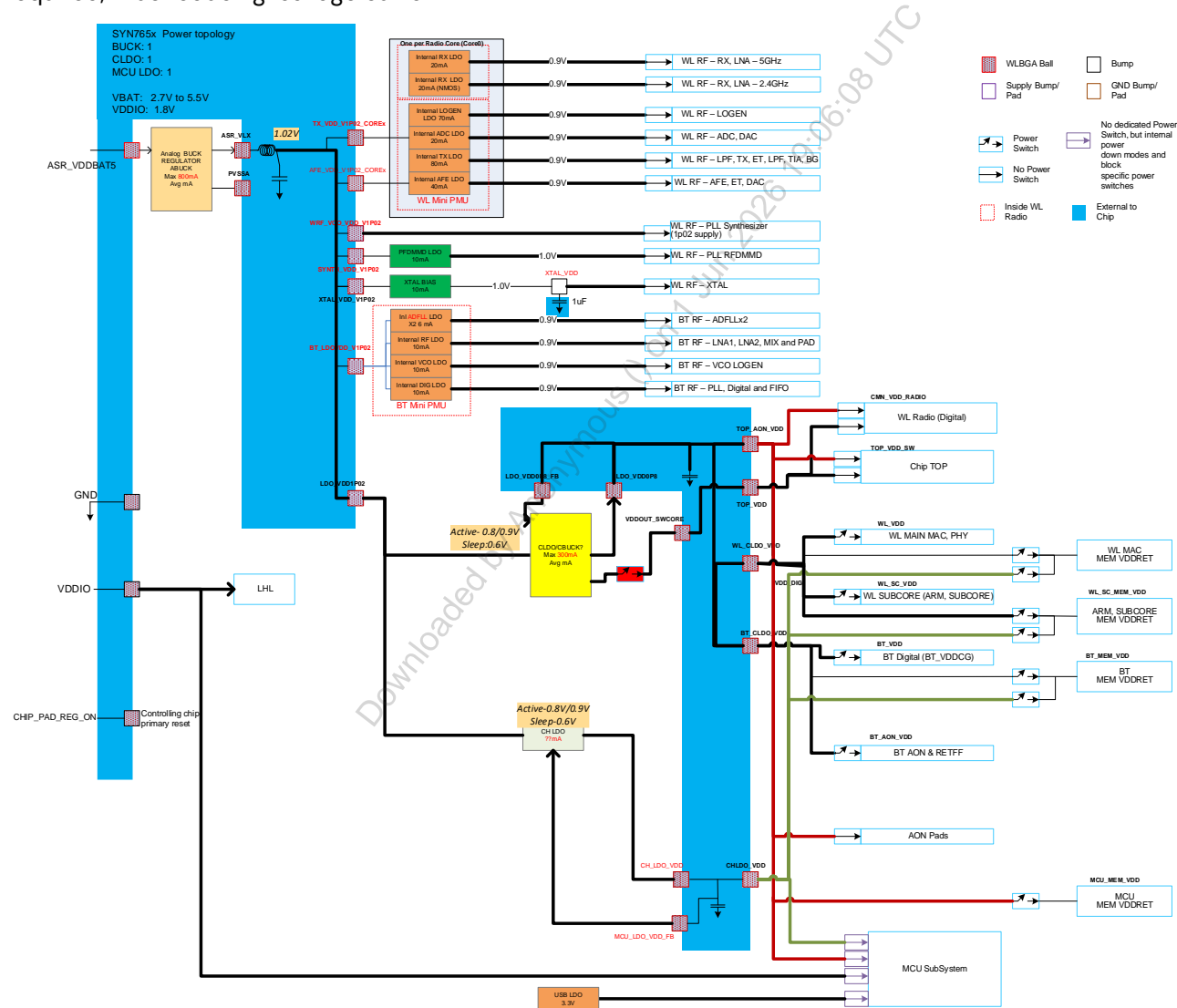


Figure 19. Typical power topology: VBAT and VDDIO

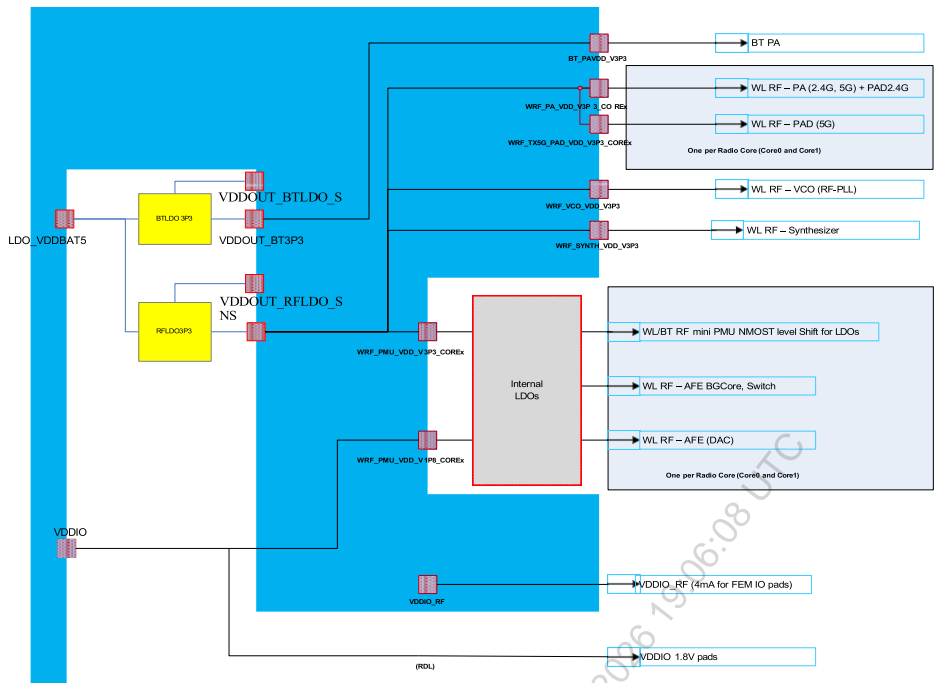


Figure 20. Typical power topology: 1.8 V and 3.3 V

Downloaded by Anonymous () on 1 Jun 2026 15:06:08 UTC

## 5.2. Power Topology

The SRW1500 Series is designed with independent power-saving mode for WLAN, BT, and MCU which provides significant power savings by putting the SRW1500 Series into various power management states appropriate to the operating environment and activities being performed.

The PMU enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable.

The SRW1500 Series power states are described as follows:

- Active mode — All blocks in the SRW1500 Series are powered up and fully functional with active carrier sensing, and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current.
- Partially active state –
  - Active (MCU + BT) – In this mode, MCU is active and BT is also enabled by MCU and BT is in active state while WLAN is kept in OFF state.
  - Active (MCU + WLAN) – In this mode, MCU is active and WLAN is enabled by MCU while BT is kept in OFF state.
- Deep Sleep mode — Most of the chip, including both the analog and digital domains, and most of the regulators are powered off. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to minimize active power. The 32.768 kHz LPO clock is available so that the chip can wake up and transition to Active mode. Logic states in the digital core are saved and preserved in a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers or an external interrupt, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy hardware reinitialization. In Deep-sleep mode, the primary source of power consumption is leakage current. MCU subsystem also supports full retention and standby modes.
- Power-down mode — The SRW1500 Series is effectively powered off by shutting down all internal regulators. External logic brings the chip out of this mode by re-enabling the internal regulators.

## 5.3. Power Off Shutdown

In stand-alone systems (no external host), the SRW1500 Series operates as the host and can enter shutdown when not needed using `CHIP_PAD_REG_ON`. The device restores operation through the `CHIP_PAD_REG_ON` pin, which controls power-up and reactivation of internal circuitry.

In systems with an external host, shutdown is initiated by the host while the SRW1500's I/O domain stays powered to avoid loading shared interfaces. In this mode, power-up remains controlled by the `CHIP_PAD_REG_ON` pin, while wake-up events are triggered by a host-provided GPIO, enabling precise host-managed power sequencing and minimizing system power consumption.

When the SRW1500 Series is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

The SRW1500 Series PMU has an undervoltage lockout (ULVO). When it detects either  $V_{BAT} < 2.23\text{ V}$  or  $V_{DDIO} < 1.52\text{ V}$ , it will shut down the PMU (chip).

## 5.4. Power-up, Power-down, and Reset Circuits

The SRW1500 Series has control signals that enable or disable the SRW1500 Series circuits and the internal regulator blocks, allowing the host to control power consumption.

Table 31. Power-up, power-down, and reset control signals

Signal	Description
CHIP_REG_ON	This signal is used by the PMU to power-up the chip. When this pin is high, the regulators are enabled, and the MCU, WLAN and BT are out of reset following a reset sequencing. When this pin is low, the SRW1500 Series is in reset. BT and WL ON/OFF is controlled by MCU FW. Supported mode is MCU + BT, MCU+WLAN and MCU+BT+WLAN.

Table 32. CHIP\_PAD\_REG\_ON electrical specification

Parameter	Symbol	Conditions	Min.	Type	Max.	Unit
Input high voltage	$V_{IH}$	For CHIP_PAD_REG_ON	1	—	1.89	V
Input low	$V_{IL}$	—	VSS	—	0.3	V
Pull-down	$R_{PD}$	—	—	50	—	k $\Omega$
Leakage	$I_{LEAK\_DIS}$	—	—	28	—	nA
REG OFF time	$T_{REG\_OFF}$	$C_{REG\_ON} \leq$	2	—	—	ms

## 5.5. Internal Regulator Electrical Specifications

### 5.5.1. PMU

Table 33. PMU Electrical specification

Parameter	Symbol	Conditions	Min.	Typical	Max.	Unit
Input supply voltage	$V_{bat}$	—	2.5	3.6	5	V
I/O supply voltage	$V_{ddio}$	—	1.71	1.80	1.89	V
Input supply voltages ramp-up time	$T_{ramp}$	—	40 $\mu$ s	—	100 ms	—
Power-up time	$T_{pu}$	CLDO output reaching 0.8 V with respect to REG_ON	—	295	—	$\mu$ s
		ASR output reaching 1.02 V with respect to REG_ON	—	315	—	$\mu$ s
VDDIO brownout threshold	$V_{BRWO\_rise}$	Rising	—	1.597	—	V
	$V_{BRWO\_fall}$	Falling	—	1.424	—	V

### 5.5.2. Analog Switching Regulator

Table 34. Analog switching regulator (ASR) electrical specification

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input supply	$V_{bat}$	DC voltage range inclusive of	2.5	3.6	5	V
Switching	$F_{sw}$	PWM mode	—	3.2	—	MHz
Output	$I_{out}$	PWM mode	—	—	400	mA
Output	$I_{out\_limit}$	Peak inductor current	—	0.75	—	A
Output	$V_{out}$	—	—	1.02	—	V
DC accuracy	$V_{out\_\Delta err}$	Includes line and load regulation.	−4	—	4	%
		After trim at PWM mode.	−2	—	2	%
Efficiency <sup>1</sup>	$E_{ff\_pwm}$	PWM peak efficiency at 200 mA. Typical inductor DCR is 114 m $\Omega$ . ACR typical is 1 $\Omega$ . FSW = 3.2 MHz.	—	89	—	%
	$E_{ff\_lppfm}$	LPPFM efficiency at 50 mA. Typical inductor DCR is 114 m $\Omega$ . ACR typical is 1 $\Omega$ .	—	89	—	%
Start-up time	$T_{su}$	With VDDIO = 1.8 V as always-on. Measure from rising edge of REG_ON to the ASR output reaching 1.16 V.	—	315	—	$\mu$ s

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
External inductor	L	Effective inductance (Refer to the Synaptics reference board BOM.)	0.6	2.2	—	μH
External output	C <sub>o</sub>	Effective load capacitance (Refer to the Synaptics reference board BOM.)	1.3	4.7	—	μF
External input capacitor <sup>2</sup>	C <sub>in</sub>	Effective load capacitance (Refer to the Synaptics reference board BOM.)	0.67	4.7	—	μF

**Notes:**

1. Efficiency numbers are assumed at typical condition (that is, VBAT = 3.6 V, VDDIO = 1.8 V, ASR VOUT = 1.02V, CLDO VOUT = 0.8V, and room temperature is 27°C). Component parts used for L = 2.2 μH, and CO = 4.7 μF.
2. The minimum capacitor value refers to the effective value after taking into account part-to-part tolerance, DC-bias, temperature, and aging. The typical capacitor value is the manufacturer-specified nominal part value. The maximum capacitor value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there are any). Refer to the Synaptics reference board BOM for preferred components.

**5.5.3. CLDO & CHLDO**

Table 35. CLDO Electrical specification

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input supply voltage	V <sub>in</sub>	Regular mode Dropout voltage requirement must be met for performance	—	1.02	—	V
Input supply voltage	V <sub>in</sub>	Bypass Mode	—	0.8	—	V
Input supply voltage	V <sub>in</sub>	Low power	—	0.8	—	V
Nominal output voltage	V <sub>out</sub>	Regular mode	—	0.8	—	V
Output voltage programmability	—	Range DC Accuracy at any step	0.66 -3	—	0.9 3	V %
Dropout voltage	—	Max load	120	—	—	mV
Output current @	I <sub>out</sub>	—	0.1	—	170	mA
Output current @	I <sub>out</sub>	—	0.1	—	20	mA
Quiescent current	IQ_NoLoa	No load	—	10	12.6	μA
	IQ_MaxLo	Max load.	—	3.68	5.34	mA
Power-down current	I <sub>q_pd</sub>	VIN= 1.02V Typ at Junction Temp 25 C, Max at Junction Temp 85C	—	0.73	2.7	uA

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Bypass current	IQ_byp	VIN= 0.8V (Chip DSO) Typ at Junction Temp 25 C, Max at Junction Temp 85C	—	0.15	0.34	uA
Line regulation	—	VIN from (VOUT+ Vd) - 1.3V; IOU=200mA.	—	—	1	mV
Load regulation	—	Load from 1-200 mA; VIN=1.02V.	—	—	5	mV
Load step error	—	Load from 1-125 mA in 100 ns Load from 125mA – 200mA in 100 ns at VIN=1.22 V;CO=0.5 $\mu$ F effective.	—	—	61	mV
PSRR	—	Freq from 100-100 kHz at ½ max load. Freq at FSW at ½ max load	20	—	—	dB
Turn-on time	Ton	Measure from pu signal to VOUT=0.8V with reference ready. CO = 1 $\mu$ F	—	40	—	$\mu$ s
Turn-on time	Ton	Measure from adj signal change VOUT= 0.7 to 0.8 V with reference ready. CO = 1 $\mu$ F	—	30	—	$\mu$ s
In-rush current	linrush	CO = $\mu$ F	—	50	71	mA
Output capacitor	Co	See components section for details	0.6	1	—	$\mu$ F

#### 5.5.4. BTLDO3P3

Table 36. BTLDO3P3 Electrical specification

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input supply voltage	Vbat	DC voltage range inclusive of disturbances	2.5	3.6	5	V
Nominal output voltage	Vout	—	—	3.3	—	V
Output voltage programmability	—	Range	2.86	—	3.465	V
		Accuracy at any step	-4	—	4	%
Dropout voltage	—	Maximum load	—	—	200	mV
Output current	Iout	—	0.2	—	450	mA
Turn-on time	Ton	Measure from VOUT ramping from 0 V to 3.3 V with reference	—	—	66	$\mu$ s
Output current limit	Iout_limit	—	—	1060	1420	mA
In-rush current	linrush	—	—	155	220	mA

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output capacitor <sup>1</sup>	CO	Refer to the Synaptics reference board BOM.	1	4.7	—	μF

1.The minimum capacitor value refers to the effective value after considering part-to-part tolerance, DC-bias, temperature, and aging. The typical capacitor value is the manufacturer-specified nominal part value. This includes all decoupling caps connected at the load side (if there are any). Refer to the Synaptics reference board BOM for preferred components.

### 5.5.5. RFLDO3P3

Table 37. RFLDO3P3 electrical specification

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input supply voltage	Vbat	DC voltage range inclusive of	2.5	3.6	5	V
Nominal output voltage	Vout	—	—	3.3	—	V
Output voltage programmability	—	Range	2.86	—	3.465	V
		Accuracy at any step	−4	—	4	%
Dropout voltage	—	Maximum load	—	—	200	mV
Output current	Iout	—	0.3	—	450	mA
Turn-on time	Ton	Measure from the rising edge of WL_REG_ON to VOUT = 3.3 V with reference ready. CO = 4.7	—	—	66	μs
Output current limit	Iout_limit	—	—	1060	1420	mA
In-rush current	Iinrush	—	—	155	220	mA
Output capacitor <sup>1</sup>	Co	Refer to the Synaptics reference board BOM	1	4.7	—	μF

1.The minimum capacitor value refers to the effective value after considering part-to-part tolerance, DC-bias, temperature, and aging. The typical capacitor value is the manufacturer-specified nominal part value. This includes all decoupling caps connected at the load side (if there are any). Refer to the Synaptics reference board BOM for preferred components.

## 5.6. Sequencing of Reset and Regulator Control Signals

The SRW1500 Series has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described in Table 31. Power-up, power-down, and reset control signals. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

The SRW1500 Series has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating PCIe accesses. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50  $\mu\text{s}/\text{V}$ .

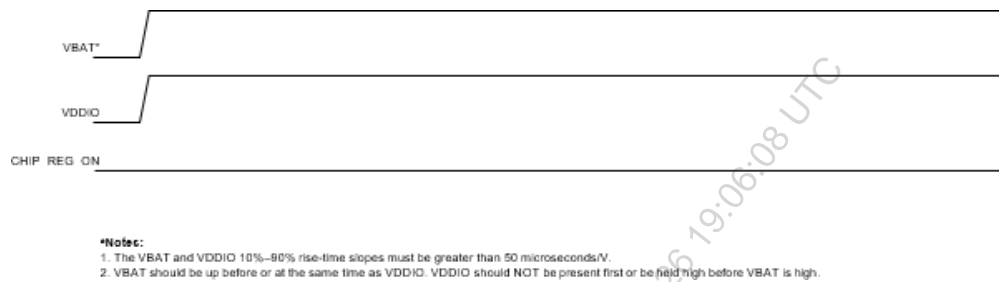


Figure 21. WLAN = ON, Bluetooth = ON

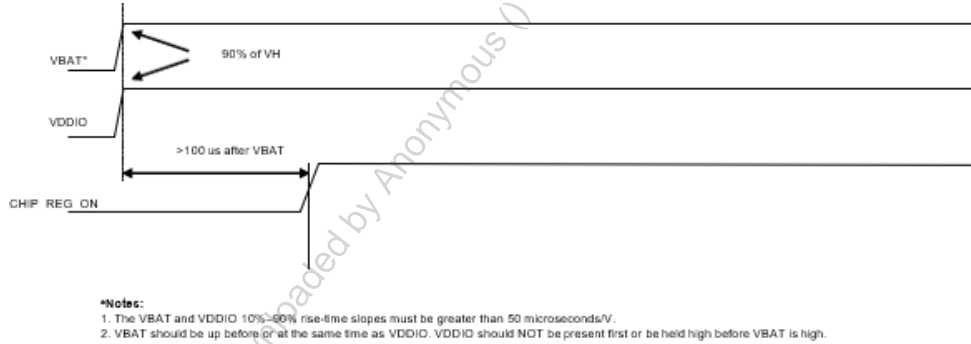


Figure 22. WLAN = OFF, Bluetooth = OFF

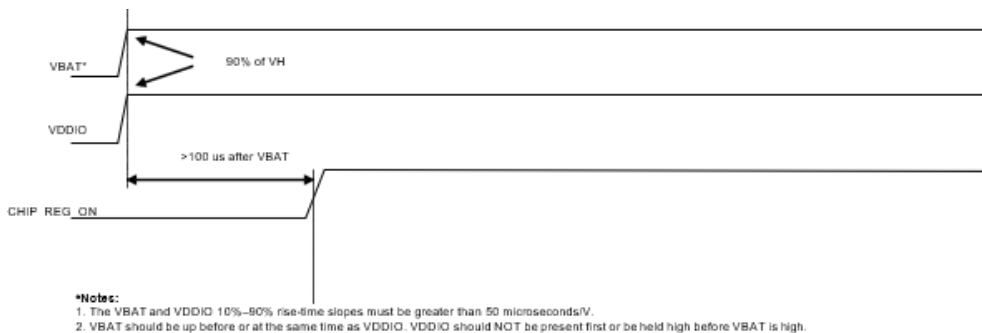


Figure 23. WLAN = ON, Bluetooth = OFF

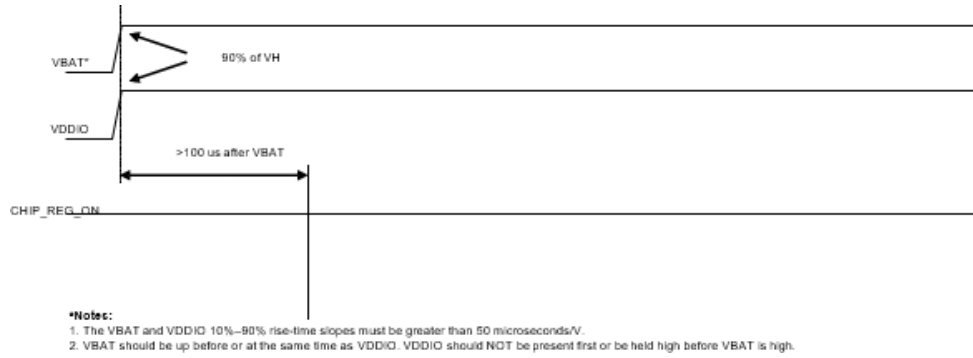


Figure 24. WLAN = OFF, Bluetooth = ON

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 6. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

### 6.1. Crystal Interface and Clock Generation

The SRW1500 Series can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 25. Consult the reference schematics for the latest configuration.

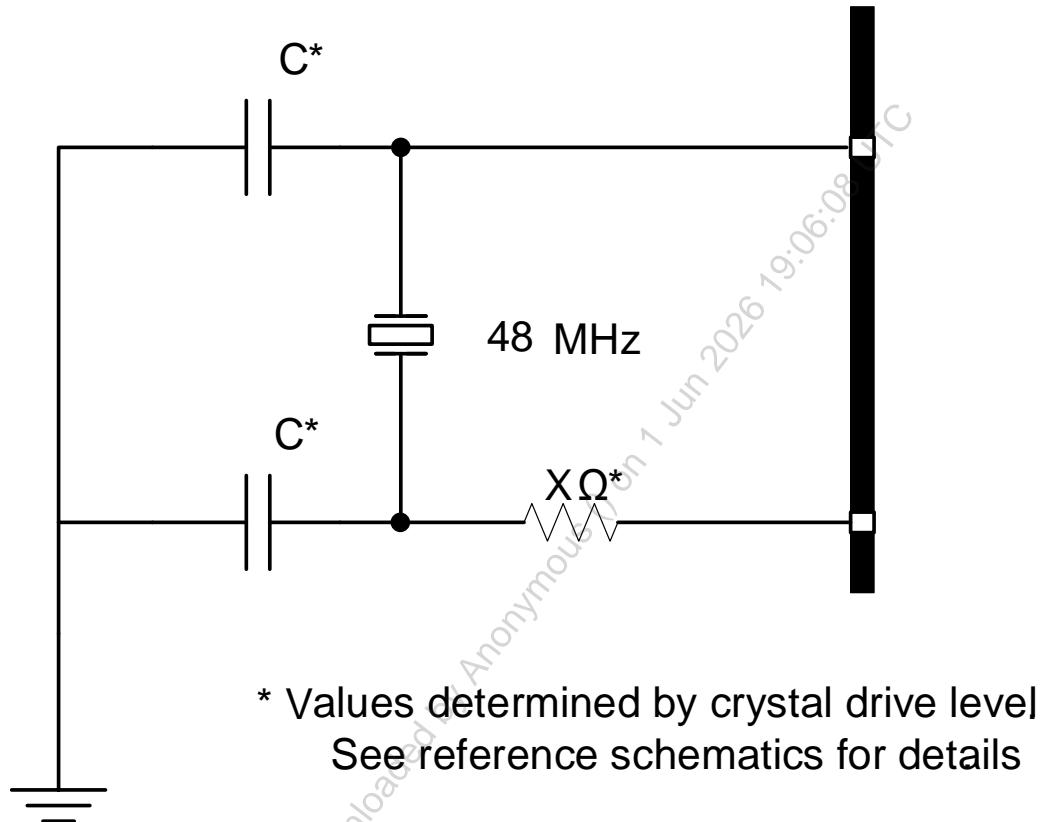


Figure 25. Recommended oscillator configuration

A fractional-N synthesizer in the SRW1500 Series generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 48 MHz crystal. The signal characteristics for the crystal oscillator interface are provided in Table 38. Crystal oscillator requirements.

Table 38. Crystal oscillator requirements

Parameter	Conditions/Note	Crystal			Unit
		Min.	Typ.	Max.	
Frequency	2.4 GHz and 5 GHz bands: IEEE 802.11ax operation, SDIO WLAN interface	–	48	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature <sup>1</sup>	Without trimming	–20	–	20	ppm
Crystal load capacitance	–	–	10	–	pF
ESR	–	–	–	60	$\Omega$
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	$\mu$ W

1.The equipment designer is responsible for selecting oscillator components that comply with these specifications.

## 6.2. External 32.768 kHz Low-Power Oscillator

The SRW1500 Series uses a secondary low-frequency clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ( $\pm 30\%$ ) over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power-save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock, which meets the requirements listed below.

Table 39. External 32.768 kHz sleep clock specifications

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	$\pm 200$	ppm
Duty cycle	30–70	%
Input signal amplitude	200–1800	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance	>100k	$\Omega$
	<5	pF

## 7. Security

The device implements a multi-processor security architecture built around a dedicated Secure Island Processor (SynaPROT Root of Trust), providing the foundation for secure operations.

### 7.1. Core Security Features

Table 40. Core Security Features

Feature	Description
Processing Cores	Secure Island (SynaPROT RoT); MCU (Arm® Cortex®-M52); WLAN Processor (Arm® Cortex®-R4); Bluetooth Processor (Arm® Cortex®-M4)
Power-On Root of Trust	Secure Island powers on first and executes immutable ROM-based RoT code
SPK Authentication	Secure Processor Kernel (SPK) authenticated and loaded using ECC digital signature verification
MCU Boot Validation	MCU boot loader image authenticated prior to releasing control to the MCU domain
MCU Subsystem Bring-Up Control	MCU initiates controlled bring-up of WLAN and Bluetooth subsystems following authentication
Wireless Secure Boot	Each subsystem includes its own ROM-based boot loader and enforces secure boot validation with assistance from Secure Island
Image Authentication Engines	All image authentication uses tamper-proof hardware-accelerated AES and ECC engines located in the Secure Island
Firmware Encryption & Verification	WLAN and Bluetooth firmware images encrypted and verified prior to execution
Anti-Rollback Protection	Firmware downgrade prevention mechanisms
Certificate Control	Certificate invalidation mechanisms supported
Memory Isolation	TrustZone Controller (TZC) for WLAN; Memory and Peripheral Protection Controllers (MPC/PPC) for Bluetooth
Hardware-Anchored Chain of Trust	Trust model spanning Secure Island, MCU, WLAN, and Bluetooth domains from power-on reset through subsystem firmware validation

## 8. MCU Subsystem

The SRW1500 Series is a member of the Synaptics family of chips targeting IoT applications. It is designed for customers seeking to reduce system costs associated with IC manufacturing, assembly, and bill of materials (BOM).

The device integrates an on-chip Arm® Cortex®-M52 CPU to run application software, along with an embedded hardware cryptographic accelerator to meet system security requirements. This chip family supports both on-chip host and off-chip host operating models.

The MCU subsystem consists of multiple components, including a dedicated Security Island (SynaPROT) that is responsible for key storage and security services for the rest of the system. The MCU subsystem also includes a cryptographic accelerator, on-chip memory, and OTP storage.

The MCU subsystem includes a rich set of peripherals and accelerators:

- 1 – USB 2.0 dual-role up to 480 Mb/s (LS/FS/HS)
- 2 – UARTs with flow control
- 1 – UARTs for debug
- 1 – I<sup>2</sup>C Host
- 1 – I<sup>2</sup>C Target
- 1 – SPI Host supports up to 25 MHz
- 1 – SPI Target up to 25 MHz
- 6 – PWMs supporting Motor Control & LED Brightness features
- 1 – PDM interface support 2 Digital Mics
- 1 – I2S with simultaneous RX/TX
- 32 MCU GPIOs – (Approx. 13 dedicated, other pinmuxed in SoC for debug and development modes)
- SDIO
- ADC: 8-channel general-purpose ADC (can be converted to GPIO if ADC channels are not used)
- General-purpose DAC
- Test and Development Interfaces
  - JTAG
  - ATE Debug support
  - ARM-DAP

## 8.1. M52 Subsystem

The SRW1500 Series MCU subsystem is built around an Arm® Cortex®-M52 processor and is optimized for high-performance embedded processing, system integration, and edge AI workloads. Based on the Armv8.1-M Mainline architecture, the Cortex-M52 supports the M-profile Vector Extension (MVE, also known as Helium), enabling efficient acceleration of digital signal processing and machine learning workloads.

The subsystem integrates a scalable memory architecture, high-throughput DMA engines, and a rich set of peripherals, enabling efficient data movement and real-time processing across the system.

The Cortex-M52 operates up to 240 MHz and supports dynamic frequency scaling to optimize performance and power consumption based on application requirements.

The MCU is tightly integrated with system-level resources, including:

- Arm-based interconnect fabric for efficient communication across subsystems
- Multi-channel DMA-230 and DMA-350 controllers for high-bandwidth data transfers
- 1 MB on-chip SRAM and system ROM supporting flexible application deployment

The subsystem supports advanced system capabilities, including:

- Execute-in-place (XIP) via Octal SPI, enabling extended code space beyond internal memory
- Encrypted external flash support, with secure key management handled by the SynaPROT security island
- Dedicated cryptographic hardware accelerators (AES, TDES, SHA, MD5) for secure applications

The SRW1500 Series is designed for intelligent edge processing and integrates AI acceleration through an embedded NPU, enabling efficient execution of machine learning workloads. Additional hardware offload engines, including checksum acceleration, further reduce CPU load and improve system efficiency.

The MCU subsystem also supports:

- M-profile Vector Extension (MVE / Helium) for SIMD acceleration of DSP and machine learning workloads
- Functional safety features aligned with IEC 60730 Class B requirements, enabling system-level self-test and diagnostic capabilities

A comprehensive peripheral set supports diverse application needs, including GPIO, PWM, capture (CAP), I<sup>2</sup>S, I<sup>2</sup>C, ADC, DAC, UART, PDM, and SPI interfaces. The MCU supports flexible boot options, including Flash, USB 2.0, SDIO, SPI, I<sup>2</sup>C, and UART, enabling adaptable system architectures for both standalone and host-assisted designs.

## 8.2. NPU

The Neural Processing Unit (NPU) improves the inference performance of neural networks. The NPU targets 8-bit and 16-bit integer quantized Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN). The NPU supports 8-bit weights.

The NPU includes a Direct Memory Access (DMA) controller that can read and write to external memory. When the NPU performs inferences, the DMA controller reads the neural network description. This description contains:

- The command stream
- Network weights
- Bias information
- Scale information

The DMA controller also transfers the Input Feature Maps (IFMs) and Output Feature Maps (OFMs) and NPU-private intermediate data that is also held in system memory.

## 8.3. SynaPROT

SynaPROT is responsible for the root of trust and secure boot. It includes a security engine and secure OTP. Dedicated cryptographic accelerators are present within SynaPROT; access to these engines is restricted from the rest of the system. The application core has its own dedicated cryptographic engines. SynaPROT provides secure storage and various cryptographic services, such as signature verification, to the MCU core. A secure, command mailbox-based mechanism is supported for interaction between SynaPROT and the application core.

SynaPROT is the custodian of symmetric and asymmetric keys. Flash decryption is accessible only to SynaPROT, and the decryption key is installed as part of the boot process, thereby limiting exposure to the rest of the system. When the device is in a secure state, JTAG is disabled; JTAG can be enabled only through authentication.

SynaPROT supports the following functions:

- On-chip 32Kbit anti-fuse OTP
- True random number generator
- DRM engine supports
  - AES, DES, 3DES, SHA1/SHA2/MD5, RSA, ECC

## 8.4. OTP

The OTP provides a 32-bit-wide bus interface for read operations and a 1-bit-wide bus interface for programming. Each bit is a one-way field in the Kilopass OTP; only a logic '1' can be programmed, and programming a '0' is not supported. The purpose of write password protection is to ensure that only authenticated users or firmware can program the OTP and to prevent accidental programming. This password protection applies to all OTP fields. Before programming any OTP field, the user must provide a 128-bit password to a password verification module. OTP programming is allowed only after successful password verification.

OTP provides permanent on-chip storage for configuration data and security keys. The SRW1500 Series supports 32 Kbits of OTP, of which 16 Kbits are designated as secure. Secure OTP is accessible only to SynaPROT, while non-secure OTP is accessible to all on-chip processors.

A 256-byte region of secure OTP is reserved for OEM use. In addition, 512 bytes of OTP space are allocated in the non-secure OTP region.

## 8.5. Interfaces Summary

SRW1500 Series supports a rich set of interfaces suitable for diverse application needs.

Table 41. SRW1500 Series MCU Interface Functional and Electrical Summary

Interface	Instances	Role	Functional Features	Performance / Resolution	DMA	Reset/ Special Notes
GPIO	32	Input / Output	Programmable direction; pin multiplexing; alternate signal mapping	—	—	Tri-stated after reset; configurable pull and mux
SPI	1 Host + 1 Target	Host / Target	Motorola SPI, TI SSP, Microwire compatible; programmable clock phase/ polarity	Up to 25 MHz	Yes	Full duplex
I <sup>2</sup> C	1 Host + 1 Target	Host / Target	7-bit / 10-bit addressing; bulk transmit; Ultra-Fast mode	Standard ( $\leq 100$ kb/s); Fast ( $\leq 400$ kb/s); Fast+ ( $\leq 1$ Mb/s); High-Speed ( $\leq 3.4$ Mb/s)	Yes	Open-drain interface
UART	3	Serial	16550-compatible; configurable character length; parity; stop bits; false start detect; prioritized interrupts	Programmable baud (fractional divider); 5–8 data bits; 9-bit mode; RTS/CTS flow control	Yes	DMA signaling modes supported

Interface	Instances	Role	Functional Features	Performance / Resolution	DMA	Reset/ Special Notes
PDM	1	Audio Input	Supports up to 2 digital microphones (L/R pair); HW decimation filters	Input clock: 512 kHz–3.072 MHz; Output rate: 8 kHz–192 kHz; 16-bit samples	Yes	Direct RAM transfer via DMA
PWM (TCPWM)	Up to 6 counters	Timer / Control	Timer, Capture, Quadrature decode, PWM, BLDC motor control, Pseudo-random PWM, Shift register	16-bit or 32-bit counters; Prescaler $\pm 1-128$ ; Up/Down/ Up-Down modes	–	Suitable for motor and precision timing control
I2S	1	Host / Target	Philips I2S, Sony, Right-Justified, Left-Justified, PCM, TDM modes; programmable polarity and frame length	Programmable sample size and sample rate; MSB/LSB selectable; Left/Right order programmable	Yes	Shared SCK/ WS support
ADC	1	Analog Input	SAR architecture; internal calibration; CPU-configured, autonomous operation	12-bit resolution; Up to 1.536 Msps; 8-channel input MUX	–	External analog inputs
DAC	1	Analog Output	Single conversion; Continuous conversion via DMA; Comparator mode	10-bit resolution	Yes	Voltage output; threshold interrupt support
SDIO	1	Host	SDIO v3.0; interrupt remap to GPIO; strap-enabled mode	DS (25 MHz); SDR12 (25 MHz); SDR25 (50 MHz); SDR50 (100 MHz); SDR104 (150 MHz); DDR50 (50 MHz)	Yes	Backward compatible with SDIO v2.0
USB 2.0	1	Dual-Role Device (DRD)	USB 2.0 OTG compliant; integrated PHY; self-calibrated termination	HS (480 Mb/s); FS (12 Mb/s); LS (1.5 Mb/s)	Yes	Supports 24/20 MHz crystal or internal PLL

## 8.6. Boot Option

The SRW1500 Series MCU subsystem supports boot from the following interfaces:

- Flash
- SDIO
- USB2.0
- SPI
- UART

Boot option is selectable using bootstrapping pins.

Table 42. Boot option

Pin	Strap Name	Description	Default Pull
MCU GPIO {30:31}	BOOT	Boot strap to indicate which source needs to be used to load the software and M52 code 00: Boot from USB 01: Boot from OSPI 10: Boot from SDIO 11: Boot from other (SPI,I <sup>2</sup> C,UART)	None
MCU_GPIO21	PLLBYPASS	Boot strap to indicate the PLL Bypass, so the boot ROM won't switch the clock to PLL but continue with RC oscillator clock	Pull Down
MCU_GPIO{4,3}	DAPSEL	Select DAP for M52 00 – Functional pin mux. 11 – MCU DAP selection	Pull Down

## 9. WLAN Global Functions and Interfaces

### 9.1. WLAN CPU and Memory Subsystem

The SRW1500 Series WLAN section includes an integrated Arm Cortex-R4 32-bit processor with internal RAM and ROM. The on-chip memory for the CPU includes 960 KB SRAM and 1408 KB ROM.

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 10. Bluetooth Subsystem

### 10.1. Overview

The SRW1500 Series integrates a Bluetooth 6.0 compliant 2.4 GHz transceiver with an embedded controller and processor subsystem. The Bluetooth subsystem includes RF, baseband, protocol stack execution, and firmware update support.

### 10.2. Bluetooth Subsystem Summary

Table 43. Bluetooth Subsystem Summary

Feature	Description
Bluetooth Standard	Bluetooth® 6.0
RF Band	2.4 GHz ISM band
Transmit Capability	Class 1 power amplifier with Class 2 capability
Controller Processor	Arm® Cortex®-M4 32-bit RISC core
Debug Support	Embedded ICE-RT debug and JTAG interface units
Protocol Stack Execution	Executes software from Link Control (LC) layer up to Host Controller Interface (HCI)
ROM	1024 KB (program storage and boot ROM)
System RAM	512 KB system-data RAM
Patch RAM	Supports firmware patching and configuration flexibility

### 10.3. Firmware and Patch Support

At power-up, the lower-layer Bluetooth protocol stack executes from internal ROM.

Patch RAM enables firmware updates for bug fixes, feature enhancements, or configuration variants. External patches may be downloaded from the host to the SRW1500 Series through UART transport.

## 11. Wi-Fi RF Specifications

### 11.1. Wi-Fi Introduction

The SRW1500 Series includes an integrated Tri-band direct conversion radio that supports the 2.4 GHz, 5 GHz and the 6 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz and 6 GHz radios.

Unless otherwise stated, limit values apply for the conditions specified in [Table 5](#) and [Table 6](#). Typical values apply for an ambient temperature +25°C.

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 11.2. 2.4 GHz Band General RF Specifications

Table 44. 2.4 GHz band general RF specifications

Item	Condition	Min.	Typ.	Max.	Unit
TX/RX switch time	Including TX ramp down	—	—	5	μs
RX/TX switch time	Including TX ramp up	—	—	2	μs
Power-up and power-down ramp time	DSSS/CCK modulations	—	—	< 2	μs

## 11.3. Wi-Fi 2.4 GHz Receiver Performance Specifications

**Note:** The values in the table below are specified at the chip port unless otherwise noted.

Table 45. Wi-Fi 2.4 GHz Receiver Performance Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	—	2400	—	2484	MHz
RX sensitivity IEEE 802.11b, 8% PER for 1024 octet PSDU	1 Mb/s DSSS	—	-98.6	—	dBm
RX sensitivity IEEE 802.11g, 10% PER for 1024 octet PSDU	54 Mb/s OFDM	—	-76.3	—	dBm
RX sensitivity IEEE 802.11n HT20, LDPC 10% PER for 4096 octet PSDU. Defined for default parameters: MM, 800 ns GI and non-STBC.	MCS7	—	-76.7	—	dBm
RX sensitivity IEEE 802.11be 10% PER for 4096 octet PSDU. CP/LTF = 0.8 μs + 2 × LTF non-STBC	MCS0	—	-94.1	—	dBm
	MCS9	—	-71.0	—	dBm
RX sensitivity IEEE 802.11ax 10% PER for 4096 octet PSDU. CP/LTF = 0.8 μs + 2 × LTF non-STBC	MCS0	—	-94.1	—	dBm
	MCS9	—	-71.0	—	dBm
26 resource units (RU 26): RX sensitivity IEEE 802.11ax 10% PER for 4096 octet PSDU. CP/LTF = 0.8 μs + 2 × LTF, LDPC, non-STBC	MCS0	—	-93.9	—	dBm
	MCS9	—	-70.0	—	dBm

Parameter	Conditions	Minimum	Typical	Maximum	Unit
52 resource units (RU 52): RX sensitivity IEEE 802.11ax 10% PER for 4096 octet PSDU. CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC	MCS0	—	-93.9	—	dBm
	MCS9	—	-69.8	—	dBm

## 11.4. Wi-Fi 2.4 GHz Transmitter Performance Specifications

**Note:** The values shown below are specified at the chip port unless otherwise indicated.

Table 46. Wi-Fi 2.4 GHz Transmitter Performance Specifications

Parameter	Conditions		Minimum	Typical	Maximum	Unit
Frequency range	—		2400	—	2484	MHz
—	Modulation	EVM max.	—	—	—	—
—	802.11b	-9 dB	—	22	—	dBm
—	(DSSS/ CCK)					
TX power for highest power level setting	OFDM, BPSK		-8 dB	—	22	dBm
	OFDM, 16-QAM		-19 dB	—	21.5	dBm
at 25°C with spectral mask and EVM compliance	OFDM, 64-QAM (R = 5/6)		-27 dB	—	19.5	dBm

## 11.5. Wi-Fi 5 GHz/6 GHz Receiver Performance Specifications

**Note:** The values shown below are specified at the chip port unless otherwise noted.

Table 47. Wi-Fi 5 GHz/6 GHz Receiver Performance Specifications

Parameter	Conditions		Minimum	Typical	Maximum	Unit
Frequency range	—		4900	—	7125	MHz
RX sensitivity IEEE 802.11a, 20 MHz, single RF chain	6 Mb/s OFDM	—	—	-93.9	—	dBm
RX sensitivity IEEE 802.11n HT20, LDPC, 10% PER for 4096 octet PSDU. Defined for default parameters: MM, 800 ns GI and non-STBC.	MCS0	—	—	-94	—	dBm
	MCS7	—	—	-76.5	—	dBm
	MCS0	—	—	-94	—	dBm

Parameter	Conditions		Minimum	Typical	Maximum	Unit
RX sensitivity IEEE 802.11ac VHT20, LDPC, 10% PER for 4096 octet PSDU. Defined for default parameters: 800 ns GI and non-STBC.	MCS9	—	—	-69.2	—	dBm
RX sensitivity IEEE 802.11ax, full BW mode, 10% PER for 4096 octet PSDU. CP/LTF = $0.8 \mu\text{s} + 2 \times \text{LTF}$ non-STBC, for 20 MHz BW.	MCS0	—	—	-94	—	dBm
	MCS9	—	—	-70.2	—	dBm
RX sensitivity IEEE 802.11be, full BW mode, 10% PER for 4096 octet PSDU. CP/LTF = $0.8 \mu\text{s} + 2 \times \text{LTF}$ non-STBC, for 20 MHz BW.	MCS0	—	—	-94	—	dBm
	MCS9	—	—	-70.2	—	dBm
26 resource units (RU 26): RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU), CP/ LTF = $0.8 \mu\text{s} + 2 \times \text{LTF}$ , LDPC, non-STBC, and 20 MHz BW	MCS0	—	—	-93.2	—	dBm
	MCS9	—	—	-68.9	—	dBm
52 resource units (RU 52): RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU), CP/ LTF = $0.8 \mu\text{s} + 2 \times \text{LTF}$ , LDPC, non-STBC, and 20 MHz BW	MCS0	—	—	-93.7	—	dBm
	MCS9	—	—	-70.3	—	dBm
106 resource units (RU 106): RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU), CP/LTF = $0.8 \mu\text{s} + 2 \times \text{LTF}$ , LDPC, non-STBC, and 20 MHz BW	MCS0	—	—	-93.8	—	dBm
	MCS9	—	—	-70.1	—	dBm

## 11.6. Wi-Fi 5 GHz/6 GHz Transmitter Performance Specifications

**Note:** The values are specified below at the chip port, unless otherwise indicated.

Table 48. Wi-Fi 5 GHz/6 GHz transmitter performance specifications

Parameter	Conditions		Minimum	Typical	Maximum	Unit
Frequency range	—		4900	—	7125	MHz
	—	EVM does not exceed	—	—	—	—
TX power for highest power level setting at 25 °C with spectral mask and EVM compliance	OFDM, BPSK	-13 dB	—	20	—	dBm
	OFDM, 256-QAM (R = 5/6)	-32 dB	—	16	—	dBm

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 12. Bluetooth RF Specifications

**Note:** Values in this datasheet are design goals and are subject to change based on device characterization results.

Unless otherwise stated, limit values apply for the conditions specified in Table 6. Typical values apply for these conditions:

- VBAT = 3.6 V
- Ambient temperature +25 °C

Table 49. Bluetooth receiver RF specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>General</b>					
Frequency range	—	2402	—	2480	MHz
Receive sensitivity: LELR, BLE, and LE2 with dirty transmit off.	125 kbps, LELR, 30.8% PER	—	-109.5	—	dBm
	500 kbps, LELR, 30.8% PER	—	-104	—	dBm
	1 Mb/s, BLE, 30.8% PER	—	-100.5	—	dBm
	2 Mb/s, LE2, 30.8% PER	—	-97.5	—	dBm
Input IP3 (max. LNA gain)	—	-12	—	—	dBm
Maximum input at chip port	For successful reception	-17	—	—	dBm
	Without damaging the chip	—	—	+13	dBm

**Notes:**

- The maximum value represents the actual Bluetooth specification required for qualification as defined in the version 6.0 specification.
- The Bluetooth sensitivity levels for 1 Mb/s, 2 Mb/s, and 3 Mb/s operation are:
  - 93.5 dBm (MSLE on), -93 dBm, and -87.5 dBm, respectively, in the presence of the blockers indicated.
- Interferer: 2570 MHz, BW = 20 MHz, measured at 2480 MHz.
- Interferer: 2555 MHz, BW = 20 MHz, measured at 2480 MHz.

**Note:** The specifications in Table 50 are measured at the Bluetooth chip port output, unless otherwise defined.

Table 50. Bluetooth transmitter RF specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	—	2402	—	2480	MHz
TX output power requirements in BT normal power mode	BLE	—	11	—	dBm
	LE2	—	11	—	dBm
	LELR	—	11	—	dBm
TX output power requirements in BT high-power mode: TX power at chip output that meets Bluetooth Test Specification RF.TS.4.0.0 ACP/EVM requirements.	BLE, GFSK	—	20	—	dBm
	LE2, GFSK	—	20	—	dBm
	LELR, GFSK	—	20	—	dBm

**Notes:**

- Unless otherwise indicated, this applies to BT nominal TX and BT HP TX.
- The typical number is measured at ± 3 MHz offset.
- Applicable to BT nominal TX and BT HP TX.
- Transmitted power in cellular and FM bands at the antenna port.

Downloaded by Anonymous (on 1 Jun 2026 19:05:08 UTC)

Table 51. Local oscillator performance

Parameter	Minimum	Typical	Maximum	Unit
<b>LO Performance</b>				
Lock time	—	72	—	μs
Initial carrier frequency tolerance	—	±25	—	kHz
<b>Frequency Drift 1</b>				
DH1 packet	—	±8	±25	kHz
DH3 packet	—	±8	±40	kHz
DH5 packet	—	±8	±40	kHz
Drift rate	—	5	20	kHz/50 μs
<b>Frequency Deviation</b>				
00001111 sequence in payload2	140	155	175	kHz
10101010 sequence in payload3	115	140	—	kHz
Channel spacing	—	—	—	MHz

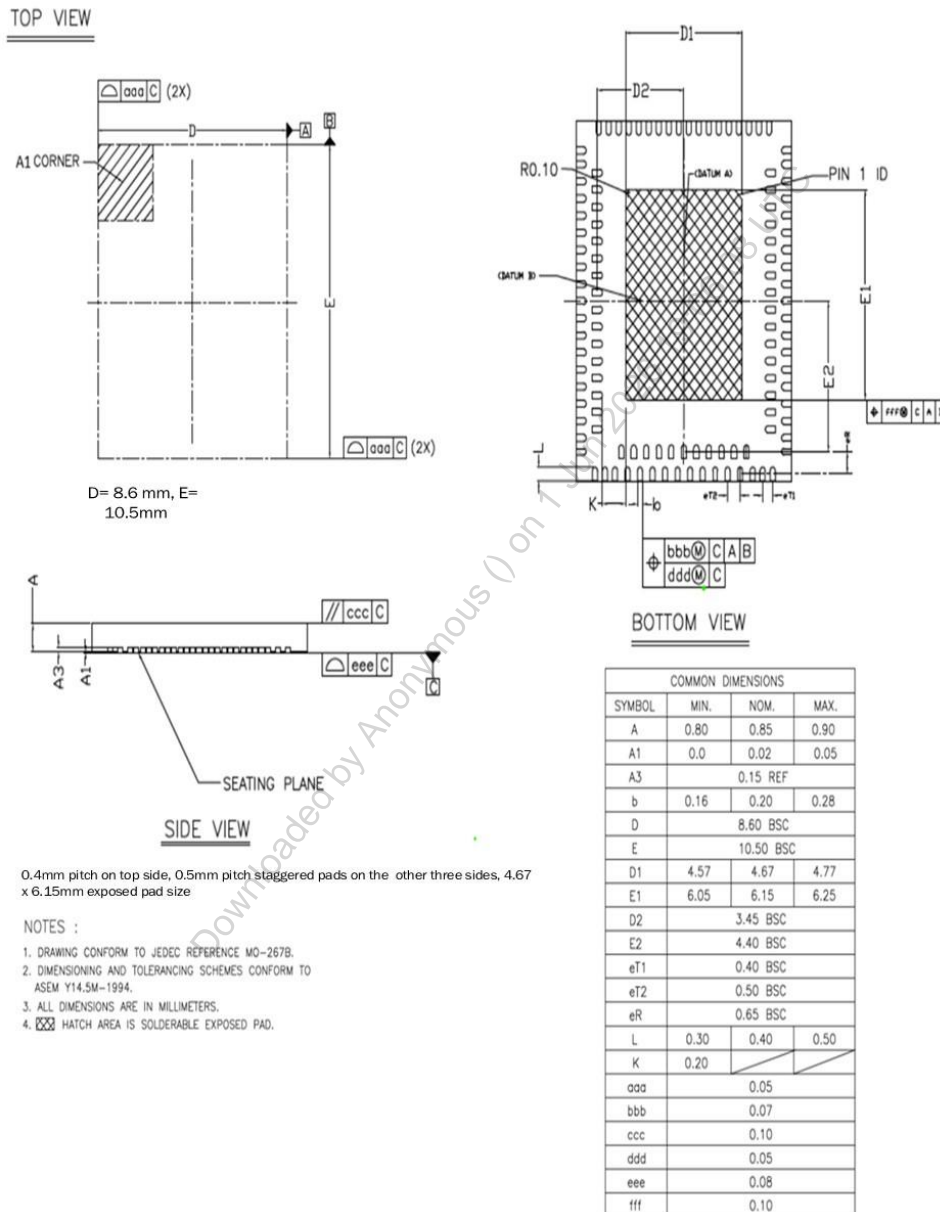
**Notes:**

- Applicable to BT nominal TX and BT HP TX.
- This pattern represents an average deviation in payload.
- Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

### 13. Package Information

The SRW1500 Series device is housed in an 8.6 × 10.5 × 0.9 mm, 115-lead DR-QFN package. The package features a single row of pads on a 0.4 mm pitch on one side, and staggered pads on a 0.5 mm pitch on the remaining three sides.

The figure below shows the package outline drawing, including the 4.67 × 6.15 mm exposed pad, which must be connected to the PCB ground plane using short, dense bias to ensure proper thermal and electrical performance.



0.4mm pitch on top side, 0.5mm pitch staggered pads on the other three sides, 4.67 x 6.15mm exposed pad size

**NOTES :**

1. DRAWING CONFORM TO JEDEC REFERENCE MO-267B.
2. DIMENSIONING AND TOLERANCING SCHEMES CONFORM TO ASEMI Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. [Hatched Area] HATCH AREA IS SOLDERABLE EXPOSED PAD.

## 14. Package Thermal Characteristics

The information below is based on the following conditions:

- No heat sink. This is an estimate, based on a 4-layer PCB that conforms to EIA/ JESD51-7 (101.6 mm × 101.6 mm × 1.6 mm).
- Absolute junction temperature limits are maintained through active thermal monitoring or turning off one of the TX chains, or both.

Table 52. Package thermal characteristics

Characteristic	HPC WLBGA
$\theta_{JA}$ (°C/W) (value in still air)	18.193
$\theta_{JB}$ (°C/W)	4.688
$\theta_{JC}$ (°C/W)	9.402
$\Psi_{JT}$ (°C/W)	0.138

### 14.1. Junction Temperature Estimation and PsiJT versus ThetaJC

The package thermal characterization parameter PsiJT ( $\Psi_{JT}$ ) yields a better estimation of actual junction temperature ( $T_J$ ) than using the junction-to-case thermal resistance parameter ThetaJC ( $\theta_{JC}$ ). The reason for this is that  $\theta_{JC}$  assumes that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package.  $\Psi_{JT}$  considers the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

- $T_J$  = Junction temperature at steady-state condition (°C)
- $T_T$  = Package case top center temperature at steady-state condition (°C)
- $P$  = Device power dissipation (Watts)
- $\Psi_{JT}$  = Package thermal characteristics; no airflow (°C/W)

## 15. Ordering and Part Marking Information

Information for this section will be added when available.

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC

## 16. Revision History

Revision	Description
1	Initial release.
A	Initial public release.

Downloaded by Anonymous () on 1 Jun 2026 19:06:08 UTC



**Copyright**

Copyright © 2026 Synaptics Incorporated. All Rights Reserved.

**Trademarks**

Synaptics, the Synaptics logo, Astra, and the Astra logo are trademarks or registered trademarks of Synaptics Incorporated in the United States and/or other countries.

FreeRTOS is a trademark of Amazon.com, Inc. or its affiliates. Arm, Cortex, and Ethos are trademarks or registered trademarks of Arm Limited. Zephyr is a registered trademark of The Linux Foundation. FreeRTOS is a trademark of Amazon.com, Inc. or its affiliates. All other trademarks are the property of their respective owners.

**Contact Us**

Visit our website at [www.synaptics.com](http://www.synaptics.com) to locate the Synaptics office nearest you.

PN: 505-001567-01 Rev A

**Notice**

This document contains information that is proprietary to Synaptics Incorporated ("Synaptics"). The holder of this document shall treat all information contained herein as confidential, shall use the information only for its intended purpose, and shall not duplicate, disclose, or disseminate any of this information in any manner unless Synaptics has otherwise provided express, written permission.

Use of the materials may require a license of intellectual property from a third party or from Synaptics. This document conveys no express or implied licenses to any intellectual property rights belonging to Synaptics or any other party. Synaptics may, from time to time and at its sole option, update the information contained in this document without notice.

INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED "AS-IS," AND SYNAPTICS HEREBY DISCLAIMS ALL EXPRESS OR IMPLIED WARRANTIES, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND ANY WARRANTIES OF NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT SHALL SYNAPTICS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES ARISING OUT OF OR IN CONNECTION WITH THE USE OF THE INFORMATION CONTAINED IN THIS DOCUMENT, HOWEVER CAUSED AND BASED ON ANY THEORY OF LIABILITY, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, AND EVEN IF SYNAPTICS WAS ADVISED OF THE POSSIBILITY OF SUCH DAMAGE. IF A TRIBUNAL OF COMPETENT JURISDICTION DOES NOT PERMIT THE DISCLAIMER OF DIRECT DAMAGES OR ANY OTHER DAMAGES, SYNAPTICS' TOTAL CUMULATIVE LIABILITY TO ANY PARTY SHALL NOT EXCEED ONE HUNDRED U.S. DOLLARS.