SR80 Series Audio AI MCUs

Electrical Specification

Description

The Synaptics® Astra™ SR80 Series of Audio AI MCUs deliver industry-leading performance with ultra-low-power consumption, enabling the next generation of AI-enhanced, voice-driven, consumer and enterprise-grade IoT devices.

The AI MCUs combine an Arm® Cortex®-M33 MCU, Synaptics DSP cores, a Synaptics NPU, a Tensilica® HiFi 5 DSP, a built-in CODEC, high-speed USB, a rich set of I/O interfaces and advanced security features into a powerful platform designed for state-of-the-art wired and true-wireless (TWS) headsets, earbuds, voice-enabled smart-home devices, soundbars, and conferencing systems.

Turnkey AI-accelerated algorithms such as environmental noise cancellation (ENC) designed to exceed Microsoft® Teams™ version 5 Premium requirements, hybrid active noise cancellation (ANC), and speech and sound recognition, deliver natural, responsive voice experiences and human-machine interactions in real-world environments.

Open software and design collateral including the Astra SDK, audio performance tuning tools, reference designs, and evaluation hardware are supported on the SR80 Series to accelerate product development.

The SR80 Series gives product designers signal processing capability that far exceeds what is available today. An advanced **multi-core** audio processing engine provides a wealth of DSP resources to support advanced features. The NPU enables advanced AI features and support for TensorFlow™ Lite for Microcontrollers.

Additionally, a Tensilica HiFi 5 DSP, and an Arm® M33 processor complement the core signal processing engines. The Tensilica HiFi 5 DSP supports an Open-DSP platform for third party and customer application development. The Arm M33 core provides control and sensor fusion functions. The SR80 Series provides secure boot, secure firmware updates, secure debugging, user, and sensor data protection by utilizing integrated device identification, authentication, secure memory partitioning, and encryption functionality.

The integrated audio codec provides high performance, stereo (two) digital-to-analog converters (DACs), four analog-to-digital converters (ADCs), and eight digital microphones (DMIC) inputs.

High-performance class-AB/G headphone amplifiers complement the high dynamic range DACs for high fidelity playback (110 dB dynamic range).

Advanced continuous time delta-sigma ADCs paired with cap-less differential input amplifiers offer 106 dB of dynamic range for analog mic inputs for demanding applications.

The SR80 Series interfaces include USB 2.0 high-speed interface, three I2S, I3C host/target, two I^{2}C hosts, one I^{2}C target, three UART, two SPI host, one QSPI host/SPI target, PWM LED, 31 GPIOs, one 10-bit Monitor ADC, and JTAG debug.

A comprehensive set of software development and tuning tools, reference designs, and evaluation hardware is available to guide product development.

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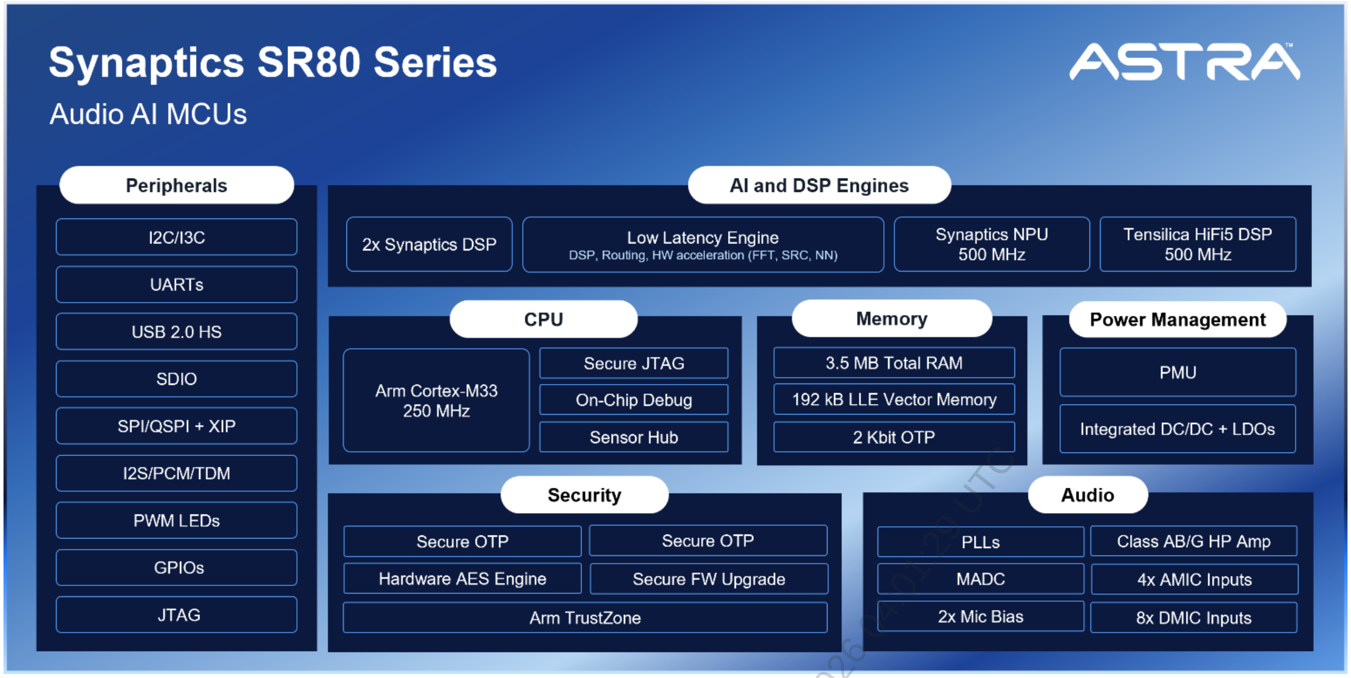


Figure 1. SR80 Series block diagram

2. Features

- **Processors:** Arm Cortex-M33 CPU, HiFi 5 DSP, Synaptics dual CAPE 2 DSP, Synaptics LLE for ANC, and Synaptics NPU
- **Processing Subsystems**
  - Arm Cortex-M33 CPU: up to 250 MHz
  - HiFi 5 DSP (32-bit audio DSP supporting floating-point and fixed-point operations), up to 500 MHz
  - Synaptics low-power DSP subsystem
    - 2× CAPE 2 DSPs (32-bit IEEE floating-point + fixed-point)
    - Low Latency Engine (LLE) for ANC
    - Up to 250 MHz
  - Synaptics NPU: Up to 500 MHz
- **Memory**
  - 3.5 MB total memory
- **Security**
  - Hardware security features
    - Arm® TrustZone®
    - Device Identification and authentication
    - Secure / non-secure memory partitioning
    - Secure boot, firmware updates, and debugging
    - Hardware AES engine
    - OTP for key storage

    Advanced encryption standard (AES) for encryption, decryption
- **Audio Processing**
  - Active Noise Cancellation
    - Ultra-low latency
    - Flexible mixing of anti-noise, ambient fusion, and playback signals
    - Support for multiple form factors/designs
    - Easy to use tuning tool
    - Supervisory controls
    - User adaptive
    - Environment adaptive
  - Voice Processing
    - Voice capture noise reduction optimized for all major electronic devices (high-performance doorbells, intercoms, security cameras, and panels)
  - High performance, low-power audio
    - Stereo 110 dBA dynamic range class-AB/G headphone amplifiers
    - Four 105 dBA differential microphone inputs
- **Power Management / Charging Interfaces**
  - One-wire PLC Communication

- **Connectivity Interfaces**
    - 3× Inter-IC Sound (I2S) / pulse-code modulation (PCM) / time division multiplexed (TDM) interfaces
    - USB 2.0 high-speed interface
    - One SD/SDIO-SDR50 support up to 100 MHz
    - One QSPI host interface (supports program execution from external flash memory), SPI target
    - Two Serial Peripheral Interface (SPI) hosts
    - Three I2C: two host interfaces and one target interface
    - I3C® interface supports host or target operation (MIPI improved inter-integrated circuit bus with a two-wire, sensor interface)
- **Debug**
    - Joint Test Action Group (JTAG) for debug
    - Three (3) Universal asynchronous receiver/transmitter (UART) for debug
- **Packaging**
    - 76-balls WLCSP, 0.35 mm pitch, 3.082 mm x 3.20 mm
    - 76-balls LGA, 6.00 mm x 6.50 mm

Table 1. SR80 Series Product Families Feature Summary

PRODUCT FAMILY / FEATURES	SR82 	SR85 	SR88 
MCU-Cortex-M33, DSP-CAPE2, LLE	Yes	Yes	Yes
HiFi5	No	Yes	Yes
NPU	No	No	Yes
Grade & Package			
Package	WLCS-76 / LGA-76		
Consumer	Yes (TA: 0 to +70 ˚C / TJ: -40 to +85 ˚C)		

2.1. Overview

The SR80 Series device combines a low-power, secure, Arm Cortex-M33 32-bit microcontroller unit (MCU), an industry standard Tensilica® HiFi 5 32-bit DSP supporting both fixed-point and floating-point operations, a Synaptics low-power DSP subsystem, Synaptics NPU, industry standard interfaces, generous memory, and advanced algorithms into a powerful platform for advanced noise cancelling devices.

System-level AI compute performance is achieved through a combination of the NPU, CAPE2 DSPs, and LLE, with aggregate throughput dependent on workload distribution across these processing engines.

2.1.1. Analog Subsystem

The analog subsystem provides low-power, high-performance ADCs, DACs, amplifiers, and other functions.

Microphone path:

- Four ADCs for analog inputs
- Dynamic Range: 105 dB(A)
- THD+N: -90 dB @ -1 dBFS
- Differential cap-less inputs
- Analog PGA with 0, 6, 12 dB gain
- Additional digital gain (boost)
- Two microphone bias voltage outputs, up to 3.0 V, 5 mA current capability
  - Independently programmable (100 mV steps)
  - Bypass mode outputs 1.8 V mic bias
- Four PDM interfaces for up to eight digital microphones

Analog playback Path:

- Two DACs
- High-performance stereo Class-AB/G differential headphone amplifier
- 30 mW/32 Ohms
- Dynamic Range: 110 dB(A)
- THD+N: -95 dB @ -1 dBFS

2.1.2. Arm M33 CPU Subsystem

A secure, single core, 32-bit Arm M33 based SSE200 sub-system provides system and sensor management and other functions.

Hardware features:

- Arm Cortex-M33 Processor, up to 250 MHz
  - DSP/single instruction, multiple data (SIMD)
  - Single precision floating-point unit (FPU)
- 128 KB SRAM
- 16 KB I-Cache
- 16 kB D-Cache
- 96 KB ROM
- 64 KB I-TCM
- 64 KB D-TCM
- 64-bit wide AXI bus matrix
- QSPI flash controller

- Built-in system security
    - Secure boot and Secure firmware upgrade
    - Device identification and authentication
    - Data security for local storage and data over the network
    - Secure JTAG debugging
    - AES-128/256: advanced encryption standard
- Timer/counter/watchdog
- On-chip debug

Software features:

- System control
- Boot-up host
- Firmware update
- Communication with Bluetooth® subsystem
- Sensor hub
- SDK for third party development

2.1.3. HiFi 5 DSP Subsystem

A dedicated Tensilica HiFi 5 DSP plus memory subsystem handles customer and third-party algorithms.

The HiFi 5 DSP high-performance core is part of the Tensilica HiFi DSP family for audio, voice, and speech, offering low-energy, high-performance processing for audio and voice algorithms.

Hardware features:

- Tensilica HiFi 5 processor, up to 500 MHz
- 32-bit fixed-point and floating-point support
- 1 MB local RAM, plus additional 1.5 MB shared RAM (total 2.5 MB accessible memory)
- TCM
    - 64 KB instruction
    - 128 KB data
- Cache
    - 32 KB instruction
    - 32 KB data
    - Prefetch
- On-chip debug (OCD)
- Configurable interrupt controller external to the core

Software features:

- Fully open platform for customer use (SDK available)
- FreeRTOS™
- Software API to the rest of the SR80 Series chip
- Control interface to applications running on other processors
- Control interface to hardware configuration
- Configurable audio routing to/from other points in the SR80 Series system

2.1.4. Synaptics DSP Subsystem

The Synaptics DSP Subsystem includes dual CAPE 2 cores and a low-latency engine (LLE) for ANC.

Hardware features:

- Dual CAPE 2 DSPs, up to 250 MHz
- 32-bit IEEE floating-point and 32-bit fixed-point
- Dual multiply/add + dual load/store + dual index update, all in one cycle
- Two floating point MACs per cycle
- Two 32-bit, four 16-bit, or eight 8-bit fixed-point multiply-accumulate operations (MACs) per cycle
- Program cache
- Low latency engine for ANC
    - Extension to architecture
    - Complex vector arithmetic
    - Fast Fourier transform (FFT) acceleration
    - Bi-quad filter acceleration
    - Sample rate conversion (SRC) (power of 2) acceleration
    - 24 bit, 8 bit, and ternary neural network acceleration

Software features:

- Environmental noise cancellation (ENC)
- Active Noise Cancellation (ANC)
- Acoustic echo cancellation (AEC)
- Voice wake-up/voice trigger
- Sample rate conversion
- Equalizer (EQ)
- Dynamic range control
- Neural networks

2.1.5. Synaptics NPU

Synaptics easy to use and highly optimized AI Neural Network acceleration processor working seamlessly with HiFi5 DSP supporting TensorFlow Lite for Microcontrollers (TFLM), for advanced voice and audio applications.

- 500 MHz maximum core speed
- 32 (8x8 and 16x8) MACs
- 75% average MAC usage
- 32 @ 500 MHz GOPS
- 32 kB local buffer and flexible allocation of low-latency shared memory

2.1.6. Interfaces

A generous offering of general-purpose input/output (GPIO) and industry standard interfaces makes connecting to external memories, sensors, SoCs, buttons, and indicators easy.

- USB 2.0 high-speed interface
- Three I2S/PCM/TDM host/target interfaces
- Two I^{2}C host interfaces
- One I^{2}C target interface (or I3C host/target)
- JTAG debug interface
- Three UART interfaces
- One QSPI host/SPI target interface
- Two SPI host interfaces
- 32 GPIOs

2.1.7. Timers

The system has multiple counter/timers that provide periodic triggers, count incoming events, or provide watchdog capability for system robustness.

2.1.8. Measurement ADC

A 10-bit measurement ADC (MADC) can be used for multi-button sensing, or for general-purpose monitoring of system voltages.

2.1.9. Power Management Unit

A dedicated power management unit (PMU) manages the multiple power domains and primary power states within the SR80 Series. The PMU provides controls for firmware to further manage power states and generate interrupts from wake events.

3. Pin Information

3.1. Pin Definitions

Table 2. Pin type and direction abbreviations

Abbreviation	Definition
Type	
A	Analog
D	Digital
OD	Open Drain
Diff	Differential (analog)
P	Power
GND	Ground
Direction	
In	Input only
Out	Output only
In/Out	Input and output

Table 3. Signal definitions

Signal	Ball	Pad	Type, Direction	Description
I2S/PCM Interfaces				
I2S0_PCM_BCLK	E15	59	D, IN/OUT	I2S0 bit clock
I2S0_PCM_WS	C11	60	D, IN/OUT	I2S0 word select
I2S0_PCM_TX_DAT	B14	54	D, OUT	I2S0 TX data
I2S0_PCM_RX_DAT	B12	56	D, IN	I2S0 RX data
I2S1_RX_DAT	K16	39	D, IN	I2S1 RX data
I2S1_WS	K14	41	D, IN/OUT	I2S1 word select
I2S1_TX_DAT	F14	43	D, OUT	I2S1 TX data
I2S1_BCLK	G15	47	D, IN/OUT	I2S1 bit clock
I2S1_RX_DAT_b	J13	37	D, IN	I2S1 RX data (alternate pin)
I2S1_TX_DAT_b	J15	38	D, OUT	I2S1 TX data (alternate pin)
I2S2_BCLK	G11	29	D, IN/OUT	I2S2 bit clock
I2S2_WS	J11	31	D, IN/OUT	I2S2 word select
I2S2_TX_DAT	K12	33	D, OUT	I2S2 TX data
I2S2_RX_DAT	K10	35	D, IN	I2S2 RX data
I2S2_BCLK_b	H10	25	D, IN/OUT	I2S2 bit clock (alternate pin)
I2S2_WS_b	J9	27	D, IN/OUT	I2S2 word select (alternate pin)
I2S2_TX_DAT_b	G9	32	D, OUT	I2S2 TX data (alternate pin)
I2S2_RX_DAT_b	H8	34	D, IN	I2S2 RX data (alternate pin)

Signal	Ball	Pad	Type, Direction	Description
I^{2}C Target, I^{2}C Host/Target, I3C Host/Target				
I2C_SLV_SCL/I3C_SCL	D12	50	OD, I/O	I2C target clock I3C host/target clock
I2C_SLV_SDA/I3C_SDA	C13	48	OD, I/O	I2C target data I3C host/target data
I3C_SCL_b	J15	38	OD, I/O	I3C host/target clock (alternate pin)
I3C_SDA_b	J13	37	OD, I/O	I3C host/target data (alternate pin)
I2C0_MS_SCL	J15	38	OD, I/O	I2C0 host/target clock
I2C0_MS_SDA	J13	37	OD, I/O	I2C0 host/target data
I2C1_MS_SCL	H16	40	OD, I/O	I2C1 host/target clock
I2C1_MS_SDA	H14	36	OD, I/O	I2C1 host/target data
I2C1_MS_SCL_b	J7	28	OD, I/O	I2C1 host/target clock (alternate pin)
I2C1_MS_SDA_b	K8	30	OD, I/O	I2C1 host/target data (alternate pin)
UART				
UART0_RX	D12	50	D, IN	UART0 RX data in
UART0_TX	C13	48	D, OUT	UART0 TX data out
UART0_CTS	K12	33	D, IN	UART0 CTS flow control
UART0_RTS	K10	35	D, OUT	UART0 RTS flow control
UART0_CTS_b	J7	28	D, IN	UART0 CTS flow control (alternate pin)
UART0_RTS_b	K8	30	D, OUT	UART0 RTS flow control (alternate pin)
UART0_RX_b	J11	31	D, IN	UART0 RX data in (alternate pin)
UART0_TX_b	G11	29	D, OUT	UART0 TX data out (alternate pin)
UART0_RX_c	J9	27	D, IN	UART0 RX data in (alternate pin)
UART0_TX_c	H10	25	D, OUT	UART0 TX data out (alternate pin)
UART1_RX	A15	58	D, IN	UART1 RX data in
UART1_TX	D14	53	D, OUT	UART1 TX data out
UART1_RX_b	J13	37	D, IN	UART1 RX data in (alternate pin)
UART1_TX_b	J15	38	D, OUT	UART1 TX data out (alternate pin)
UART2_RX	H14	36	D, IN	UART2 RX data in
UART2_TX	H16	40	D, OUT	UART2 TX data out
UART2_RX_b	J9	27	D, IN	UART2 RX data in (alternate pin)
UART2_TX_b	B10	66	D, OUT	UART2 TX data out (alternate pin)
QSPI Host, SPI Target, SPI Host				
QSPI_CLK/SPI_SL_SCK	B16	57	D, IN/OUT	QSPI CLK SPI target CLK
QSPI_CS0/SPI_SL_CS	E13	49	D, IN/OUT	QSPI chip select SPI target chip select
QSPI_SI/QSPI_SIO0/SPI_SL_SDI	C15	55	D, IN/OUT	QSPI SI/SIO0 SPI target SDI
QSPI_SO/QSPI_SIO1/SPI_SL_SD	D16	51	D, IN/OUT	QSPI SO/SIO1 SPI target SDO
QSPI_SIO2	D14	53	D, IN/OUT	QSPI SIO2
QSPI_SIO3	A15	58	D, IN/OUT	QSPI SIO3

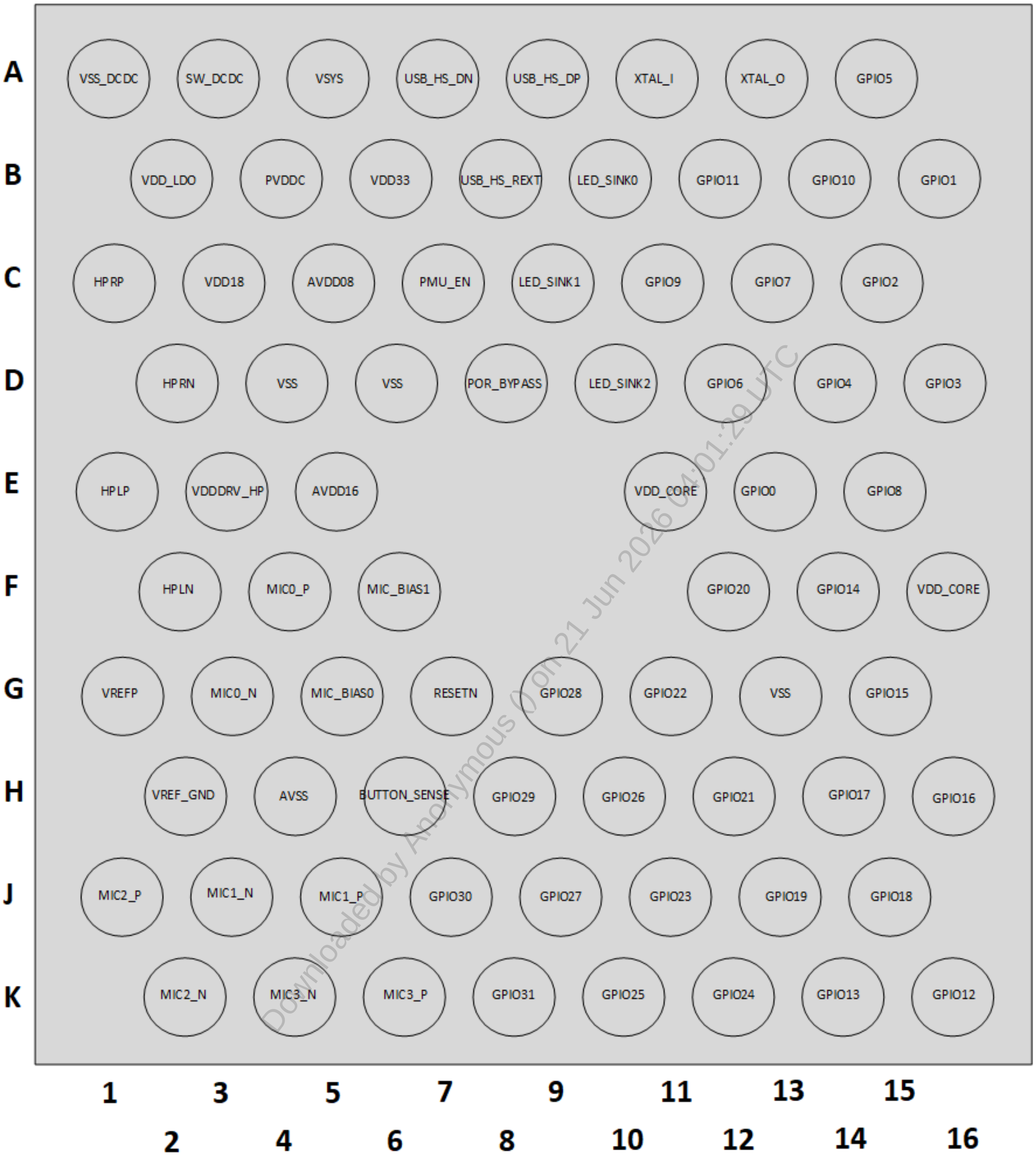
Signal	Ball	Pad	Type, Direction	Description
SPI_SL_SCK_b	D12	50	D, IN	SPI target CLK (alternate pin)
SPI_SL_CS_b	K16	39	D, IN	SPI target chip select (alternate pin)
SPI_SL_SDI_b	C13	48	D, IN	SPI target SDI (alternate pin)
SPI_SL_SDO_b	F14	43	D, OUT	SPI target SDO (alternate pin)
SPI1_MSTR_CLK	G11	29	D, OUT	SPI1 host clock
SPI1_MSTR_CS	J11	31	D, OUT	SPI1 host chip select
SPI1_MSTR_MOSI	K12	33	D, OUT	SPI1 host data out
SPI1_MSTR_MISO	K10	35	D, IN	SPI1 host data in
SPI2_MSTR_CLK	H10	25	D, OUT	SPI2 host clock
SPI2_MSTR_CS	J9	27	D, OUT	SPI2 host chip select
SPI2_MSTR_MOSI	G9	32	D, OUT	SPI2 host data out
SPI2_MSTR_MISO	H8	34	D, IN	SPI2 host data in
SDIO Interface				
SD_CLK	H10	25	D, IN	SDIO clock
SD_DAT0	H8	34	D, IN/OUT	SDIO data line 0
SD_DAT1	J7	28	D, IN/OUT	SDIO data line 1
SD_DAT2	K8	30	D, IN/OUT	SDIO data line 2
SD_DAT3	J9	27	D, IN/OUT	SDIO data line 3
SD_CMD	G9	32	D, IN/OUT	SDIO command line
USB Interface				
DP	A9	67	D, IN/OUT	USB D+
DM	A7	69	D, IN/OUT	USB D-
TXRTUNE	B8	65	A, IN	Tuning resistor input
Reset				
RESETN	G7	23	D, IN	Active-low chip reset input
GPIO				
GPIO[0:31]	–	–	D, IN/OUT	Fully configurable GPIO pins (see pin multiplexing section)
Crystal				
XTAL_I/MASTER_CLK	A11	63	D, IN	Crystal In pin Host CLK In
XTAL_O	A13	61	D, I/O	Crystal Out pin
Digital Microphones				
DM0_CLK/CLKOUT	F12	44	D, OUT	DMIC0 clock
DM0_DATA	H12	42	D, IN	DMIC0 data
DM1_CLK	G11	29	D, OUT	DMIC1 clock
DM1_DATA	J11	31	D, IN	DMIC1 data
DM2_CLK	K12	33	D, OUT	DMIC2 clock
DM2_DATA	K10	35	D, IN	DMIC2 data

Signal	Ball	Pad	Type, Direction	Description
DM3_CLK	H10	25	D, OUT	DMIC3 clock
DM3_DATA	J9	27	D, IN	DMIC3 data
DM3_CLK_b	F14	43	D, OUT	DMIC3 clock (alternate pin)
DM3_DATA_b	K16	39	D, IN	DMIC3 data (alternate pin)
Analog Microphones				
MIC0_P	F4	12	A, IN	Mic0 input (positive) MADC input
MIC0_N	G3	14	A, IN	Mic0 input (negative)
MIC1_P	J5	20	A, IN	Mic1 input (positive)
MIC1_N	J3	18	A, IN	Mic1 input (negative)
MIC2_P	J1	19	A, IN	Mic2 input (positive)
MIC2_N	K2	21	A, IN	Mic2 input (negative)
MIC3_P	K6	22	A, IN	Mic3 input (positive)
MIC3_N	K4	24	A, IN	Mic3 input (negative)
MIC_BIAS0	G5	8	A, OUT	Bias voltage for microphones
MIC_BIAS1	F6	10	A, OUT	Bias voltage for microphones
Multi-button Sense				
BUTTON_SENSE	H6	6	A, IN	Pushbutton array MADC input.
Headphone				
HPLP	E1	13	Diff, O	Headphone positive left output
HPLN	F2	11	Diff, O	Headphone negative left output
HPRP	C1	5	Diff, O	Headphone positive right output
HPRN	D2	7	Diff, O	Headphone negative right output
VDDDRV_HP	E3	9	A, OUT	Headphone driver supply filter pin
PWM LEDs				
LED_SINK0	B10	66	D, OUT	PWM LED sink 0 1-Wire PLC TX (UART2_TX_b)
LED_SINK1	C9	64	D, OUT	PWM LED sink 1
LED_SINK2	D10	62	D, OUT	PWM LED sink 2
PWM3	G9	32	D, OUT	PWM LED output 3
PWM4	J7	28	D, OUT	PWM LED output 4
PWM5	K8	30	D, OUT	PWM LED output 5
Power				
PMU_EN	C7	72	D, IN	Enable signal for PMU (LDOs, DC-DC)
POR_BYPASS	D8	2	—	—
VSYS	A5	73	P, IN	Main system supply input (from VBUS or battery). Input to DC-DC Input to 3.3-V LDO
SW_DCDC	A3	75	P, OUT	Switching node of DC-DC converter

Signal	Ball	Pad	Type, Direction	Description
VDD_LDO	B2	74	P, IN	Input to core LDO Input to 0.8-V LDO
VDD18	C3	1	P, IN	HP driver supply I/O voltage supply
VDD33	B6	70	P, OUT	Output of 3.3-V LDO
AVDD16	E5	4	P, OUT	Output of 1.65-V LDO
AVDD08	C5	3	P, OUT	Output of 0.8-V LDO
PVDDC	B4	71	P, OUT	Output of core LDO
VDD	E11 F16	46 52	P, IN	Digital cores voltage supply Power from PVDDC
VREF	G1	15	A, OUT	0.96 V analog reference voltage
VREF_GND	H2	17	A, GND	Analog reference ground
AVSS	H4	16	GND	Analog ground
VSS	D4 D6 G13	26 45 68	GND	Digital ground
VSS_DCDC	A1	76	GND	DC-DC ground

3.2. Pin Assignments

The SR80 Series WLCSP pin assignment is shown in Figure 2.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS_DCDC		SW_DCDC		VSYS		USB_HS_DN		USB_HS_DP		XTAL_I		XTAL_O		GPIO5	
B		VDD_LDO		PVDDC		VDD33		USB_HS_REXT		LED_SINK0		GPIO11		GPIO10		GPIO1
C	HPRP		VDD18		AVDD08		PMU_EN		LED_SINK1		GPIO9		GPIO7		GPIO2	
D		HPRN		VSS		VSS		POR_BYPASS		LED_SINK2		GPIO6		GPIO4		GPIO3
E	HPLP		VDDDRV_HP		AVDD16						VDD_CORE		GPIO0		GPIO8	
F		HPLN		MIC0_P		MIC_BIAS1						GPIO20		GPIO14		VDD_CORE
G	VREFP		MIC0_N		MIC_BIAS0		RESETN		GPIO28		GPIO22		VSS		GPIO15	
H		VREF_GND		AVSS		BUTTON_SENSE		GPIO29		GPIO26		GPIO21		GPIO17		GPIO16
J	MIC2_P		MIC1_N		MIC1_P		GPIO30		GPIO27		GPIO23		GPIO19		GPIO18	
K		MIC2_N		MIC3_N		MIC3_P		GPIO31		GPIO25		GPIO24		GPIO13		GPIO12

Figure 2. SR80 Series pin assignment (package balls facing down)

The SR80 Series LGA pin assignment is shown in Figure 3.

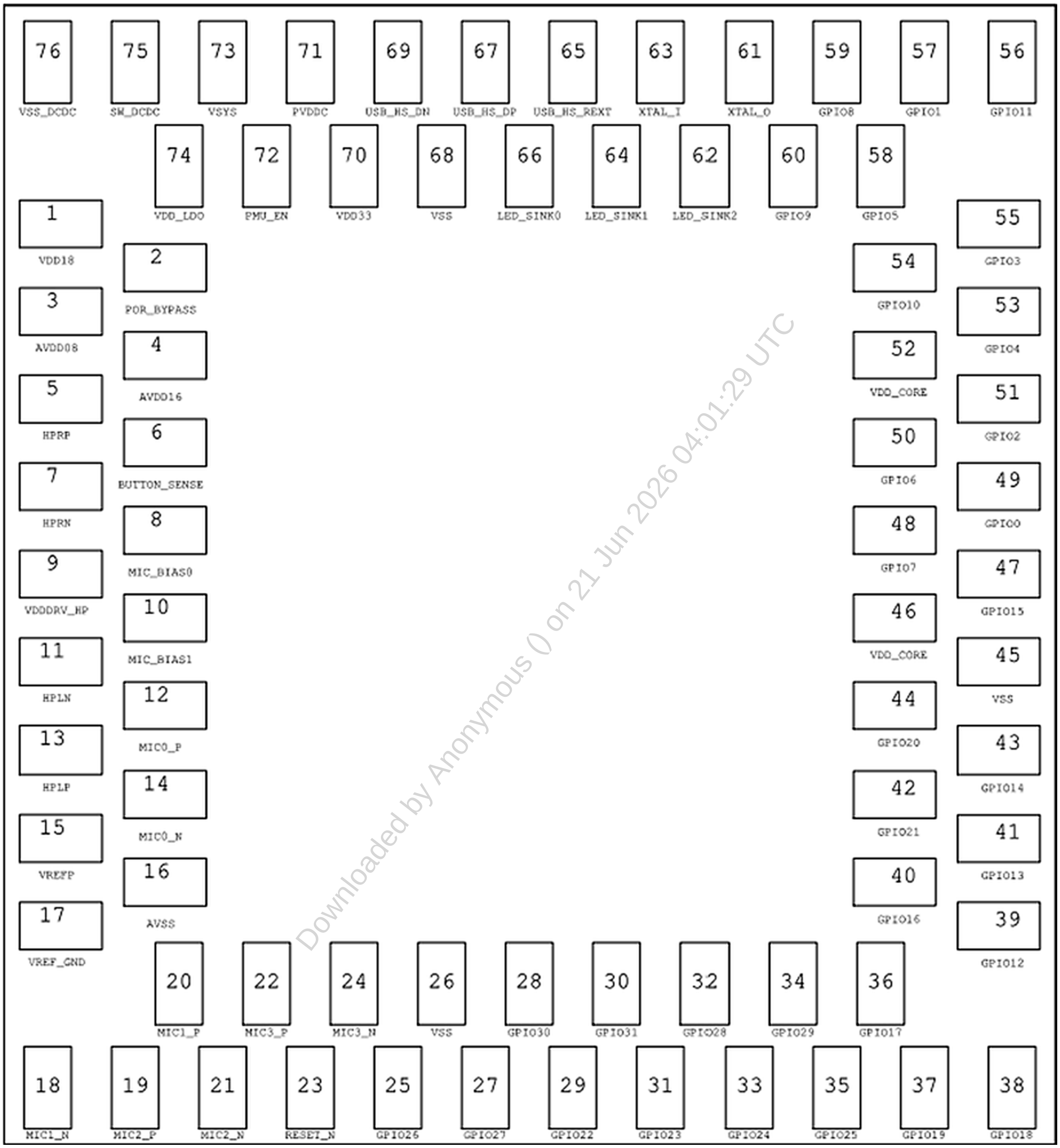


Figure 3. SR80 Series pin assignment (package pads facing down)

3.3. Pin Multiplexing

Many of the SR80 Series device pins support multiple functions, one of which can be enabled at a given time.

All 32 GPIOs can be configured for multiple functions (that is, functions are multiplexed at the pin). This section tabulates the functions supported by each of the device pins, along with other pin attributes (default function, input, output, pull-up/pull-down resistor and so on).

Table 4. Pin multiplexing for the SR80 Series GPIOs.

Name	Ball No.	Pad No.	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	PU/PD
QSPI_CS/SPI_SL_CS	E13	49	GPIO0	QSPI_CS	SPI_SL_CS	—	—	—	—	PU
QSPI_CLK/SPI_SL_SCK	B16	57	GPIO1	QSPI_CLK	SPI_SL_SCK	—	—	—	—	PU
QSPI_SI/QSPI_SIO0/SPI_SL_SDI	D16	55	GPIO3	QSPI_SI/SIO0	SPI_SL_MOSI	—	—	—	—	Hi-Z
QSPI_SO/QSPI_SIO1/SPI_SL_SDO	C15	51	GPIO2	QSPI_SO/SIO1	SPI_SL_MISO	—	—	—	—	Hi-Z
QSPI_SIO2/GP4/UART1_TX	D14	53	GPIO4	QSPI_SIO2	UART1_TX	—	—	—	—	Hi-Z
QSPI_SIO3/GP5/UART1_RX	A15	58	GPIO5	QSPI_SIO3	UART1_RX	—	—	—	—	Hi-Z
I2C_SLV_SCL/UART0_RX	D12	50	GPIO6	I2C_SLV_SCL	UART0_RX	I3C_SCL	SPI_SL_SCK_B	—	—	PU
I2C_SLV_SDA/UART0_TX	C13	48	GPIO7	I2C_SLV_SDA	UART0_TX	I3C_SDA	SPI_SL_MOSI_B	—	—	PU
I2S0_PCM_BCLK	E15	59	GPIO8	I2S0_BCLK	—	—	—	—	—	Hi-Z
I2S0_PCM_WS	C11	60	GPIO9	I2S0_WS	—	—	—	—	—	Hi-Z
I2S0_PCM_TX_DAT	B14	54	GPIO10	I2S0_TX_DAT	—	—	—	—	—	Hi-Z
I2S0_PCM_RX_DAT	B12	56	GPIO11	I2S0_RX_DAT	—	—	—	—	—	Hi-Z
GP12/TDI_A/I2S1_RX	K16	39	TDI_A	GPIO12	I2S1_RX_DAT	SPI_SL_CS_B	DM3_DATA_B	—	—	Hi-Z
GP13/I2S1_WS	K14	41	GPIO13	I2S1_WS	—	—	—	—	—	Hi-Z
GP14/TDO_A/I2S1_TX_DAT	F14	43	TDO_A	GPIO14	I2S1_TX_DAT	SPI_SL_MISO_B	DM3_CLK_B	—	—	PD (**STRAP0**)
GP15/I2S1_BCLK/TRSTN	G15	47	GPIO15	I2S1_BCLK	TRSTN	—	—	—	—	Hi-Z
TCK/I2C1_MS_SCL/UART2_TX	H16	40	TCK_A	GPIO16	I2C1_MS_SCL	UART2_TX	—	—	—	PU
TMS/I2C1_MS_SDA/UART2_RX	H14	36	TMS_A	GPIO17	I2C1_MS_SDA	UART2_RX	—	—	—	PU
I2C0_MS_SCL/I2S2_TX_B	J15	38	GPIO18	I2C0_MS_SCL	I2S1_TX_DAT_B	UART1_TX_B	I3C_SCL_B	—	—	PU
I2C0_MS_SDA/I2S2_RX_B	J13	37	GPIO19	I2C0_MS_SDA	I2S1_RX_DAT_B	UART1_RX_B	I3C_SDA_B	—	—	PU

Name	Ball No.	Pad No.	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	PU/PD
DM0_CLK/CLKOUT	F12	44	GPIO20	DM0_CLK	CLKOUT	TDO_B	—	—	—	PU
DM0_DATA	H12	42	GPIO21	DM0_DATA	TDI_B	1-Wire_RX_B	—	—	—	Hi-Z
DM1_CLK/UART0_TX_B/I2S2_CLK	G11	29	GPIO22	DM1_CLK	UART0_TX_B	I2S2_BCLK	SPI1_MSTR_CLK	—	—	Hi-Z
DM1_DATA/UART0_RX_B/I2S2_WS	J11	31	GPIO23	DM1_DATA	UART0_RX_B	I2S2_WS	SPI1_MSTR_CS	—	—	Hi-Z
DM2_CLK/CLKOUT UART0_CTS/I2S2_TX (**STRAP1**)	K12	33	GPIO24	DM2_CLK	UART0_CTS	I2S2_TX_DAT	SPI1_MSTR_MOSI	—	—	PD (**STRAP1**)
DM2_DATA/UART_RTS/TDI_B/I2S2_RX	K10	35	GPIO25	DM2_DATA	UART0_RTS	I2S2_RX_DAT	SPI1_MSTR_MISO	—	—	Hi-Z
GP26 (**TEST_N**)	H10	25	GPIO26	I2S2_BCLK_B	UART0_TX_C	DM3_CLK_A	—	SPI2_MSTR_CLK	SD_CLK	PU (**TEST_N**)
GP27	J9	27	GPIO27	I2S2_WS_B	UART0_RX_C	DM3_DATA_A	—	SPI2_MSTR_CS	SD_DAT3	Hi-Z
GP28	G9	32	GPIO28	I2S2_TX_DAT_B	PWM3	—	—	SPI2_MSTR_MOSI	SD_CMD	PD
GP29	H8	34	GPIO29	I2S2_RX_DAT_B	—	—	—	SPI2_MSTR_MISO	SD_DAT0	Hi-Z
GP30	J7	28	GPIO30	I2C1_MS_SCL_B	PWM4	—	—	UART0_CTS_B	SD_DAT1	Hi-Z
GP31	K8	30	GPIO31	I2C1_MS_SDA_B	PWM5	—	—	UART0_RTS_B	SD_DAT2	Hi-Z

3.4. Bootstrapping Pins

Some signal pins in the SR80 Series device are used to configure the device for a certain mode at power up.

Table 5. Bootstrap pins.

Bootstrap	Assigned Pin	Reset State	Description
STRAP0	GPIO14	PD	STRAP[1:0] used by boot ROM to select boot option.
STRAP1	GPIO24	PD	
TEST_N	GPIO26	PU	TEST_N is pulled down to enable product test mode; pull up at power up during normal mode.

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation under these conditions or at any other condition beyond those indicated for normal operation is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings.

Supply	Min.	Max.	Units	Description
VSYS	−0.3	7.0	V	Main system supply, typically from battery or USB interface. Input to 3.3-V LDO Input to DC-DC
VDD18	−0.3	1.98	V	VDD for HP driver, typically sourced from DC-DC I/O input supply, typically sourced from DC-DC

4.2. DC Supply Voltages

Table 7. DC supply voltages

Supply	Min.	Typical	Max.	Units	Description
VSYS	3.1	3.7/5.0	5.5	V	Main system supply, typically from battery or USB interface. Input to 3.3-V LDO Input to DC-DC
VDD33	−5%	3.3	+5%	V	Output of 3.3-V LDO
VDD18	−5%	1.8	+5%	V	VDD for HP driver, typically sourced from DC-DC I/O input supply, typically sourced from DC-DC
VDD_LDO	−5%	1.8 1.0	+5%	V	Input to core LDOs, typically source from DC-DC 1.8 V or 1.0 V depends on mode
PVDDC	−5%	0.8	+5%	V	Output of VDDCORE LDO
VDD	−5%	0.8	+5%	V	Input voltage supply for digital cores Power from PVDDC
AVDD16	−5%	1.6	+5%	V	Output of 1.6-V LDO Main supply for analog TX/RX blocks
AVDD08	−5%	0.8	+5%	V	Output of 0.8-V LDO Internally generated voltage for PLLs, OSC
VDDDRV_HP	−5%	1.8	+5%	V	Headphone driver supply filter pin

4.3. Analog Characteristics

4.3.1. DAC Performance

Table 8. DAC analog characteristics

DAC Output Path					
Headphone load RL = 32 Ω					
Parameter	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
Full scale output	R_L = 16 Ω, THD < 0.1% R_L = 32 Ω, THD < 0.1%	—	0.7 1.0	—	Vrms
Headphone load	—	16	32	—	Ω
Dynamic range	−60 dBFS signal source, A-weighted	—	110	—	dBA
SNR	0 dBFS for signal measurement Silence for noise measurement, A-weighted	—	120	—	dBA
THD+N	−1 dB signal source	—	-95	—	dB
Crosstalk	32 Ω stereo load	—	-100	-95	dB
Intermodulation Distortion (IMD)	5 mW output level −8 dB 60 Hz, -20 dB 7 kHz	—	-85	—	dB
DC Offset	|Voffset|	—	<50	100	µV DC
Pop Level	—	—	-75	—	dBV
Frequency response	20 Hz to 20 kHz	—	.04	.05	dB
Phase error	Between two channels 997 Hz, 0 dBFS signals	—	—	.01	degree
PSRR	@ 217 Hz – square wave, 100 mVpp, 12.5% duty cycle	80	—	—	dB
	@ 1 kHz – sine wave	80	—	—	dB
Output Capacitive Loading	Single-ended capacitance	—	0.5	—	nF
Output resistance	Measure –20 dBFS, 1 kHz signal with and without resistive load, calculate resistance.	—	0.5	—	Ω

4.3.2. ADC Performance

Table 9. ADC analog characteristics

MIC ADC Path Differential Cap-less Input					
Parameter	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
Full scale voltage	0 dB gain +6 dB gain +12 dB gain	—	1.0 0.5 0.25	—	V rms
Dynamic range	−60 dBFS, A-weighted, 0 dB gain −60 dBFS, A-weighted, 6 dB gain −60 dBFS, A-weighted, 12 dB gain	—	105 — —	—	dBA
THD+N	-1 dBFS	—	-90	—	dB
Crosstalk*	Channel to channel @ 1 kHz	—	-130	-120	dB
PSRR	217 Hz, 200 mVpp	—	—	—	dB
Analog gain range	—	0	—	12	dB
Analog gain step size	—	—	6	—	dB
Input impedance	—	—	>1M	—	Ω
Input capacitance	—	—	100	—	pF

* Crosstalk: Measurements are made with one channel driven to -1 dBFS and all other MIC inputs shorted to GND.

4.3.3. Microphone Bias Characteristics

Table 10. Microphone bias parameters

Parameter	Test Conditions/Notes	Minimum	Typical	Maximum	Unit
Mic bias Output Voltage	Used as bias for the analog microphone	1.2	—	3.0	V
Mic bias Output Voltage	In bypass mode to 1.8 V supply	—	1.8	—	V
Mic bias Voltage Step	—	—	0.1	—	V
Mic bias Load Current	—	—	—	5.0	mA
Load Capacitance	Microphone bias output does not require load capacitor for stability	0	—	10	μF

4.4. Digital I/O

4.4.1. DC Characteristics

Table 11. DC characteristics – TTL compatible (GPIOs)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Input voltage low	VIL	0	—	0.3 x DVDDIO	V	—
Input voltage high	VIH	DVDDIO x 0.7	—	DVDDIO	V	—
Output voltage low	VOL	0	—	0.2 x DVDDIO	V	—
Output voltage high	VOH	0.8 x DVDDIO	—	DVDDIO	V	—
GPIO output sink current at VOL with DVDDIO = 1.8V	IOL	—	—	8	mA	—
GPIO output source current at VOH with DVDDIO = 1.8V	IOH	—	—	8	mA	—

4.5. SD, SDIO Timing

4.5.1. SD, SDIO Default Mode Timing Parameters

Table 12. SD, SDIO Default Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	25	25	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	10	—	—	ns
t_{WH}	Clock High time	—	10	—	—	
t_{TLH}	Clock Rise time	—	—	—	10	
t_{THL}	Clock Fall time	—	—	—	10	
Inputs CMD, DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	5	—	—	ns
t_{IH}	Input Hold time	—	5	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output delay time	Data Transfer Mode	0	—	14	ns
t_{ODLY}	Output delay time	Identification Mode	0	—	50	

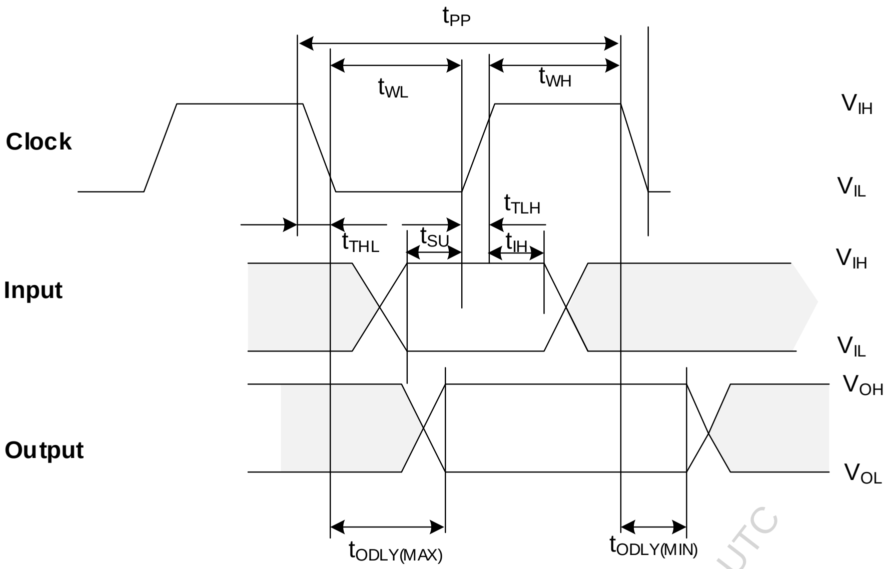


Figure 4. Timing Diagram Data Input/Output Referenced to Clock (Default)

4.5.2. SD, SDIO High-Speed Mode Timing Parameters

Table 13. SD, SDIO High-Speed Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	50	50	MHz
t_{WL}	Clock Low time	—	7	—	—	ns
t_{WH}	Clock High time	—	7	—	—	
t_{TLH}	Clock Rise time	—	—	—	3	
t_{THL}	Clock Fall time	—	—	—	3	
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	6	—	—	ns
t_{IH}	Input Hold time	—	2	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Delay time	Data Transfer Mode	0	—	14	ns
t_{OH}	Output Hold time	—	2.5	—	—	

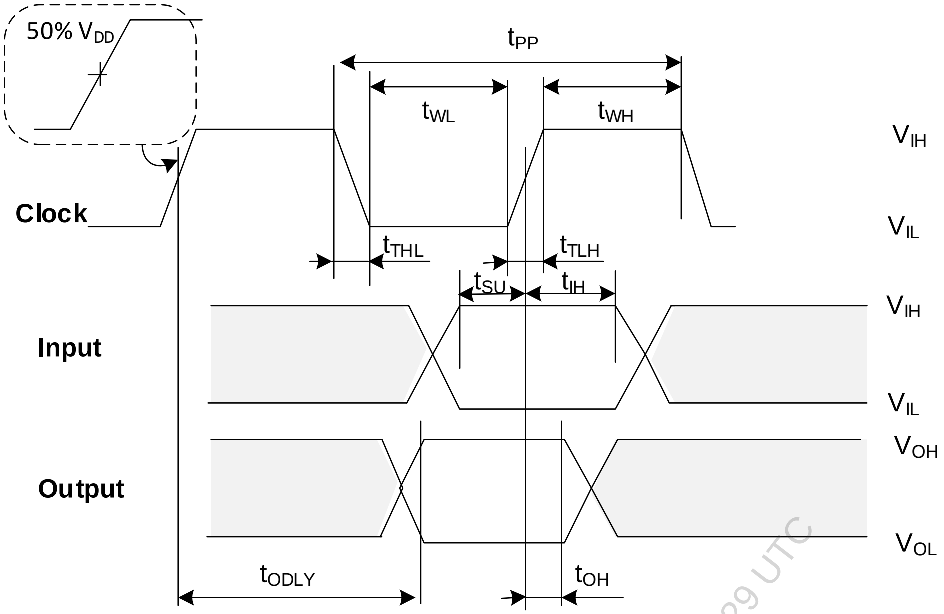


Figure 5. Timing Diagram Data Input/Output Referenced to Clock (high-speed)

4.5.3. SD, SDIO SDR50 Mode Timing Parameters

Table 14. SD, SDIO SDR50 Mode Timing Parameters

Symbol	Parameter		Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	—	0	100	100	MHz
t_{WL}	Clock Low time	—	—	1.44	—	—	ns
t_{WH}	Clock High time	—	—	1.44	—	—	
t_{TLH}	Clock Rise time	—	—	—	—	2	
t_{THL}	Clock Fall time	—	—	—	—	2	
Inputs DAT (referenced to Clock):							
t_{ISU}	Input Setup time	—	—	3	—	—	ns
t_{IH}	Input Hold time	—	—	0.8	—	—	
Outputs CMD, DAT (referenced to Clock):							
t_{ODLY}	Output Delay time	Data Transfer Mode		0	—	7.5	ns
t_{OH}	Output Hold time	—		1.5	—	—	

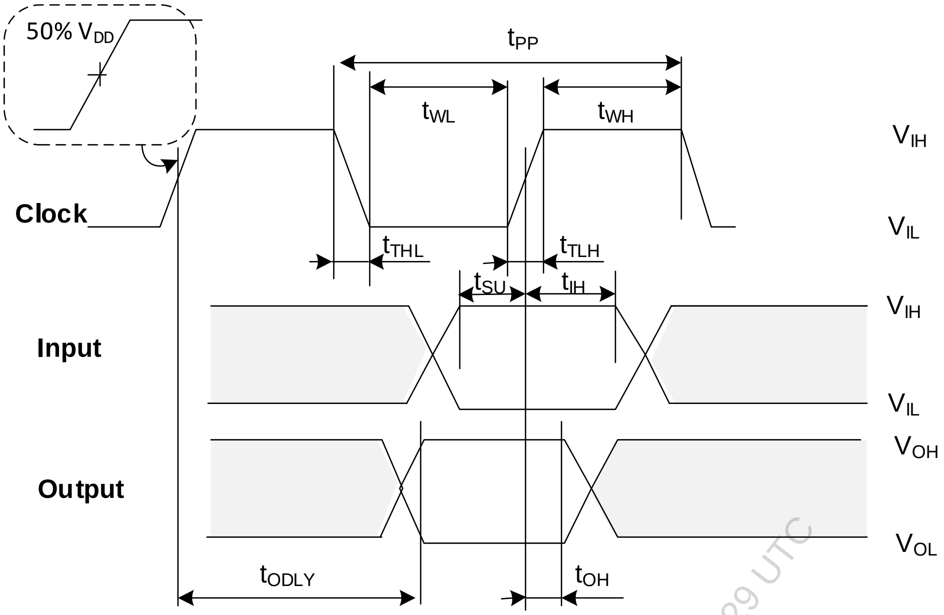


Figure 6. Timing diagram data I/O referenced to clock (high-speed & SDR50 mode)

4.6. Two-Wire Serial Interface (TWSI) Timing – I2C Compatible Timing

4.6.1. TWSI Standard and Fast Mode Timing

Table 15. TWSI Standard and Fast Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{TWSI_SCL}	SCL Clock Frequency	100 kHz	—	—	100	kHz
		400 kHz	—	—	400	
T_{TWSI_NS}	Noise Suppression Time at SCL, SDA Inputs	100 kHz	—	—	80	ns
		400 kHz	—	—	80	
T_{TWSI_R}	SCL, SDA Rise time	100 kHz	—	—	1000	
		400 kHz	—	—	300	
T_{TWSI_F}	SCL, SDA Fall Time	100 kHz	—	—	300	
		400 kHz	—	—	300	
T_{TWSI_HIGH}	Clock High Period	100 kHz	4000	—	—	
		400 kHz	600	—	—	
T_{TWSI_LOW}	Clock Low Period	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
$T_{TWSI\_SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700	—	—	
		400 kHz	600	—	—	
$T_{TWSI\_HD:STA}$	Start Condition Hold Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
$T_{TWSI\_SU:STO}$	Stop Condition Setup Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{TWSI\_SU:DAT}$	Data in Setup Time	100 kHz	250	—	—	
		400 kHz	100	—	—	
$T_{TWSI\_HD:DAT}$	Data in Hold Time	100 kHz	300	—	—	
		400 kHz	300	—	—	
T_{TWSI_BUF}	Bus Free Time	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
T_{TWSI_DLY}	SCL Low to SDA Data Out Valid	100 kHz	40	—	200	
		400 kHz	40	—	200	

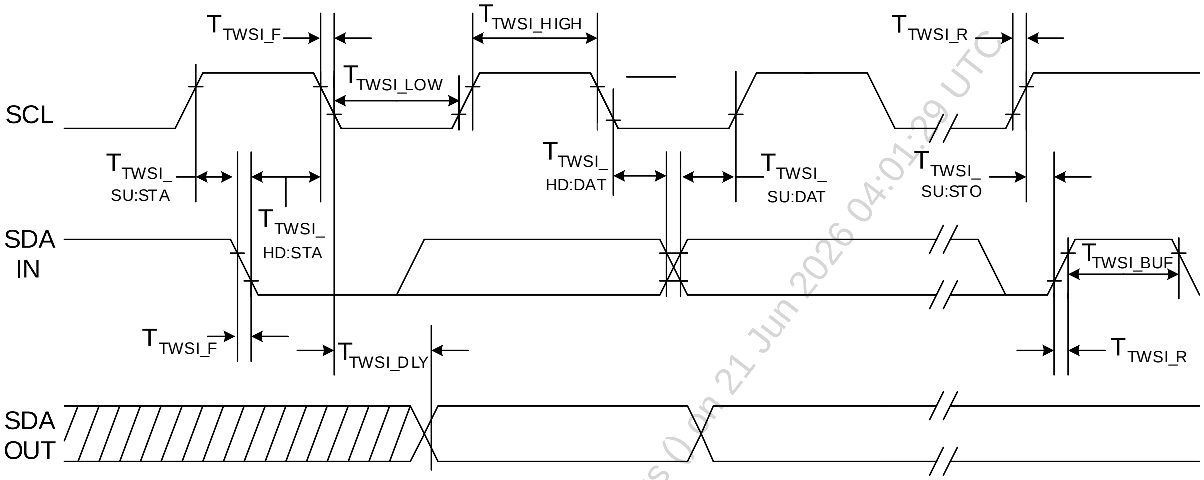


Figure 7. Two-wire serial interface timing

4.6.2. TWSI Fast mode plus – transfer rates up to 1 Mbits/s

For timing information, refer to the *I2C Bus Specification*.

4.7. UART Timing

Table 16. UART timing

Symbol	Parameter	Condition	Min	Typ[1]	Max	Units
—	Tx bit width	±5%	—	8.68	—	μs
—	Rx bit width	±5%	—	8.68	—	

1. Typical values are given for a baud rate of 115.2 kbaud. Other baud rates are supported, and bit width scales inversely with the configured baud rate.

4.8. USB 2.0 Timing

The SR80 Series features an integrated USB 2.0 high-speed device interface (up to 480 Mbps).
The interface supports USB Audio Class 1.0 and USB Audio Class 2.0 and provides up to 10 endpoints

4.8.1. USB 2.0 DC Characteristics

Table 17. USB 2.0 DC Electrical

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	High (driven)	Note[1]	2.0	—	—	V
V_{IHZ}	High (floating)		2.7	—	3.6	
V_{IL}	Low		—	—	0.8	
V_{DI}	Differential Input Sensitivity	|(D+)-(D-)| Note[1]	0.2	—	—	
V_{CM}	Differential Common Mode Range	Includes VDI range Note[1]	0.8	—	2.5	
Input Levels for High-speed						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	—	100	—	150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)	—	525	—	625	
V_{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	—	-50	—	500	
Output Levels for Full-speed						
V_{OL}	Low	Note[1], Note[2]	0.0	—	0.3	V
V_{OH}	High (Driven)	Note[1], Note[3]	2.8	—	3.6	
V_{OSE1}	SE1	—	0.8	—	—	
V_{CRS}	Output Signal Crossover voltage	Note[4]	1.3	—	2.0	
Output Levels for High-speed						
V_{HSOI}	High-speed idle level	—	-10.0	—	10.0	mV
V_{HSOH}	High-speed data signaling high	—	360	—	440	
V_{HSOL}	High-speed data signaling low	—	-10.0	—	10.0	
V_{CHIRPJ}	Chirp J level (differential voltage)	—	700	—	1100	
V_{CHIRPK}	Chirp K level (differential voltage)	—	-900	—	-500	
Input Capacitance for Full-speed						
C_{IND}	Downstream Facing Port	Note[5]	—	—	150	pF
C_{INUB}	Upstream Facing Port (without cable)	Note[6]	—	—	100	
C_{EDGE}	Transceiver edge rate control capacitance	—	—	—	75	

Symbol	Parameter	Condition	Min	Typ	Max	Units
Terminations						
R_{PU}	Bus pull-up Resistor on Upstream facing port	1.5 kOhm ±5%	1.425	—	1.575	kOhm
R_{PD}	Bus pull-down Resistor on Downstream Facing Port	15 kOhm ±5%	14.25	—	15.75	
Z_{INP}	Input impedance exclusive of pullup/pull-down (for full-speed)	—	300	—	—	
V_{TERM}	Termination voltage for upstream facing port pull-up (RPU)	—	3.0	—	3.6	V
Termination in High-speed						
V_{HSTERM}	Termination voltage in high-speed	—	-10	—	10	mV

1. Measured at A or B connector.
2. Measured with RL of 1.425 kohm to 3.6V.3.
3. Measured with RL of 14.25 kohm to GND.
4. Excluding the first transition from the idle state.
5. Measured at A receptacle.6.
6. Measured at B receptacle.

4.8.2. USB 2.0 Source Electrical Characteristics

Table 18. USB High-Speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics						
T_{HSR}	Rise Time (10%–90%)	—	500	—	—	ps
T_{HSF}	Fall Time (10%–90%)	—	500	—	—	
Z_{HSDRV}	Driver Output Resistance (which also serves as high-speed termination)	—	40.5	—	49.5	Ohm
Clock Timings						
T_{HSDRAT}	High-speed Data Rate	—	479.760	—	480.240	Mbps
T_{HSFRAM}	Microframe Interval	—	124.9375	—	125.0625	µs
T_{HSRFI}	Consecutive Microframe Interval Difference	—	—	—	4 high-speed bit times	—

Table 19. USB Full-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics						
T_{FR}	Rise Time	—	4	—	20	ns
T_{FF}	Fall Time	—	4	—	20	
T_{FRFM}	Differential Rise and Fall Time Matching	T_{FR}/T_{FF} Note[1]	90	—	111.11	%
Z_{DRV}	Driver Output Resistance for driver which is not high-speed capable.	—	28	—	44	Ohm
Clock Timings						
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high speed capable.	Average bit rate	11.9940	—	12.0060	Mbps
T_{FDRATE}	Full-speed Data Rate for devices which are high-speed capable.	Average bit rate	11.9700	—	12.0300	
T_{FRAME}	Frame Interval	—	0.9995	—	1.0005	ms
T_{RFI}	Consecutive Frame Interval Jitter	No clock adjustment	—	—	42	ns
Full-speed Data Timings						
T_{DJ1}	Source Jitter Total (including frequency tolerance): To Next Transition	Note[1] Note[2] Note[3] Note[4]	-3.5	—	3.5	ns
T_{DJ2}	For Paired transitions		-4	—	4	
T_{FDEOP}	Source Jitter for Differential Transition to SE0 Transition	Note[3]	-2	—	5	
T_{JR1}	Receiver jitter: To Next Transition	Note[3]	-18.5	—	18.5	
T_{JR2}	For Paired Transitions	—	-9	—	9	
T_{FEOPT}	Source SE0 interval of EOP	—	160	—	175	
T_{FEOPR}	Receiver SE0 interval of EOP	Note[5]	82	—	—	
T_{FST}	Width of SE0 interval during differential transition	—	—	—	14	

1. Excluding the first transition from the idle state.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. For both transitions of differential signaling.
5. Must accept as valid EOP.

4.9. I2S Timing

4.9.1. I2S Host Mode Timing

Table 20. I2S Host Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	—	—	24.576	MHz
F_{S}	Sample rate	—	—	—	192	kHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{SDPD1}	BCLK rising edge to SDATA output valid	—	—	0.5	—	ns
T_{LRPD}	BCLK rising edge to LRCK valid	—	—	0.5	—	ns
T_{SDS}	Set-up time SDATA input with regard to BCLK rising edge	—	—	6.58	—	ns
T_{SDH}	Hold time SDATA Input with regard to BCLK rising edge	—	—	0	—	ns
F_{MCLK}	MCLK (not shown) output frequency	—	—	—	12.288	MHz
D_{MCLK}	MCLK output duty cycle	—	—	50	—	%

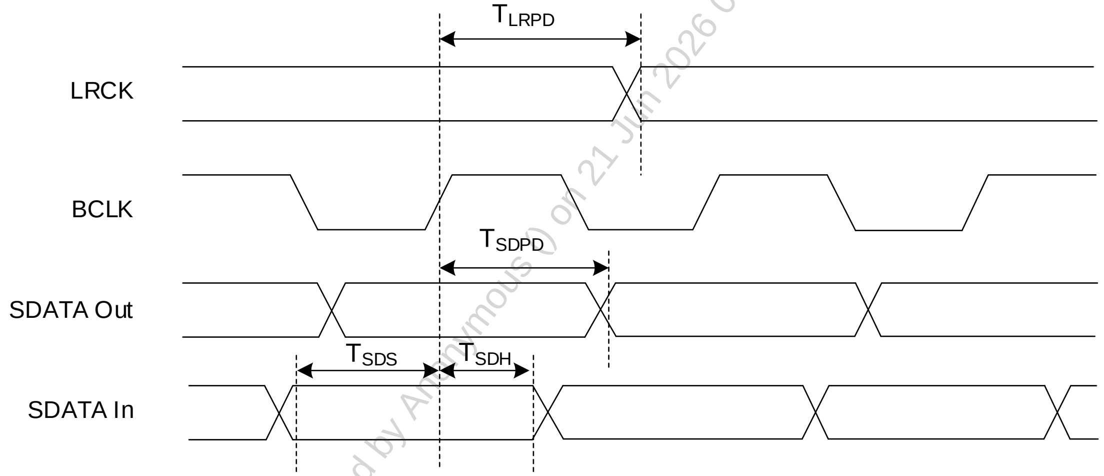


Figure 8. I2S Host mode timing.

4.9.2. I2S Target Mode Timing

Table 21. I2S Target mode timing parameters.

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	—	—	24.576	MHz
F_S	Sample rate	—	—	—	192	kHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{LRS}	Setup time LRCK input with regard to BCLK active edge	—	—	0.5	—	ns
T_{LRH}	Hold time LRCK input with regard to BCLK active edge	—	—	0.5	—	ns
T_{SDS}	Setup time SDATA Input with regard to BCLK active edge	—	—	2	—	ns
T_{SDH}	Hold time SDATA Input with regard to BCLK active edge	—	—	0	—	ns
F_{MCLK}	MCLK (not shown) input frequency	—	—	—	25	MHz
D_{MCLK}	MCLK input duty cycle	—	—	50	—	%

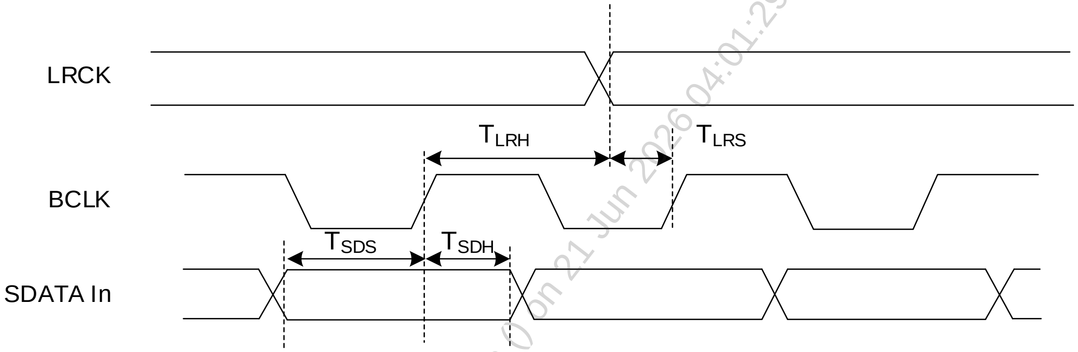


Figure 9. I2S Target mode timing.

4.10. SPI Timing

Table 22. SCLK Cycle Time Configurable Range

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SCLK}	SoC SPI SCLK cycle time	100 MHz SoC SPI controller input clock	20	—	655,340	ns

(Applies across the full range of values listed in Recommended Operating Conditions, unless otherwise specified.)

Table 23. Motorola SPI Mode 0/2 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	The first SPI cycle in a transfer	—	1.5	—	TSCLK
		Subsequent SPI cycles	—	0.5	—	
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	Other than the last SPI cycle	—	1	—	TSCLK
		The last SPI cycle in a transfer	—	1.0	—	
T_{CH}	SCLK high time	—	—	0.5	—	TSCLK
T_{CL}	SCLK low time	—	—	0.5	—	TSCLK
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0.5	—	TSCLK
		If Tx FIFO is empty	2	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	3.5	—	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	0	—	—	ns
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	TSCLK
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	0.12	—	1.28	ns

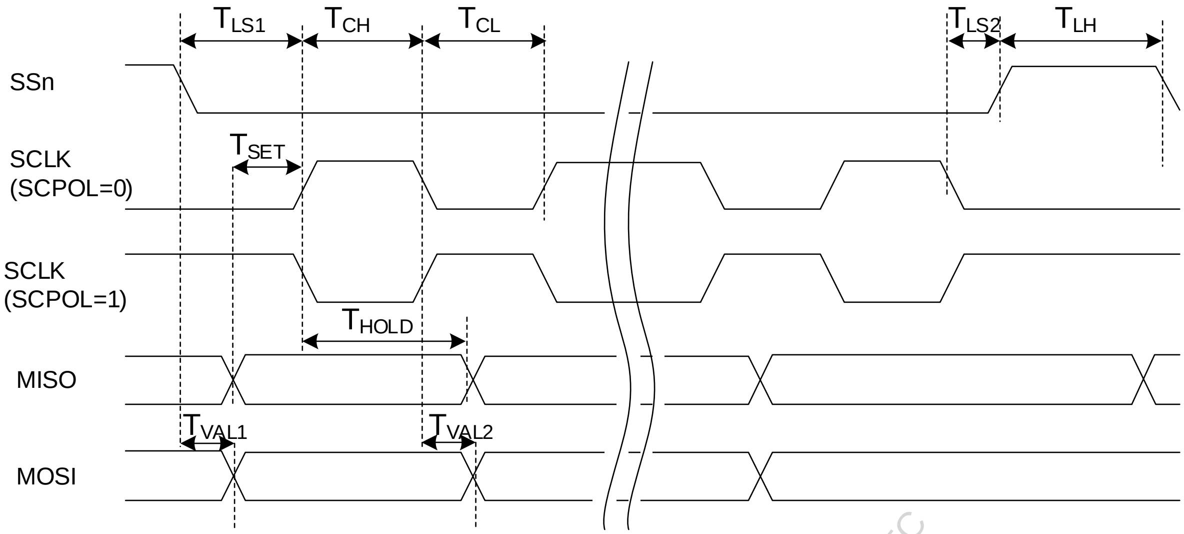


Figure 10. Motorola SPI Mode 0/2 (SCPH = 0)

(Applies across the full range of values listed in Recommended Operating Conditions, unless otherwise specified.)

Table 24. Motorola SPI Mode 1/3 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	—	—	1.0	—	TSCLK
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	—	—	1.0	—	TSCLK
T_{CH}	SCLK high time	—	—	0.5	—	TSCLK
T_{CL}	SCLK low time	—	—	0.5	—	TSCLK
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0	—	TSCLK
		If Tx FIFO is empty	1.5	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	3.5	30	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	—	30	—	ns
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	TSCLK
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	—	0.5	—	ns

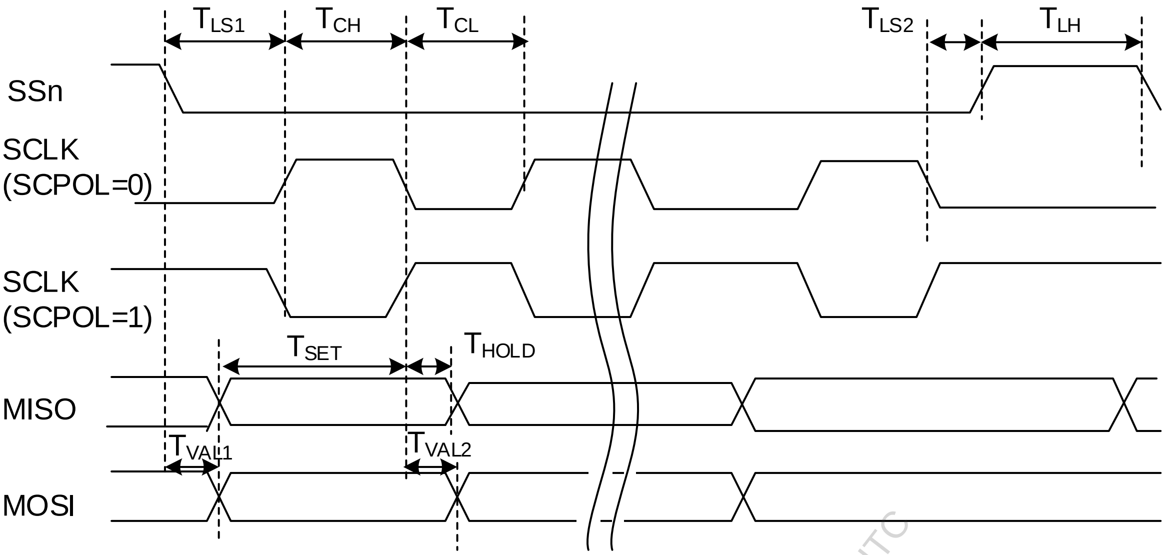


Figure 11. Motorola SPI Mode 1/3 (SCPH = 1)

5. Codec Subsystem

5.1. Overview

A low-power, high-performance, audio codec subsystem provides all the needed circuitry to connect to external transducers.

The DACs and ADCs within the codec section convert the audio to digital streams that can be processed by one or more of the DSPs in the SR80 Series. Audio is processed in two primary paths, the ANC path, and the Audio/Voice processing path. The ANC path uses specialized filters, data paths, and processing for extremely low latency while the Audio/Voice Processing Path offers flexible use of the available resources. The CODEC can be split into two functional sections, the record path (often referred to as the *transmit* or *send path* in telephony) and the playback path (often referred to as the *receive path* in telephony).

The signal data paths are shown in Figure 12.

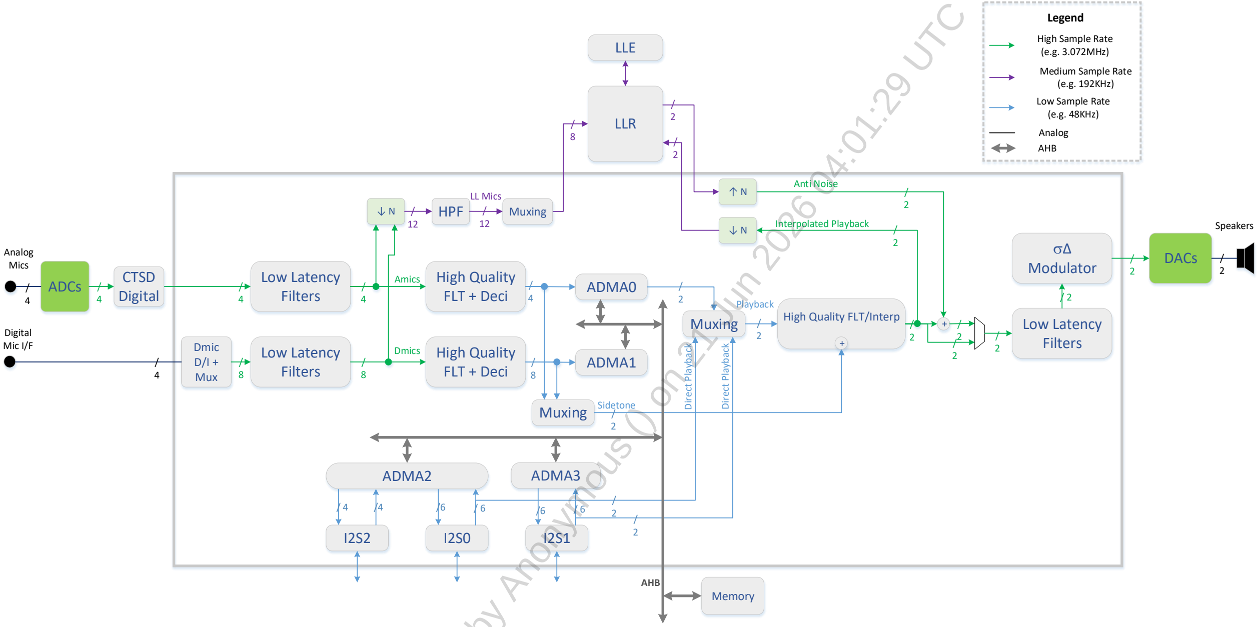


Figure 12. SR80 Series Audio data paths

5.2. Input Path

The codec subsystem has four analog inputs comprised of high dynamic range, high performance ADCs.

The codec subsystem also provides four PDM stereo DMIC interfaces, to connect to eight digital microphones.

5.2.1. Analog Inputs

The SR80 Series has 4 analog inputs capable of supporting microphone or line-level inputs.

- Each of the analog inputs has a dedicated high dynamic range continuous time sigma-delta (CTSD) ADC and programmable gain amplifier (PGA).
- Inputs can be used in a cap-less configuration, without the need for AC-coupling caps for BOM/area savings.
- Inputs provide analog gains of 0, 6, or 12 dB and support input levels up to 1.0 V.
- The analog input channels have dedicated input decimation filters, separate from the digital mic input channels.
- Low latency signal paths to the LLE engine enable ANC functionality.
- High-performance signals path enables advanced microphone DSP algorithms.

Two low noise microphone bias outputs provide 1.2 V to 3.0 V (100 mV resolution) and up to 5 mA of current to power attached microphones. The mic bias generation circuitry uses the 3.3 V LDO.

The mic bias voltage outputs can be used in a “no cap” configuration (0-1 nF) and “with cap” configuration (50 nF – 10 µF), depending on system needs. Configuration setting is via control registers.

The mic bias outputs can also be used in bypass mode, where the 1.8 V supply is connected directly to the mic bias output. This can be used to increase power efficiency, since the 1.8 V supply is generated from a high efficiency DC-DC converter, whereas in normal (non-bypass) mode the mic bias voltage is generated from the VDD33 supply.

Input MIC0P can be re-purposed as input to the 10-bit MADC, for general-purpose voltage measurements.

5.2.2. Microphone Bias

Two low noise microphone bias outputs provide 1.2 V to 3.0 V (100 mV resolution) and up to 5 mA of steady-state DC current to power attached microphones. The mic bias generation circuitry uses the 3.3 V LDO.

The Microphone Bias output current is limited to a value that is configurable by firmware (2 mA, 6 mA, 10 mA, or *disable*). Transient currents during 'output enable' can be higher than 5 mA depending on loading, so it's recommended to set a higher current limit, such as 10 mA, during this transition; the current limit can then be lowered to 6 mA or 2 mA.

The mic bias voltage outputs can be used in a “no cap” configuration (0-1 nF) and “with cap” configuration (50 nF – 10 µF), depending on system needs. Configuration setting is via control registers.

The mic bias outputs can also be used in bypass mode, where the 1.8 V supply is connected directly to the mic bias output. This can be used to increase power efficiency, since the 1.8 V supply is generated from a high efficiency DC-DC converter, whereas in normal (non-bypass) mode the mic bias voltage is generated from the VDD33 supply.

Input MIC0P can be re-purposed as input to the 10-bit MADC, for general-purpose voltage measurements.

5.2.3. *Digital Microphone Inputs*

The SR80 Series has four PDM digital microphone interfaces with separate clock and data pins. One or two digital microphones can be connected to each interface and a total of 8 digital microphones can be used at the same time.

One DMIC clock cannot be configured to be as the clock source for multiple DATA pins.

Each of the digital mic inputs has dedicated hardware decimation filters, to enable simultaneous use of all microphones (8 digital, 4 analog).

5.2.4. *Input Path Signal Decimation*

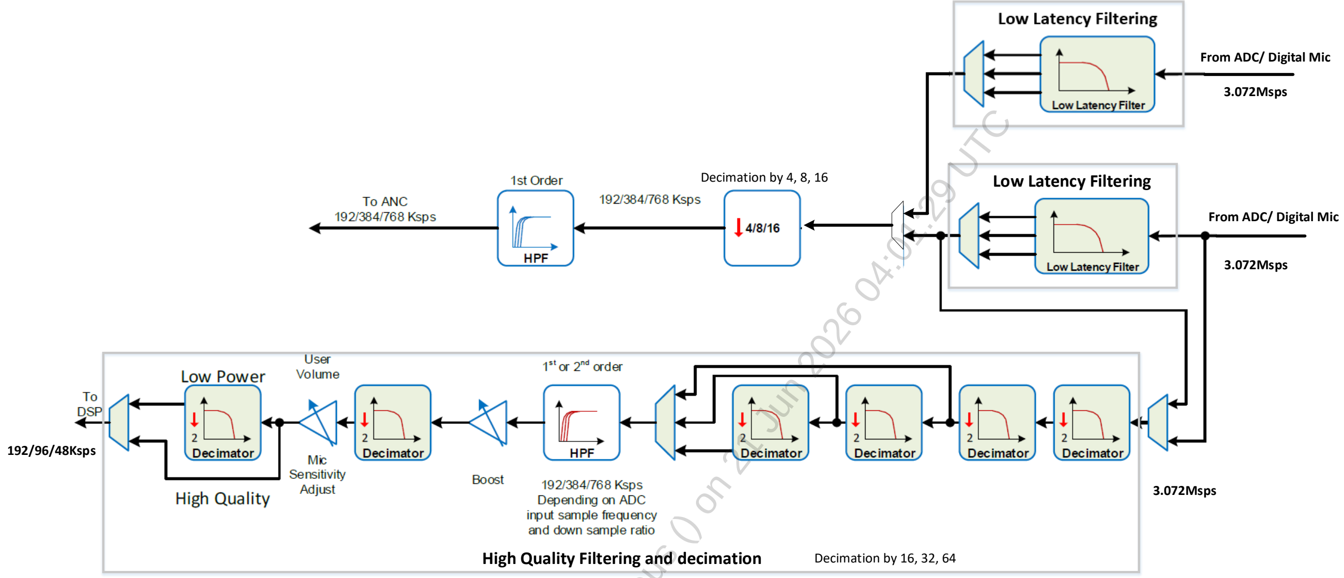


Figure 13. Input signal decimation in SR80 Series

5.3. Analog Playback Path

The Playback path provides hardware interpolation filters, a stereo high-performance DAC, and stereo class-AB/G headphone amplifier to connect the SR80 Series to headphones or other devices.

Low latency signal paths from/to the LLE engine enable ANC functionality.

High-performance audio paths support ANC as well as telephony and media applications. Volume control, anti-pop circuitry, and side-tone mixing are also provided.

5.3.1. DAC + Headphone Amplifier

The DAC and headphone amplifier are optimized for high-performance playback, using a class-AB design.

In addition, class G operation allows power-sensitive use cases to benefit from improved power efficiency by switching to a lower amplifier supply voltage.

The outputs are differential (balanced) and thus should not be connected to ground-connected loads.

- 1.0 Vrms/32 Ω
- 0.7 Vrms/16 Ω
- >40 kHz bandwidth (-1 dB)
- ±0.03 dB magnitude response from 20 Hz to 20 kHz
- 24-bit DAC
- Dynamic range of 110 dBA
- Volume control: -74 to +6 dB in 0.5 dB steps
- Audio sample rates up to 192 kHz
- Low latency ANC support

5.3.2. Playback Path Signal Interpolation

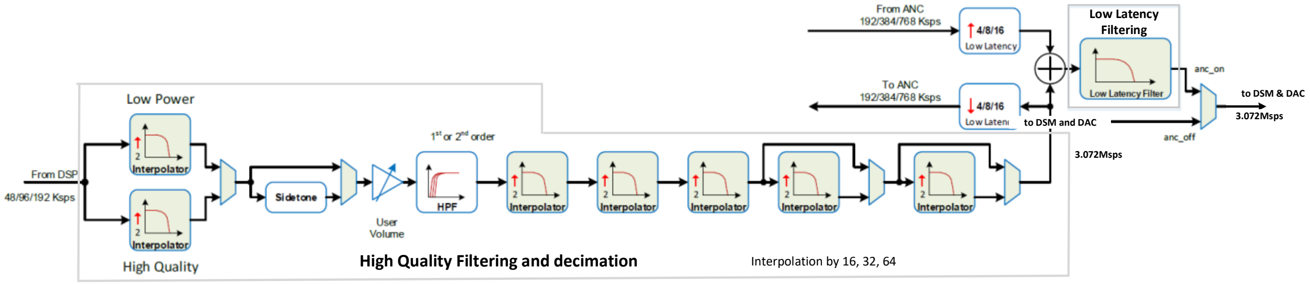


Figure 14. Playback path signal interpolation in SR80 Series

6. M33 CPU Subsystem

A secure, single-core, 32-bit Arm Cortex-M33 based SSE200 sub-system provides system and sensor management and other functions.

The Cortex-M33 was developed to address all embedded and IoT markets, especially those requiring efficient security or digital signal control. TrustZone for ARMv8-M is the foundation of security for all embedded applications. The Cortex-M33 achieves an optimal blend between real time determinism, energy efficiency, software productivity, and system security that opens the door for many new applications and opportunities across diverse markets.

Supported functions:

- System management
- Trust management
- Sensor fusion
- Wake management
- Interrupt processing
- Firmware update
- I/O management

6.1. Hardware Features

The SSE200 system contains:

- A Cortex M33 32-bit processor running up to 250 MHz
- 64-bit wide AXI bus matrix
- Secured subsystem
- System controller
- Power, clock, and reset control infrastructure
- Interrupt controller
- Trust management and encryption

6.2. Software Supported Features

6.2.1. Boot Host

The CPU subsystem boots while all other processors are held in reset allowing for a secure and orderly boot process. The remaining processors are initialized and managed by the CPU subsystem.

6.2.2. Sensor Hub

Connected sensors are managed by the M33 subsystem.

6.3. Memory

The CPU subsystem has:

- 16 KB I-Cache
- 16 KB D-Cache
- 128 KB local SRAM memory
- 64 KB I-tightly coupled memory
- 64 KB D-tightly coupled memory
- 96 KB Local ROM

The QSPI interface allows for code execution from external memory.

6.4. Test/Debug

6.4.1. UART Capture

Debug print messages can be output to a terminal, during code development.

6.4.2. Debug Expansion Module

The debug expansion module provides a trace port and a JTAG debug interface. The JTAG debug interface has these key features:

- JTAG port from DAPSWJDP
- Supports JTAG request to power up the PD_DEBUG power domain through the debug power integration kit (PIK)
- System timestamp generation

6.4.3. M33 Debug Interface

- Timestamp. A 64-bit input driven from an external timestamp generator. The subsystem routes the timestamp to the CPU elements, for use in the Cortex-M33 processor trace data.
- Debug Access. The DAP interface allows an external DAP to access the debug logic in the subsystem.
- Cross Trigger. The CTI interface provides some trigger inputs and outputs for system expansion.
- Debug expansion

6.5. Security

The following security components are available in SSE200 system.

- **MPC:** AHB5 TrustZone memory protection controller
- **AHB5 PPC:** AHB5 TrustZone peripheral protection controller
- **APB PPC:** APB TrustZone peripheral protection controller
- **MSC:** AHB5 TrustZone host security controller
- **SAU:** Security attribution unit
- **IDAU:** Implementation defined attribution unit

6.5.1. Memory Protection Controller

The memory protection controller (MPC) gates transactions to the AHB5 host interface when a security violation occurs. The controller can be instantiated in the system in connection to any non-security aware AHB5 memory. The security checking is done based on block/page level, configured externally by the security controller through an APB interface.

6.5.2. APB Peripheral Protection Controller Block

PPC gates transactions and responses from peripherals when a security violation occurs. The APB4 TrustZone peripheral protection controller can be instantiated in the system in connection to any non-security aware peripherals. The security checking is done based on peripheral (PSEL) inputs configured externally by configuration inputs. (Similar to AHB5 PPC).

6.5.3. MSC with Implementation Defined Attribution Unit

The MSC is an adapter used to connect a legacy AHB-lite host, or an AHB5 host without the security extension to an AHB5 system and add TrustZone for ARMv8-M capability. IDAU Lite interface is used to check if the address is secure or non-secure.

6.5.4. Security Attribution Unit

The MPU improves system reliability by defining the memory attributes for different memory Regions. It provides up to 16 different regions, and an optional predefined background region. There can be two MPUs, one secure and one non-secure. Each MPU can define memory attributes independently. The SAU improves system security by defining security attributes for different regions. It provides up to 8 different regions and a default background region.

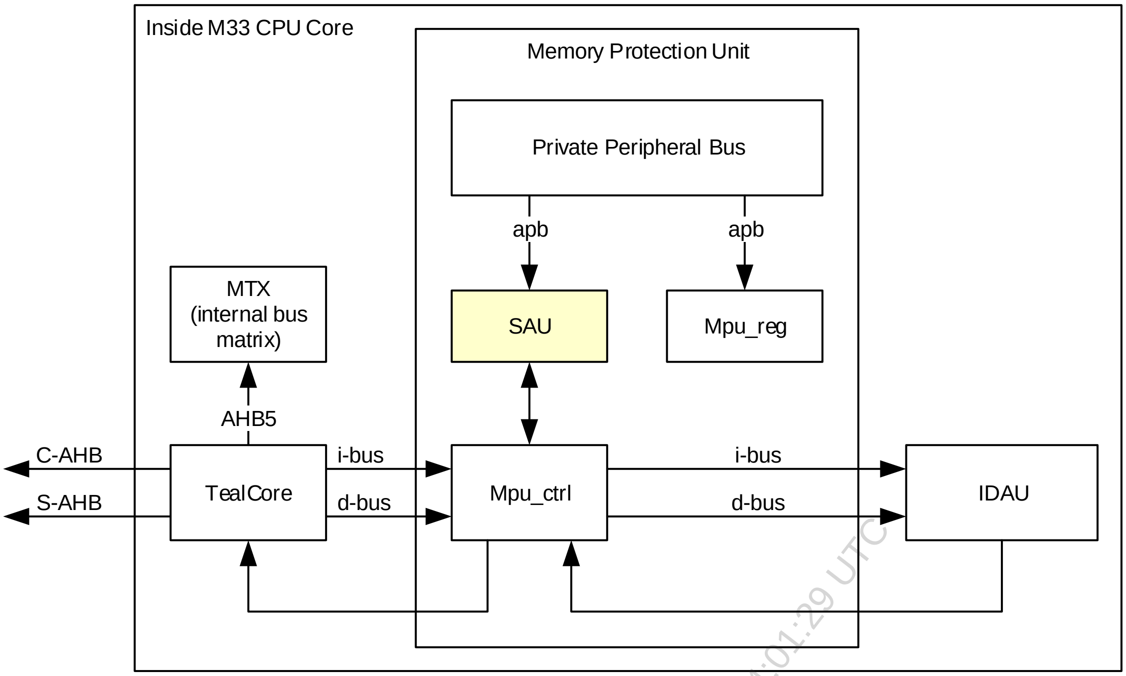


Figure 15. M33 CPU core

6.5.5. Security-use Cases

- Secure boot
  - OTP
  - AES
- Secure firmware upgrade
  - I²C in secure region (via Bluetooth)
- Device identification/authentication
  - AES would be used for this purpose
- Data security including local storage and data over the network
  - AES encryption/decryption
- MPC is used for memory protection
- Secure JTAG debugging
  - Supported by M33

7. HiFi 5 DSP Core

A Tensilica HiFi 5 DSP plus memory subsystem is dedicated for customer and third-party algorithms.

7.1. Hardware

- 32-bit fixed-point and floating-point
- Up to 500 MHz maximum DSP clock
- 1 MB local RAM, plus additional 1.5 MB shared RAM (total 2.5 MB available memory)
- TCM
    - 64 KB instruction
    - 128 KB data
- Cache
    - 32 KB instruction
    - 32 KB data
    - Prefetch
- Compute throughput:
    - Multiple MAC operations per cycle (fixed-point and floating-point)
    - Optimized for high-efficiency audio, voice, and AI workloads
    - Throughput depends on instruction mix, precision, and workload characteristics
- On-chip debug (OCD)/Tensilica TRAX
- Configurable interrupt controller external to the core

7.2. Software

100% open platform running on FreeRTOS (or customer's preferred embedded RTOS).

- Software APIs provided to interact with SoC resources:
    - Control interface to applications running on other processors
    - Control interface for hardware configuration
- Flexible audio routing to and from other processing points within the system

8. Synaptics DSP Subsystem

8.1. Overview

The SR80 Series DSP Subsystem is designed with the following high-level objectives in mind:

- Low power consumption
- Low latency data paths for ANC and ambient fusion
- High-compute processing in low latency data paths
- Flexible memory architecture to support a wide variety of use-cases
- Flexible audio processing platform allows for feature addition in the future
- Customer-configurable DSP

There are three Synaptics DSP cores in this subsystem:

- Two CAPE 2 DSPs
- One low latency engine (LLE - vector processor based on CAPE architecture)

The DSP system memory architecture was designed as the best possible compromise between low-power, flexibility, and cost. There are small pools of memory banks dedicated to each processor. The dedicated pools of standard SRAM (64-bit wide SRAM) banks can be accessed via each processors program, data X, or data Y ports. A dedicated pool of vector SRAM (384-bit wide SRAM) banks can be accessed on vector data X and vector data Y ports. All DSP subsystem SRAM can be accessed via AHB.

Shared local memory is 0.5 MB. This memory is also accessible by the HiFi 5 DSP core.

Mechanisms available for passing data throughout the system:

- System memory
- DMA
- Low latency data path used for low latency single-sample audio routing between DSPs and other hardware elements

8.2. DSP Subsystem Functions

Synaptics DSP engines service these high-level algorithms and tasks:

- ANC: Active noise cancellation
- Ambient Fusion: Processing of sounds external to the ear and subsequently mixed into headphone playback.
- SRC: A variety of concurrent synchronous (SRC) and asynchronous (ASRC) audio sample rate conversions within the 8 kHz to 192 kHz range.
- Playback processing: processing of music playback or voice Rx signal, with modules such as EQ and dynamic range control (DRC).
- Transmit:
  - Tx processing: Primary processing on the transmit communication path such as analysis, noise reduction, acoustic echo cancellation (AEC), and synthesis.
  - Tx post-processing: Processing of the Tx signal in the final stages before passing the signal to the transmit device such as EQ and DRC.
- Voice Wake and Voice Command
  - Keyword detection

8.2.1. Hybrid ANC

The SR80 Series provides high quality low-power active noise cancellation (ANC), with ultra-low latency. The full processing path is all digital, providing for consistent performance, ease of tuning, and algorithm upgradability/configurability.

The ANC algorithm makes use of both an external microphone (feedforward cancellation) and an internal microphone (feedback cancellation) to achieve optimal results. The algorithm can operate in either a static non-adaptive mode or in adaptive mode. Audio intended to be heard by the user, such as music playback or the receiving channel in a voice call, is not altered by the ANC algorithm, nor does the audio degrade the ANC performance.

Ambient sounds can be seamlessly mixed into the headphone speaker output along with anti-noise produced by ANC, enabling users to flexibly manage which ambient sounds they hear and which are filtered out.

8.2.2. ENC

Noise suppression algorithms significantly improve the quality of voice pickup in noisy environments and allow for decent quality voice pickup either with no boom or a short boom.

The noise suppression algorithms employ advanced signal processing techniques to single out the user's voice and suppress all other sounds picked up by the microphones.

Noise reduction for all major electronic devices is available.

8.2.3. Sample Rate Conversion

Sample rate conversion (SRC) supports common rates from 8 kHz to 192 kHz. SRCs are typically used to convert between processing rates for different algorithms (software modules) running on either Synaptics DSPs or the Tensilica HiFi 5 DSP. Low-MIPS/high-quality SRCs are used for integer ration conversions. Conversions between 44.1 kHz and 48 kHz are provided.

Both synchronous and asynchronous sample rate converters are available.

8.2.4. Playback Processing

Equalization (EQ) and dynamic range control (DRC) can be applied to the playback audio signal. The EQ is a multiband IIR design allowing for flexible control over frequency response.

Playback processing also includes a simple tone generator and file playback, both mixed into the playback stream before DRC is applied. Tones and file playback can be used for various user audio notifications.

8.3. CAPE 2

The CAPE 2 DSP is the latest generation of Synaptics audio DSPs, designed specifically for high-quality, low-power audio processing.

- Dual 32-bit fixed-point and floating-point
- Up to 250 MHz core frequency
- Compute throughput:
    - 2 × 32-bit (floating-point or fixed-point) MACs per cycle
    - 4 × 16-bit fixed-point MACs per cycle
    - 8 × 8-bit fixed-point MACs per cycle
- Flexible and easy to use memory architecture
- Dual 64-bit data memory buses
- Extensive arithmetic instruction set
- Complex arithmetic
- Program cache

8.4. LLE

The low latency engine (LLE) is a variant of the CAPE 2 processor with vector processing extensions. It is optimized for low-latency/high-compute audio processing applications such as ANC.

- 16 24-bit fixed-point MACs
- Dual 384-bit vector memory data buses
- Extensive arithmetic instruction set
- Complex arithmetic
- Program cache

9. Synaptics NPU

Synaptics easy-to-use and highly optimized AI Neural Network acceleration processor working seamlessly with HiFi5 DSP supporting TensorFlow Lite for Microcontrollers.

- Easy to use and flexible NN processor with provided Synaptics SynAI optimized compiler supporting offline weight compression and easy to use and debug simulator.
- Supporting most computation intensive TFLM NN operators for advanced AI voice and audio applications.
- On-the-fly NN model weight decompressor
- Up to 500 MHz maximum core speed
- Compute throughput:
  - 32 (8×8-bit) or 16 (16×8-bit) MACs per cycle; up to 32 GOPS @ 500 MHz
- 75% average MAC usage
- 32 kB local buffer and flexible allocation of low-latency shared system memory

The Synaptics NPU is supported with easy-to-use tools, including compiler that generates optimized models, enabling the efficient assignment of operators, as well as a simulator for offline development, and an NPU Profiler for in-depth analysis.

The Synaptics NPU supports NN models of various architectures, and upgradeable operators.

10. Memories

The SR80 Series contains many different internal memory blocks. Memory blocks may be local or external to a processor and may be available or restricted based on memory protection settings. Internal memory can be split into three memory types: OTP, RAM, and ROM.

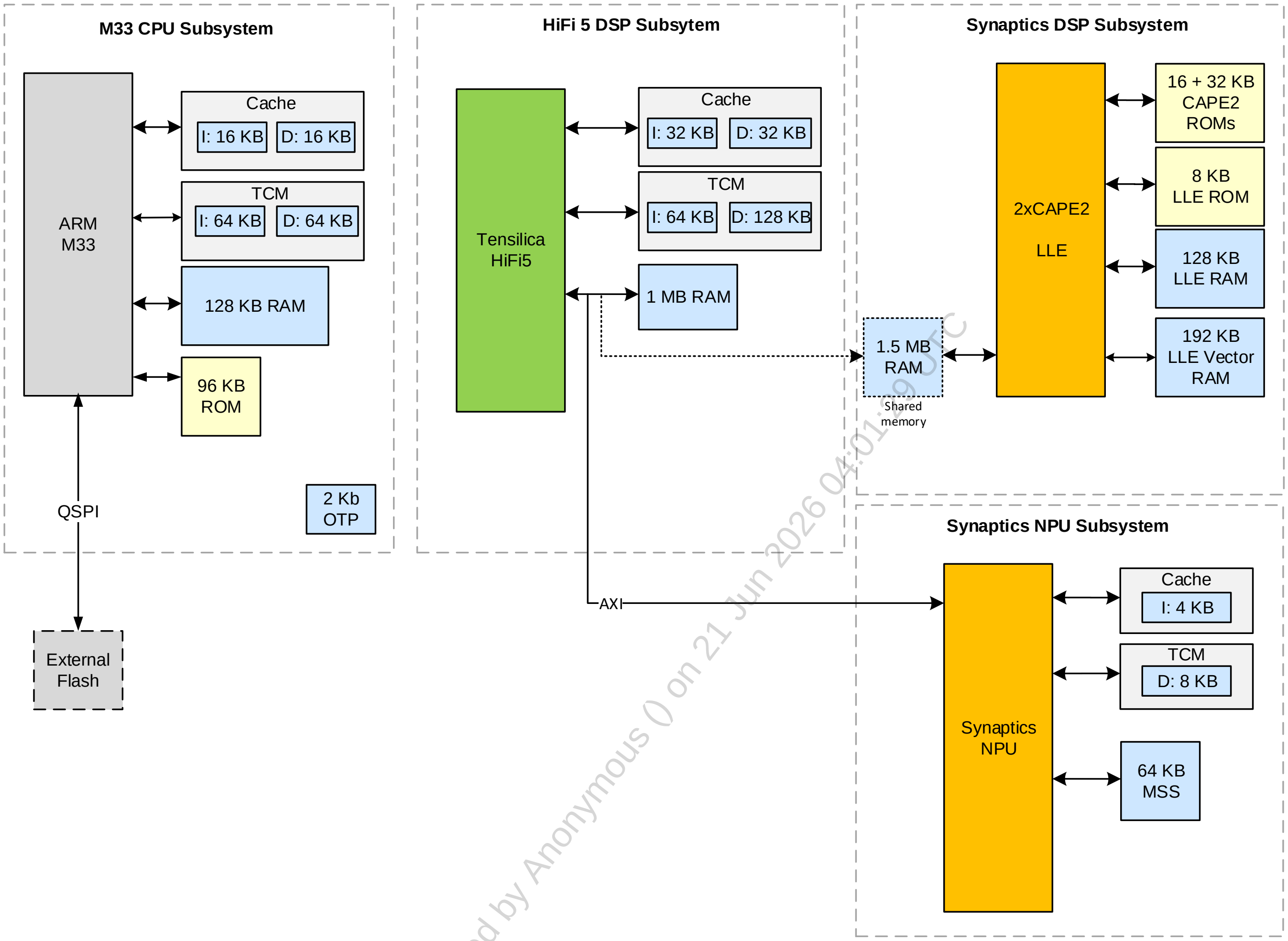


Figure 16. SR80 Series Memories

10.1. OTP

A 2 Kbit one-time programmable (OTP) memory provides persistent storage of production test calibration values and security keys.

10.2. RAM

The total RAM memory of approximately 3.5 MB is divided into:

- System memories
- Local memories

Within memory, there are vector memory banks and standard (scalar) memory banks. There are five DSPs (CAPE 2 A, CAPE 2 B, LLE, NPU, and HiFi 5) and a CPU (Arm Cortex-M33) sharing these memory banks.

- Standard memory:
    - Each processor has several banks of its own local standard memory
    - Local and cache memories are accessible by other processors when not in use
    - In addition, there is a pool of sharable banks that every DSP can use
    - Standard memory is byte-addressed in 64-bit lines
    - All DSPs use standard memory for X data, Y data, and P program
- Vector memory:
    - A separate subsystem used by the LLE

10.2.1. Local (dedicated) Memory

Each processor has local tightly coupled SRAM usable for either program or data. The Synaptics DSP Subsystem has a total of 1.5 MB of local shared SRAM, and additional 128 KB RAM for LLE.

10.2.2. System (scalar) Memory

Each processor can access system memory. Accesses to system memory are arbitrated with AHB as the highest priority. System memory is 64 bits wide.

10.2.3. Vector Memory

- 192 KB RAM
- Used by LLE

10.3. ROM

The Arm CPU and Synaptics DSP subsystems have ROM for boot code and other static information.

11. Clock and Reset

11.1. Clock Sources

The SR80 Series uses the following clocks and time-base sources:

- Crystal/MCLK
- Standard RC oscillator (STD_OSC)
- Low-power RC oscillator (LP_OSC)
- I2S0 BCLK
- I2S1 BCLK
- I2S2 BCLK
- USB start-of-frame (SOF)

11.2. Crystal/MCLK

For USB-only applications, the SR80 Series requires the use of a 24 MHz crystal, with the following specifications:

- Frequency: 24 MHz
- Frequency tolerance: 400 ppm
- Peak jitter: +/- 100 psec
- Duty cycle: 40/60 maximum

For other applications, an external clock source at MCLK can be used (such as a DECT or Bluetooth device), applied at the XTAL_I/MASTER_CLK pin.

The supported MCLK frequency range is 512 kHz to 25 MHz.

11.3. STD and LP Oscillators

The integrated standard RC oscillator (STD_OSC) in the SR80 Series generates a clock in the 16-32 MHz range. This clock is suitable as the clock source for audio use cases (PLL reference clock, ADC/DAC clock) when an external clock source is not available.

The STD_OSC oscillator is factory calibrated during production testing to ~1% frequency accuracy, with ~3% frequency variation across temperature.

The STD_OSC oscillator can also be adjusted to the same frequency as XTAL_I/MASTER_CLK, which can minimize frequency jumps when switching from external to internal clock source.

The low-power RC oscillator (LP_OSC) in the SR80 Series generates a 200 kHz internal clock. It is intended to provide a low-power clock for non-audio, low-power use cases (for example, standby or sleep).

The LP_OSC oscillator is factory calibrated to ~5% frequency accuracy.

11.4. PLLs

Two PLLs are integrated into the SR80 Series: one is the integer PLL, and the other is the fractional PLL.

Both PLLs use the following as reference clock inputs:

- I2S0, I2S1, I2S2 BCLK inputs
- XTAL_I/MASTER_CLK input
- STD_OSC internal clock

The I2S BCLK input frequency range supported is 512 kHz to 24.576 MHz.

The outputs of the PLLs are used to provide the needed clocks for the various sub-systems (audio, M33, HiFi 5, NPU, and so on), with appropriate clock dividers as needed.

11.5. PLL Reference Management

Inputs to the PLLs are managed by the PLL Reference Management block.

11.6. Reference On/Off Detection

Reference On/Off Detection block generates interrupts when the external reference is turned off or on.

Each PLL reference has a dedicated Reference On/Off Detection mechanism.

Ideally, software should be aware of when the external reference will be turned off, to manage the transition accordingly and to minimize impact on audio.

When in Automatic mode, the reference selection can be switched to internal reference when the external reference is detected to be off. This ensures that there is no loss of clock but does not necessarily ensure clean audio transitions.

11.7. USB Start-of-Frame (SOF)

The USB sub-system provides a start-of-frame time reference (1 kHz for FS, 8 kHz for HS) that is used for ASRC and clock measurements.

11.8. Clock Measurement

The clocking scheme in the SR80 Series includes a Clock Measurement block that measures the phase/frequency of various clocks to allow reference tracking and controlling the PLL output frequency accordingly.

11.9. Reset

The SR80 Series has a dedicated active-low chip reset pin (RESETN). A logic *HIGH* at this pin brings the device out of reset, provided the internal power management has completed power-on enable sequence (with PMU_EN signal).

The RESETN pin has an integrated pull-up resistor; an external resistor and capacitor can be used for more precise reset timing.

12. I2S/TDM Digital Audio

The SR80 Series device integrates three I2S/TDM digital audio interfaces, enabling digital audio connectivity in digital systems such as Bluetooth and DECT.

All three I2S interfaces can operate as host (transmit clocks) or target (receive clocks).

In target mode operation, the I2S BCLK inputs can be used as inputs to the internal clock generation blocks.

I2S0 and I2S1 support 6 RX channels, 6 TX channels.

I2S2 supports 4 RX channels, 4 TX channels.

The I2S interface block supports the following modes and configurations on the I2S/PCM bus:

- Word lengths of 8, 16, 24 bits
- Supports Philips (I^2S)/left justified/right justified/PCM/TDM modes.
- Supports host and target mode.
- Supports sharing of the WS signal between transmitter and receiver.
- Programmable length of WS signal in host mode.
- Data may be driven on falling or rising edge of BCLK.
- Programmable channel order: 'left then right' or 'right then left'
- BCLK frequency range: 512 kHz to 24.576 MHz

12.1. I2S Mode Timing

The I2S timing uses WS (LRCK) to define whether the data is being transmitted for the left channel or for right channel. The WS is low for the left channel and high for the right channel. A WS polarity control bit is provided to allow either high or low to represent the left channel. The default setting of the polarity control is 0, which means low WS = left channel. The WS need not be symmetrical.

A system clock (BCLK) running at a minimum of 2 • (sample width) • (sample frequency) is used to clock in the data. There is a delay of one clock bit from the time the WS signal changes state to the first data bit on the data line. The data is written MSB first and is valid on the rising edge of the bit clock. When the programmed sample width is taken, any remaining bits are ignored.

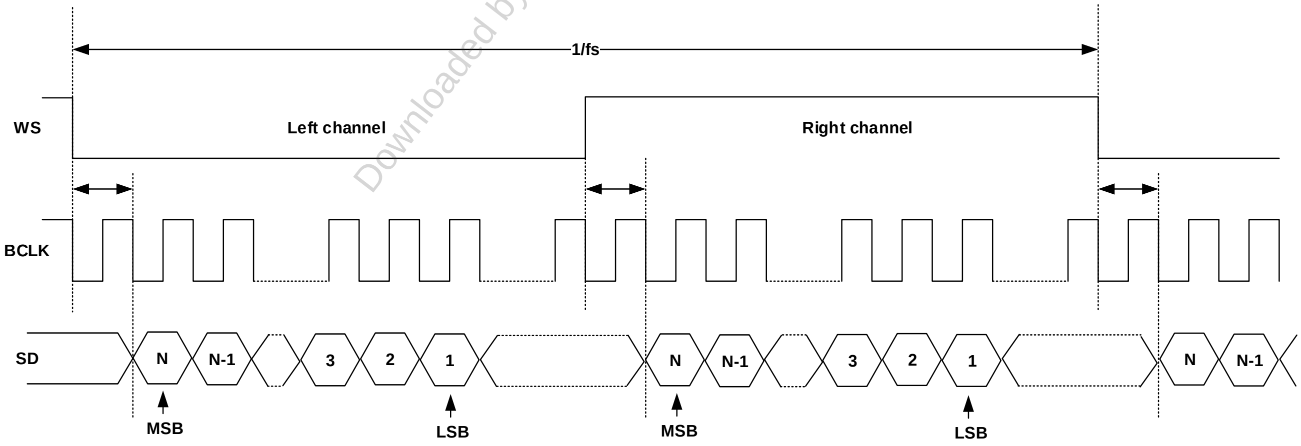


Figure 17. I2S timing diagram – width of LRCLK frame is wider than 2N bits (N = 8, 16, 24, or 32)

12.2. Left-justified Mode Timing

Left-justified timing uses the WS clock to define when the data being transmitted is for the left channel and when it is for the right channel. The WS is high for the left channel and low for the right channel (requires the WS polarity control bit to be set to 1). A bit clock running at a minimum of 2 • (sample width) • (sample frequency) is used to clock the data.

The first data bit appears on the data lines at the same time WS toggles. The data is written MSB first and is valid on the rising edge of the bit clock. When the programmed sample width is taken, any remaining bits are ignored. If the WS toggles before the full word length is read, the remaining bits are zeroed.

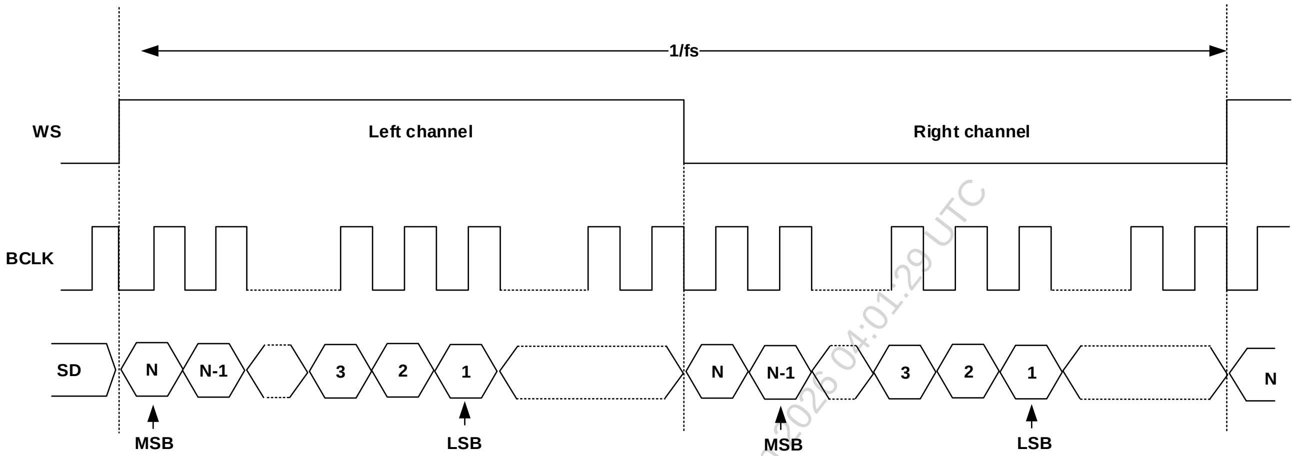


Figure 18. Left-justified timing diagram

12.3. Right-justified Mode Timing

Right-justified timing uses the WS clock to define whether the data is being transmitted for the left channel or for the right channel. The WS is high for the left channel and low for the right channel (requires the WS polarity control bit to be set to 1). A bit clock running at a minimum of 2 • (sample width) • (sample frequency) is used to clock the data.

Data is captured in a 32-bit shift register until the WS toggles. When the WS toggles, the last 32, 24, 16, or 8 bits are transferred to the channel indicated by the previous state of WS. In right-justified mode, the LSB of data is always clocked by the last bit clock before the WS transitions. The data is written MSB first and is valid on the rising edge of the bit clock. All leading bits are ignored.

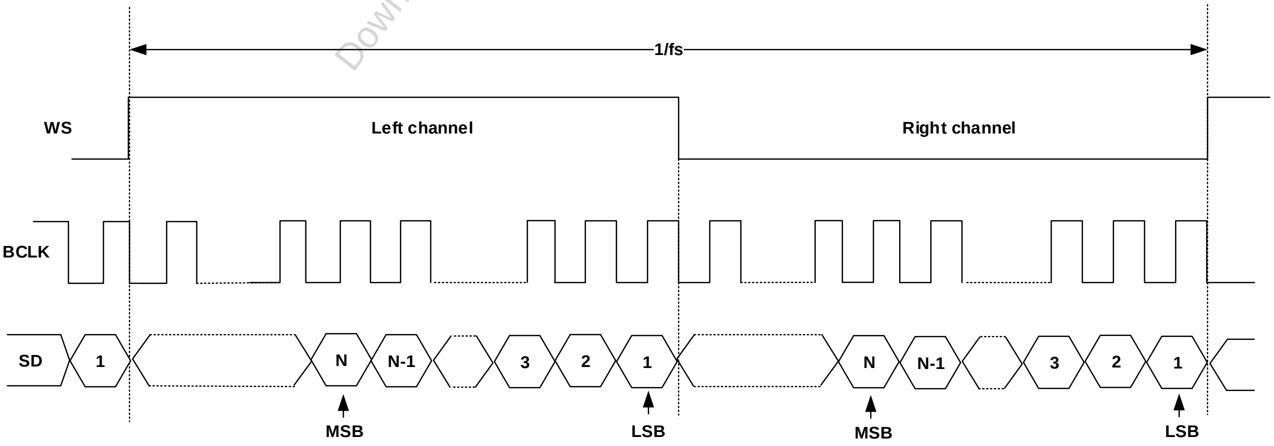


Figure 19. Right-justified timing diagram

12.4. PCM Short-frame Mode Timing

In short-frame mode, the falling edge of PCM_SYNC indicates the start of the PCM word. The PCM_SYNC is one clock long. Data is driven out on the rising edge of PCM_CLK after the PCM_SYNC pulse.

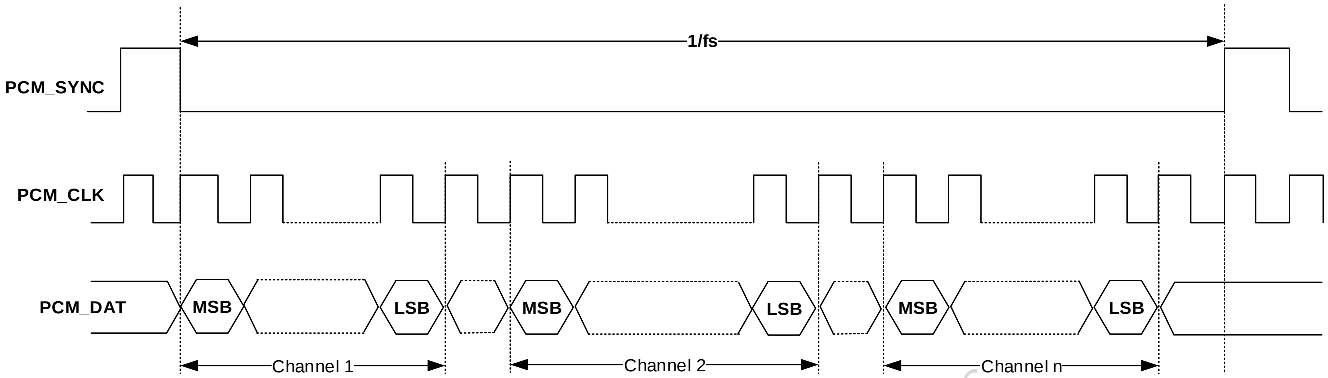


Figure 20. PCM short-frame timing diagram

12.5. PCM Long-frame Mode Timing

In long-frame mode, the rising edge of PCM_SYNC indicates the start of the PCM word. The PCM_SYNC is at least two clocks long. Data is driven out on the rising edge of PCM_CLK coincident with the rising edge of PCM_SYNC.

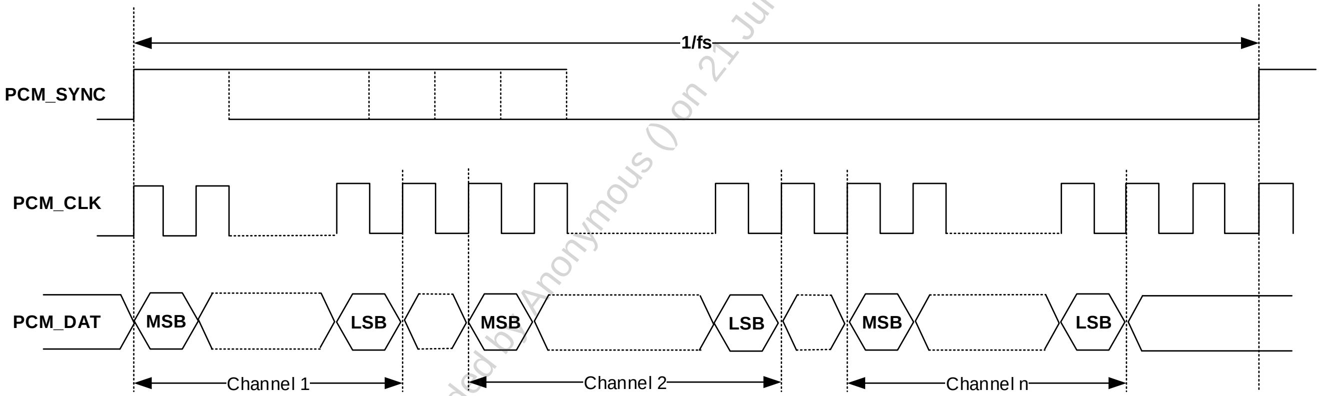


Figure 21. PCM long-frame timing diagram

12.6. PCM Multi-slot Mode Timing

In multi-slot mode, PCM_SYNC can be either long or short. Four words of data can be sent or received. The start of the PCM word position is determined by the length of the sync pulse. Slots are determined by counting data width clocks (8, 16, 24 or 32) from the first PCM word. The PCM mode supports up to four channels. While transmitting, the channel selection should always be from Channel_1.

13. Digital Mic PDM

The SR80 Series device supports up to 8 digital microphones, using four DMIC interfaces. Each interface consists of one output clock and one input data and is typically connected to a pair of digital microphones.

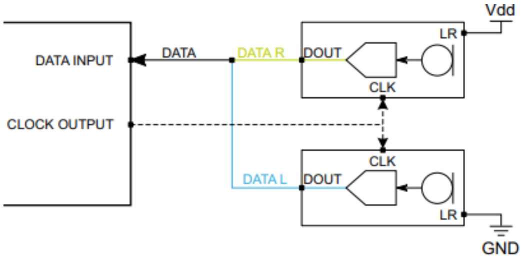


Figure 22. DMIC interface usage

The DMIC clock frequency supported is from 256 kHz to 6.144 MHz.

DMIC interface functionality:

- During the rising edge of the clock the digital microphone with select=0 is active, and the other digital microphone is in high-Z.
- During the falling edge of the clock the digital microphone with select=1 is active, and the other digital microphone is in high-Z.

14. I2C/I3C

The SR80 Series includes the following I^{2}C/I3C interfaces:

- I2C0 Host
- I2C1 Host
- I2C Target
- I3C Host/Target

The I^{2}C target interface and the I3C interface share the same pins so only one mode of operation can be used.

14.1. I2C0 and I2C1 Host

The I^{2}C0 and I^{2}C1 host in the SR80 Series works at up to 400 kHz clock rate (Fast mode) and includes support for clock stretching to pause I^{2}C communication as needed.

14.2. I2C Target

The I^{2}C target interface in SR80 Series is used for control from an I^{2}C host.

The I^{2}C target works at up to 1 MHz clock rate (Fast mode Plus) and implements clock stretching to pause I^{2}C communication as needed.

14.3. I3C Host/Target

The SR80 Series integrates a 2-wire I3C host/target interface for fast boot and control.

At initial boot-up, the interface starts as I^{2}C target and can be switched to I3C during the I^{2}C boot sequence, via a command. After I3C mode is verified, I3C fast boot can be used.

I3C features:

- Various operational modes
  - I3C controller (host or target)
  - I^{2}C target
  - Data transfer to legacy I^{2}C target devices
- Dynamic Address Assignment (DAA)
- Hot-Join feature support
- In-band interrupts (IBI)
- Data rates: FM, FM+, SDR, HDR-DDR
- CRC/parity generation and validation
- Support for broadcast and directed CCC transfers

Note that the SR80 Series I3C interface shares the same pins as the I^{2}C target.

15. 1-Wire PLC Communication

The SR80 Series features a 1-wire interface for communication between two devices, intended for communication using the 5-V charging wire (and GND) while the earbud is inside the charging case. This is also sometimes referred to as power-line communication (PLC). Note that while in 1-wire communication mode, charging is paused until communication mode is exited.

The communication is half-duplex, using a UART-like, software-implemented protocol.

In the transmit direction, one of the PWM LED outputs (*LED_SINK0*) is used as this is high-voltage tolerant pin. In the receive direction, *UART2_RX* is used.

16. Serial Peripheral Interface (SPI) Host

The SR80 Series device features two SPI host interfaces. It supports the following modes:

- Mode 0: CPOL = 0, CPHA = 0
- Mode 3: CPOL = 1, CPHA = 1

The SPI host interface is intended to interface with SPI target devices, such as a serial flash or sensors. The SPI block consists of an 8x32-bit Tx and Rx first in, first out (FIFO) with several registers for control and status. The SPI accommodates various controls for clock polarity, a phase shift of the clock, and target select polarity.

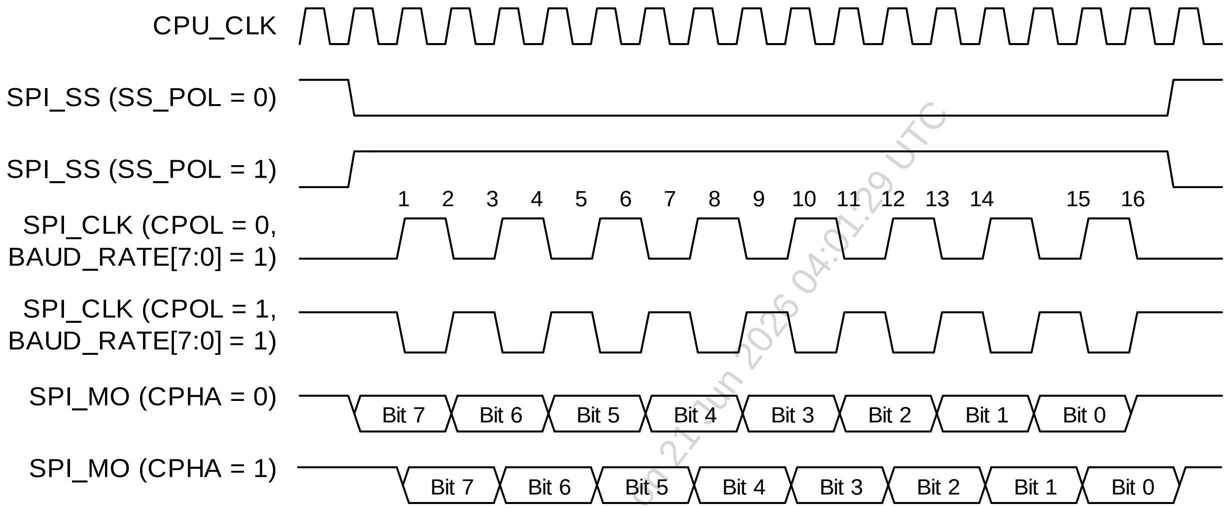


Figure 23. SPI Tx timing

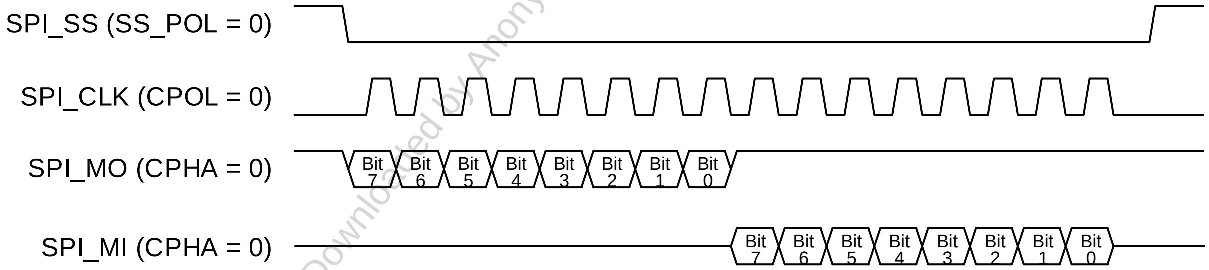


Figure 24. SPI Tx and Rx timing

17. QSPI Host/SPI Target

The SR80 Series features a QSPI host interface which provides a mechanism for accessing external devices (for example, flash memory devices) through a serial bus referred to as a serial peripheral interface (SPI).

The QSPI host interface can also be re-purposed to be a SPI target interface, which can eliminate the need for a dedicated external flash device by booting from an external SPI host, and for control of the SR80 Series.

17.1. QSPI Host

A standard SPI bus utilizes a chip select, a clock, a serial data output and a serial data input signal. The QSPI host interface supports the standard SPI bus, as well as variations of the SPI bus that provide for increased throughput. These variations include the use of multiple (2 or 4) data signals, and the ability to use data signals in a bi-directional fashion.

The QSPI host interface supports clock speeds up to 120 MHz.

The QSPI host interface supports “on-the-fly” AES-256 decryption of flash data for increased security.

The QSPI host module provides four mechanisms for initiating transfers to/from external memory.

- Programmed DMA
    - The module includes an internal DMA engine, which can be programmed to transfer data between on-chip memory and externally attached device(s). This mechanism makes use of an AHB host interface on the module to access on-chip memory through an on-chip AHB bus. This mechanism may be used to transfer data in either direction (from internal memory to external device or from external device to internal memory).
- Pre-load DMA
    - The same internal DMA engine used for programmed DMA is also used to implement a pre-load function. The pre-load function executes automatically after a power-on reset and transfers data from an external device (which should typically be a memory device) to on-chip memory. A data structure stored at the head of the external memory is used to control which data is moved from the external memory, and to what locations in internal memory it is moved.
- Execute in place (XIP)
    - The module includes an AHB-Lite target interface. The module responds to read accesses within a programmable range of AHB address space by retrieving data from the externally attached memory and delivering it through the AHB-Lite interface. This mechanism can be used only to transfer data from an externally attached memory to the internal AHB bus. This mechanism is intended to support software execution directly from the externally attached memory. For optimal performance, a cache (external to the QSPI module) is recommended.

      Note that some flash memories support a special XIP mode, which allows the usual command/instruction byte to be skipped during XIP transfers. This mode is supported by the XIP transfer initiation mechanism interface. However, the other transfer initiation mechanisms (DMA or register-based) may not function correctly while an attached memory device is configured in the special XIP mode.
- Register-based transfers
    - The module includes a register-based interface for initiating individual transfers to/from the external memory.

The QSPI interface supports four modes of operation, MODE0-MODE3. The default mode of operation is in MODE3.

- MODE0
  - Figure 25 illustrates mode 0. In mode 0, the clock idle state is low, and the first data bit of a transfer is captured (by either the host or target) on the first clock transition of the transfer.

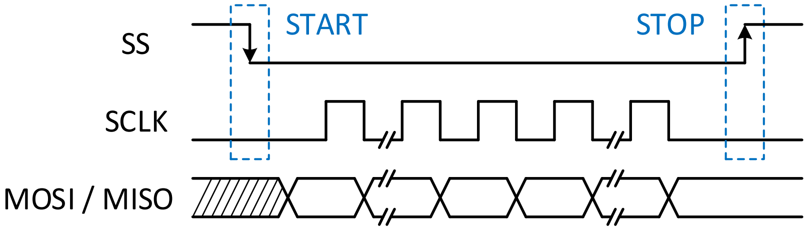


Figure 25. MODE0 timing

- MODE1
  - Figure 26 illustrates MODE1. In MODE1, the clock idle state is low, and the first data bit of a transfer is captured (by either the host or target) on the second clock transition of the transfer.

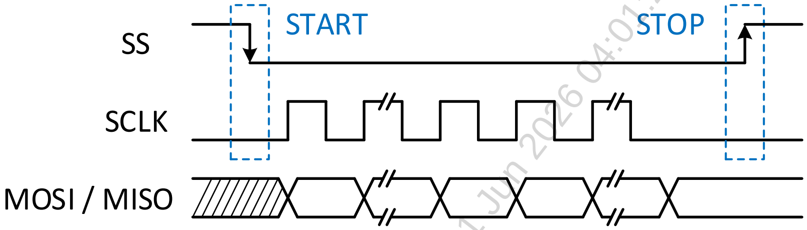


Figure 26. MODE1 timing

- MODE2
  - Figure 27 illustrates MODE2. In MODE2, the clock idle state is high, and the first data bit of a transfer is captured (by either the host or target) on the first clock transition of the transfer.

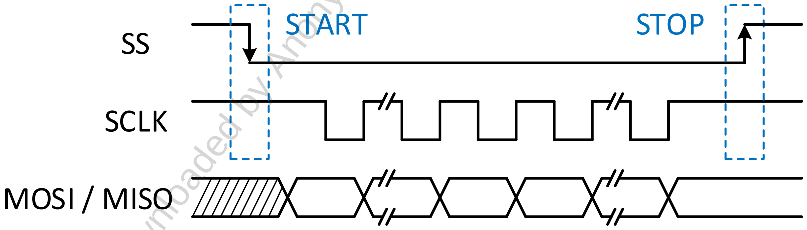


Figure 27. MODE2 timing

- MODE3
  - Figure 28 illustrates MODE3. In MODE3, the clock idle state is high, and the first data bit of a transfer is captured (by either the host or target) on the first clock transition of the transfer.

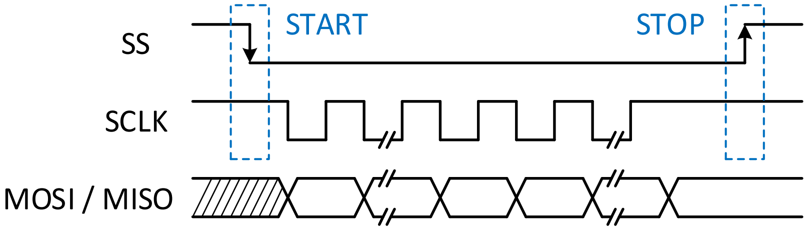


Figure 28. MODE3 timing

Basic, fast, dual output, dual I/O, and quad I/O instructions are supported. In addition, these transfer characteristics are configurable:

- Instruction value
- Address length (bytes)
- Dummy cycles (clock cycles)
- Data length (bytes)
- Single, dual, or quad address
- Single, dual, or quad data

17.2. SPI Target

The SPI target interface can be used by a SPI host for booting and control, enabling the sharing of a single SPI flash memory device.

The following modes are supported:

- Mode 0: CPOL = 0, CPHA = 0
- Mode 3: CPOL = 1, CPHA = 1

18. Flow Control UART

The SR80 Series features three universal asynchronous receiver transmitter with flow control (FC UART), compatible with a standard 16550 UART. Most register bit functions, bit locations within registers, and register base offsets are the same as in a standard 16550 UART. Compared to the 16550, the FC UART operates at a higher clock frequency and provides a flow control mechanism.

- Supports 7-bit data or 8-bit data
- Supports 1 or 2 bit stop bit
- Supports 1-bit odd or even parity
- Supports DMA or CPU channel accessing RX/TX FIFO
- Supports IRDA mode
- The baud rate can be configured by firmware
- Supports flow control

Baud rate and other configuration options are selected using the application framework managed by the CPU subsystem. Most common rates are supported, up to 3 Mbps.

The UART interface can be used for debug (for example, print messages), and for control of other devices in the system.

19. PWM LED Sinks

The SR80 Series integrates 3 high-voltage tolerant current sinks, used to directly drive external LEDs, without the need for external transistors. Each pin can sink up to 20 mA of current.

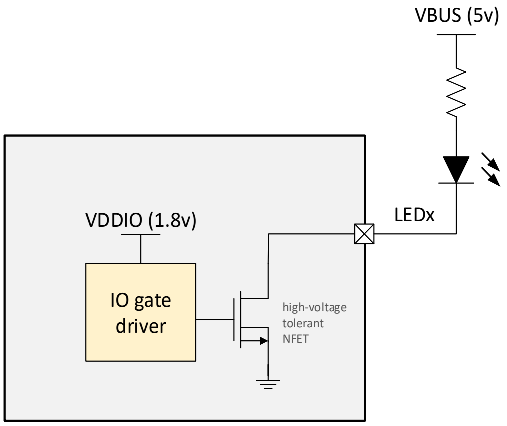


Figure 29. PWM led sink in SR80 Series

- Internal PWM logic is used to control the frequency, duty cycle, and blink rate.
- The maximum PWM frequency is 8 kHz. 8-bit dimming control is applied to the PWM signal.

The SR80 Series also includes a second set of PWM outputs, with standard I/O output capability. This second set is not high-voltage tolerant.

The two sets of PWM outputs are particularly useful for creating differentiated LED lighting for personal and enterprise devices.

20. MADC

The monitor ADC block can be used to detect button presses using a multi-button array and can also be used to measure system voltages. It uses a 10-bit SAR ADC.

The MADC will typically be operated in a power-cycled mode, where it is powered up briefly for a measurement, then powered down again, effectively consuming a small amount of power. The clock for the MADC is 200 kHz, provided by the low-power oscillator (LP_OSC).

The MADC can also be operated in a continuous mode, at ~15 ksps (200 kHz/13).

The measurement range for the MADC is 0 to 1.8 V, with absolute accuracy of +/- 15 mV maximum.

20.1. Multi-button Sensing

The multi-button sense input to the MADC offers the ability to connect multiple switches to the SR80 Series using a single pin. Typically, 1 to 4 buttons are connected using a resistive divider approach where each button momentarily connects a resistor to ground using different resistance values. Various topologies are possible.

The ultra-low-power button-sense input uses a comparator to detect button presses, which then wakes up the ADC for conversion. Firmware can then be used to implement button-press detection, including short and long presses.

20.2. Voltage Sensing

The MADC voltage sense input (at pin MIC0P) can be used for general-purpose voltage monitoring.

21. Power Management

Power is managed by the power management unit (PMU) and firmware running on the Arm M33 CPU.

21.1. Power Supplies

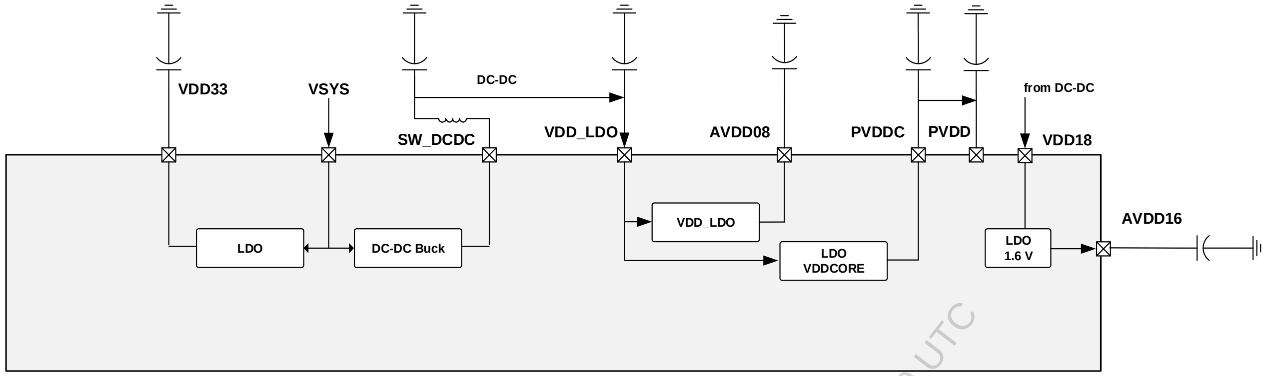


Figure 30. Power supplies in the SR80 Series device

Table 25. Power Rail Supply Summary

Supply Name	Direction	Typical Voltage	Source / Dependency	Primary Usage / Notes
VSYS	Input	3.7 V (battery) / 5.0 V (USB)	External battery or USB VBUS	Main system supply. Feeds DC-DC converter and 3.3-V LDO.
SW_DCDC	Output (switch node)	—	Internal DC-DC converter	Switching node. External inductor and capacitor generate regulated DC output (1.8 V or 1.0 V).
VDD33	Output	3.3 V (USB) / 2.85 V (battery)	Internal 3.3-V LDO from VSYS	Supplies USB PHY and microphone bias circuitry. Voltage programmable by use case.
VDD_LDO	Input	1.8 V or 1.0 V	DC-DC regulated output	Input to core LDO and 0.8-V LDO. Also serves as DC-DC feedback node.
VDD18	Input	1.8 V	External (battery mode) or DC-DC (USB mode)	Input to 1.6-V LDO and I/O/HP driver supply. Must be externally supplied in 1.0-V DC-DC battery mode.
AVDD16	Output	1.6 V	Internal 1.6-V LDO from VDD18	Supplies analog circuits (ADC, DAC, analog front-end).
AVDD08	Output	0.8 V	Internal 0.8-V LDO from VDD_LDO	Supplies PLL and high-frequency RC oscillator (HF-RCOSC).
PVDDC	Output	0.8 V (programmable)	Internal core LDO from VDD_LDO	Core voltage rail for digital processing blocks.
PVDD	Input	Same as PVDDC	From PVDDC	Direct supply input to processing cores.

21.2. Power Domains

There are three primary power domains in SR80 Series:

- M33 MCU power domain
- HiFi 5, NPU power domain
- DSP subsystem power domain (CAPE 2 and LLE cores)

21.3. Power States

Power states are primarily defined in firmware and managed by the CPU using the PMU and subsystem control registers. Power-on and wake from low power states are managed directly in hardware before transitioning to processor control. Power management uses a fine-grained approach to configure functional blocks as needed to perform the tasks at hand. This functionality not only allows adjusting the state of resources to handle the needed application tasks but also allows supporting applications with varying performance (quality/power) levels, for example low-power audio playback and high-quality audio playback.

21.4. Power Sequencing

21.4.1. PMU_EN

The Power Management Unit Enable (*PMU_EN*) pin is used to enable the internal power management. After VSYS is applied, the *PMU_EN* pin is **latched once** when it becomes logic *high*, enabling the device to come out of reset. Note that after this initial latching of *PMU_EN*, the pin simply becomes an input to the SR80 Series firmware. That is, a logic *low* at the pin does not automatically disable the internal power management.

PMU_EN can be connected directly to VSYS. Internally, the power management logic sequences the various power blocks to limit in-rush current.

21.4.2. POR_BYPASS

This pin should be tied to GND during normal use. It is intended for debug purposes, and for production testing of the SR80 Series.

22. System Overview and Application Diagrams

22.1. SoC Connectivity Overview

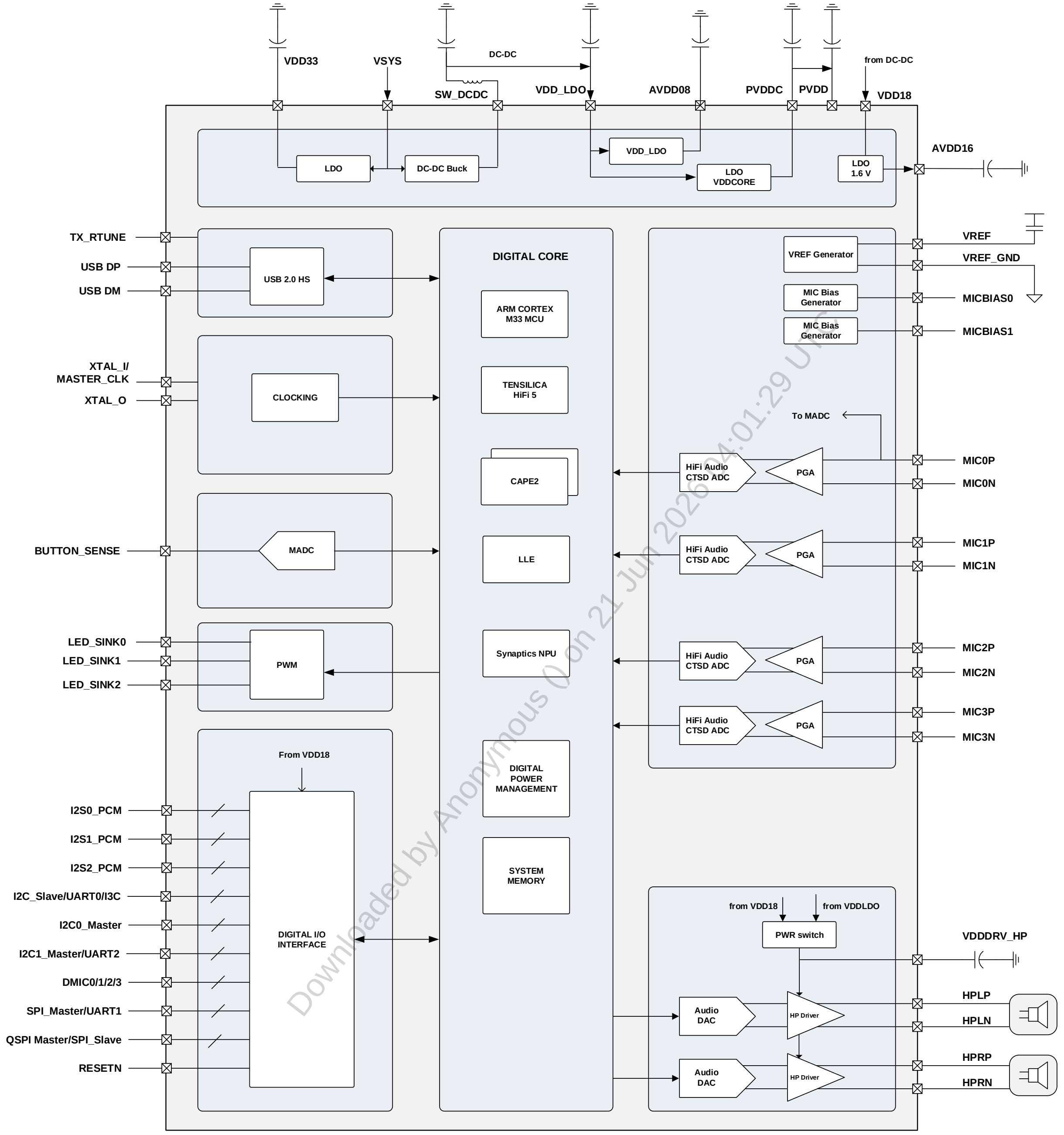


Figure 31. SoC Connectivity Overview

22.2. SR80 Series General Applications

- Advanced ANC headsets
- Office Unified Communications headsets
- Gaming headsets
- True-wireless stereo (TWS) headsets
- Wired USB headsets
- Speakerphones
- Bluetooth speakers
- USB microphones

22.3. Application Diagram with Two Stereo Speakers

Figure 32 illustrates the SR80 Series in electronic devices.

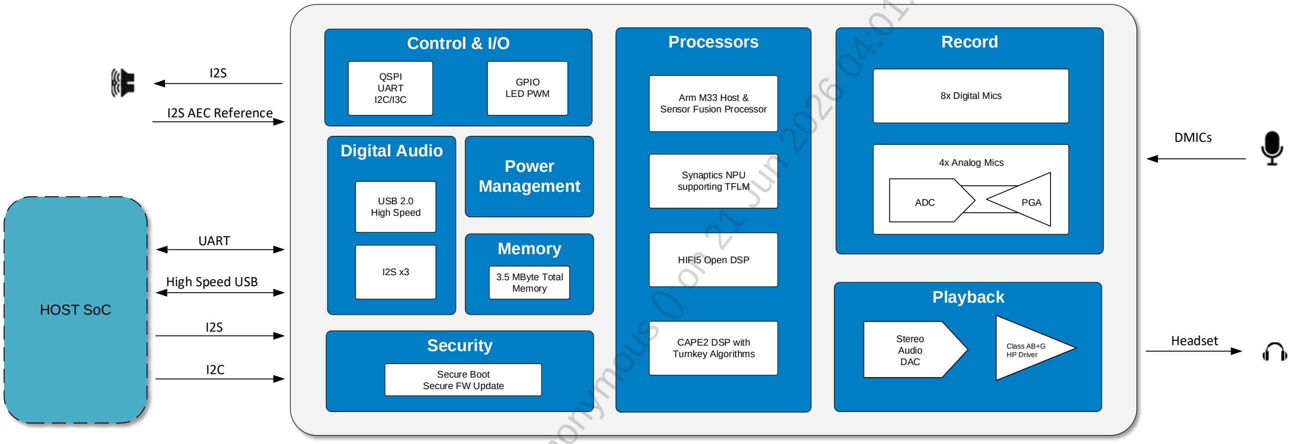
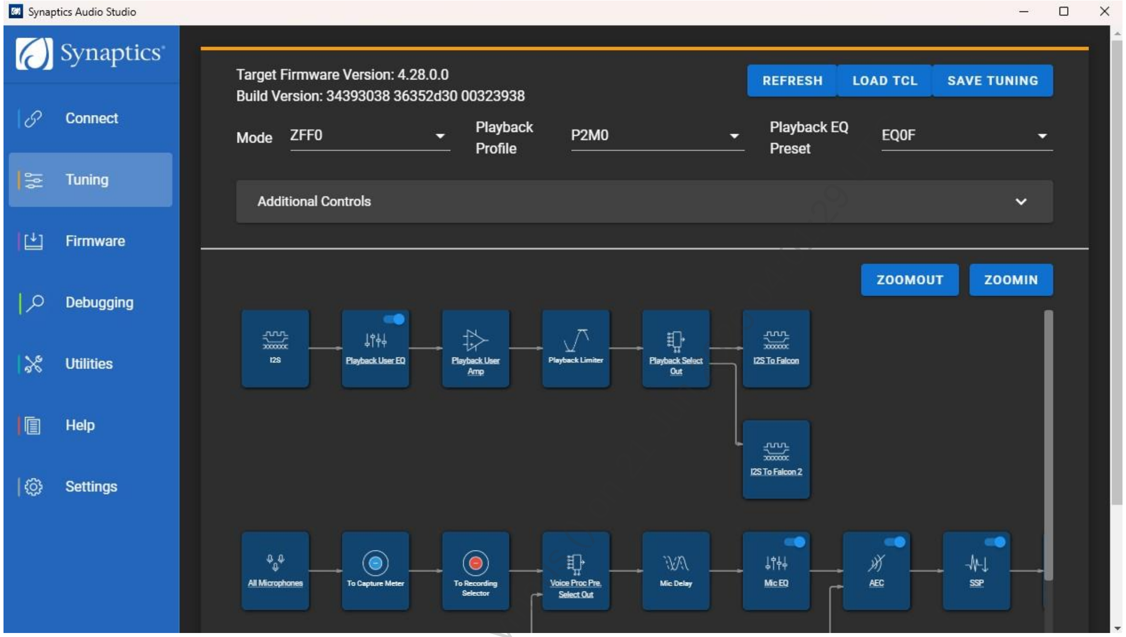


Figure 32. Electronic device application diagram with 2 stereo speakers (4 speakers optional)

22.4. Synaptics Audio Studio Application

The SR80 Series device is supported by the Synaptics Audio Studio application for tuning and configuring advanced audio processing and AI features.

- Graphical user interface
- Supports real time tuning, offline mode and firmware customizations
- Customizable memory layout
- Customizable DSP pipeline
- Easy to tune customer & third-party DSP modules



Target Firmware Version: 4.28.0.0
Build Version: 34393038 36352d30 00323938

Mode ZFF0
Playback Profile P2M0
Playback EQ Preset EQ0F

Figure 33. Synaptics Audio Studio application

Applications

- High-Performance Doorbells
- Intercoms
- Security Cameras & Panels

23. Mechanical and Package Information

23.1. Package Drawing and Dimensions

23.1.1. WLCSP-76 Package

The SR80 Series is available in 76-ball WLCSP package, with 0.35 mm ball pitch. Package dimensions are 3.08 mm x 3.20 mm. Full dimensions for the package are shown in Table 26.

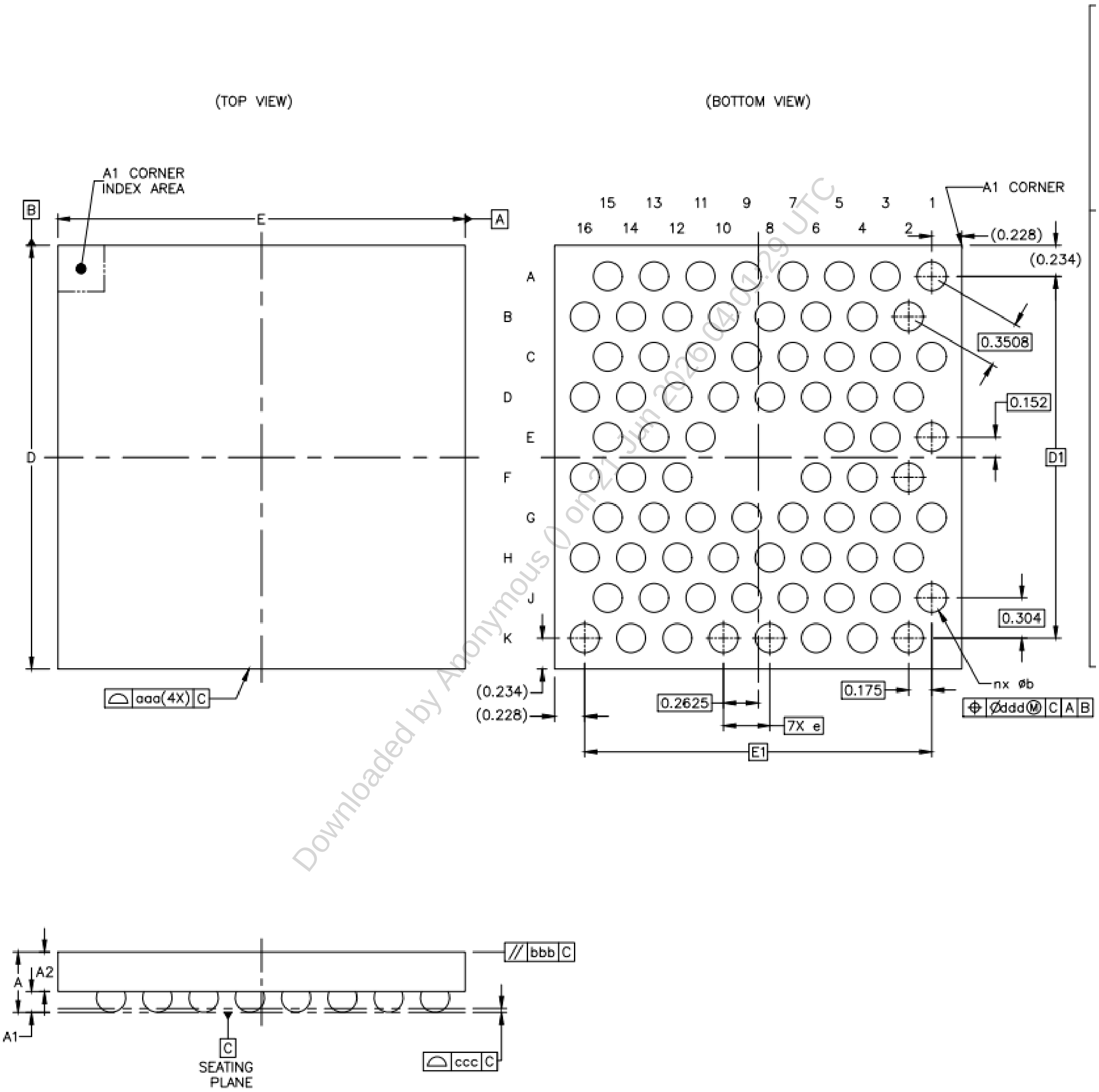


Figure 34. WLCSP package drawing for SR80 Series (units in mm)

Table 26. WLCSP Package Dimensions (in mm)

		Symbol	Common Dimensions		
			Min.	Nom.	Max.
Total Thickness		A	0.432	0.457	0.482
Standoff		A1	0.137	0.157	0.177
Wafer Thickness		A2	0.285	0.3	0.315
Film Thickness		A3	—	—	—
Body Size	X	E	3.0809		
	Y	D	3.2039		
Ball Bump Pitch	X	SE	—		BSC
	Y	SD	—		BSC
Edge Ball Center to Center	X	E1	2.625		BSC
	Y	D1	2.736		BSC
Pitch		e	0.35		BSC
Ball Diameter (Size)			0.2		
Ball/Bump Width		b	0.19	0.22	0.25
Ball/Bump Count		n	76		
Package Edge Tolerance		aaa	0.03		
Wafer Flatness		bbb	0.06		
Coplanarity		ddd	0.03		
Ball/Bump Offset (Package)		eee	0.015		

23.1.2. LGA-76 Package

The SR80 Series is also available in 76-ball LGA package. Package dimensions are 6.00 mm x 6.50 mm. Full dimensions for the package are shown in Table 27.

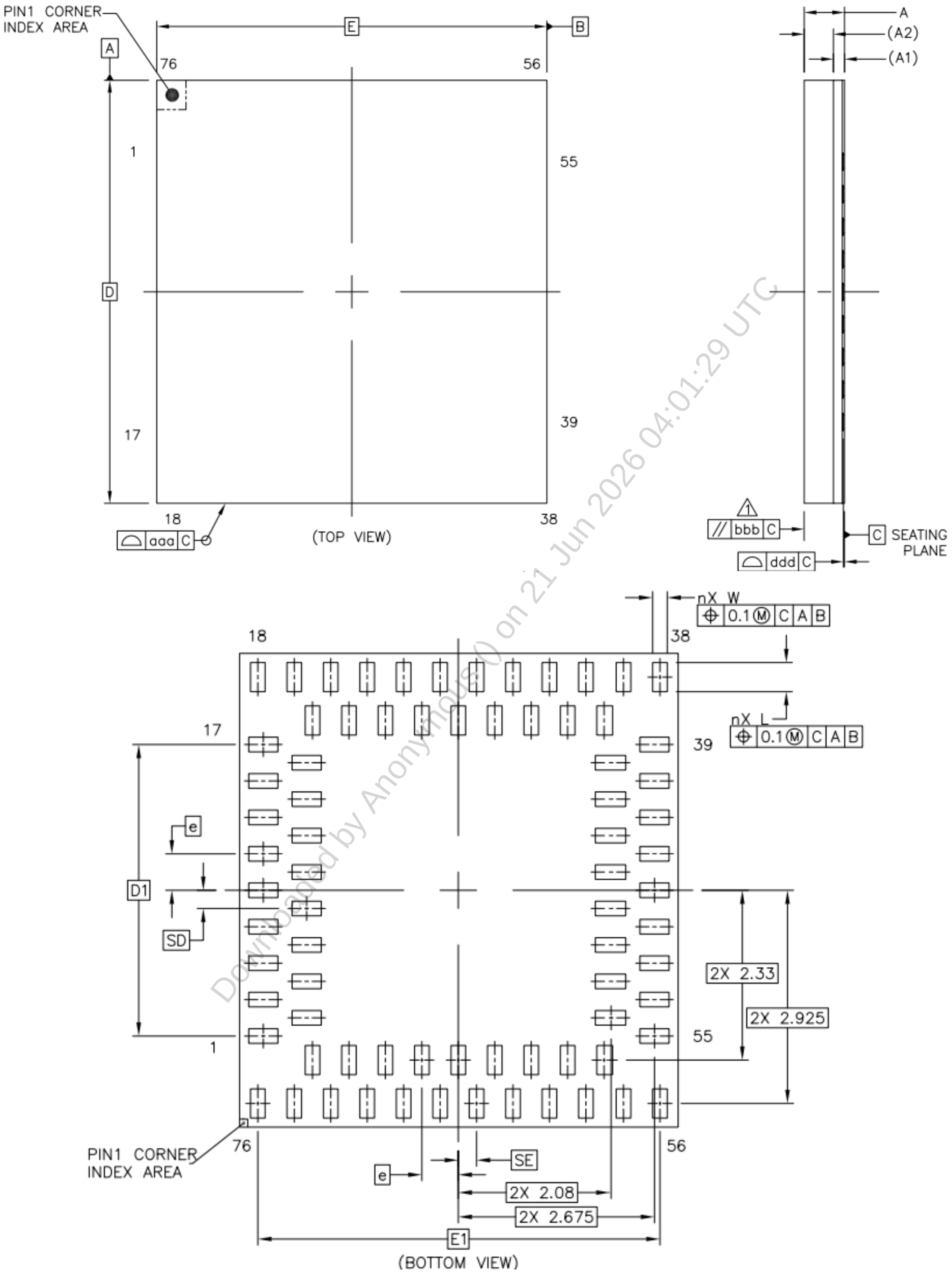


Figure 35. LGA package drawing for SR80 Series (units in mm)

Table 27. LGA Package Dimensions (in mm)

	Symbol	Common Dimensions		
		Min.	Nom.	Max.
Total Thickness	A	0.57	0.62	0.7
Substrate Thickness	A1	0.17		REF
Mold Thickness	A2	0.45		REF
Body Size	D	6.5		BSC
	E	6		BSC
Lead Width	W	0.15	0.2	0.25
Lead Length	L	0.35	0.4	0.45
Lead Pitch	e	0.5		BSC
Lead Count	n	76		
Edge Lead Center to Center	D1	4		BSC
	E1	5.5		BSC
Body Center to Contact Lead	SD	0.25		BSC
	SE	0.25		BSC
Pre-Solder		—	—	—
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.2		
Coplanarity	ddd	0.08		

23.2. Package Thermals

Table 28. Thermal specifications

Parameter	Symbol	Minimum	Typical	Maximum	Units
Thermal resistance[1, 2] (four layer)	θ_{JA}	—	37	—	°C/W
Junction Operating Temperature	TJ	0	—	125	°C
Ambient Operating Temperature	TA	-10	—	85	°C

1. For a given power dissipation, die temperature can be calculated as follows: $T_J = T_A + (\text{power dissipated} \cdot \theta_{JA})$.
2. ΘJA uses a 4-layer 139.7 x 109.2 x 1.6 mm 2s2p test board.

Note: SR80 Series package is MSL1 (Moisture Sensitivity Level 1), indicating minimal sensitivity and no special handling requirements.

24. Part Numbering and Marking

24.1. Part Order Numbering

Table 29 lists the SR80 Series part numbers and their corresponding applications.

Table 29. SR80 Series Part Order Options

Product Name	Part Number[1]	Cores	Package Type
SR82	SR82A1-LA0000-T000-R	MCU-CM33, DSP-CAPE2, LLE	LGA-76
	SR82A1-WC0000-T000-R		WLCSP-76
SR85	SR85A1-LA0000-T000-R	MCU-CM33, DSP-CAPE2, LLE and HiFi5	LGA-76
	SR85A1-LA0000-T000-R		WLCSP-76
SR88	SR88A1-LA0000-T000-R	MCU-CM33, DSP-CAPE2, LLE, HiFi5 and NPU	LGA-76
	SR88A1-WC0000-T000-R		WLCSP-76

1. T=Tray, R=Tape & Reel

24.2. Package Marking

Figure 36 illustrates a sample package marking and Pin 1 location for an SR80 Series device.

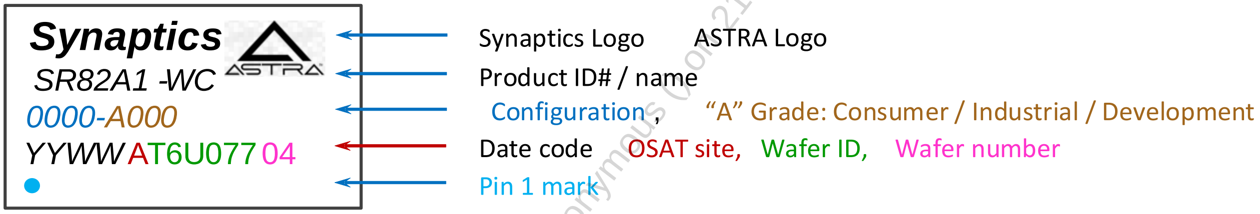


Figure 36. Package Marking and Pin 1 Location

24.3. Part Number Decoder

The following examples illustrate part numbers and their decoding process.

Example 1: SR82A1-LA0000-T000-R

Example 2: SR82A1-WC0000-T000-R

SR82: Chip name
A1: Revision name
LA: Package type: LGA76
WA: Package type: WLCSP76
0000: Reserved for SW/Model/Algo Licensing
A000: Full feature engineering sample part
V000: Reserved for Automotive part
H000: Reserved for Industrial part
T000: Consumer part

Note: The same decoding method applies to all SR85/88 part numbers.

25. References

Other related reference documents:

- I²C Specification: https://www.nxp.com/docs/en/user-guide/UM10204.pdf
- I3C Specification: https://mipi.org/specifications/i3c-sensor-specification

26. Revision History

Date Modified	Revision	Description
February 25, 2026	1	Initial release.
March 2, 2026	A	Production release.
April 28, 2026	B	Updates to the following: • 2 Features (Processing Subsystems) • 2.1 Overview • 2.1.3 HiFi 5 DSP Subsystem (Hardware features) • 7.1 Hardware (added Compute throughput) • 8.3 CAPE 2 • 9 Synaptics NPU
May 11, 2026	C	Replaced incorrect 79-pin image with correct 76-pin image in Figure 2. SR80 Series pin assignment (package balls facing down).

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