SL2610 Product Line of Embedded Processors

Electrical Specification

Overview

The Synaptics Astra™ SL Series of IoT processors are highly integrated AI-Native Linux® and Android™ systems on chip (SoCs) optimized for multimodal consumer, enterprise, and industrial IoT workloads with hardware accelerators for edge inferencing, security, video, graphics, and audio. The SL2600 series expands the portfolio with the introduction of 5 SoC families within the new SL2610 product line - the SL2611, SL2613, SL2615, SL2617 and the SL2619.

The SL2610 product line delivers unmatched price performance with multimodal, AI-native processing for IoT applications, enabled through a high-performance compute subsystem with Arm® Cortex®-A55 and Cortex®-M52 with Helium™ cores, transformer-capable NPUs with up to one TOPS inferencing, and 3D GPUs with OpenGL® and Vulkan® support.

The SL2610 Product Line introduces the Synaptics Torq™ Edge AI platform featuring the Torq T1 NPU and the industry's first production implementation of the RISC-V-based Coral NPU Machine Learning (ML) core from Google. With built-in hardware acceleration for transformers, the T1 delivers up to 1 TOPS inferencing with 512 parallel compute elements composed of dual 256 MAC units, supporting int8, int16, and BFLOAT16 data types. By leveraging flexibility of the RISC-V core, this integrated architecture allows for dynamic support of new operators, enabling real-time processing of vision, audio, and sensor fusion workloads to future-proof IoT AI system design. Torq promotes a developer-first approach, delivering an open-source Edge AI compiler and runtime based on IREE/MLIR.

The System Manager (SM) ultra-low-power subsystem supports an MCU-first approach for boot-up, thus allowing for fine-grained, on-demand control over the functional domains of the SL2610 line of SoCs. It operates independent of the Cortex-A55 application cores and is optimized to manage essential system functions during standby and low-power states. The SM integrates an Arm Cortex-M52 processor (running at up to 200 MHz) with its own tightly coupled memory and a suite of autonomous peripherals, enabling real-time control, secure management, and event-driven wakeup—even when the application core domain is powered down.

Designed for PSA Level 3 Root of Trust (RoT) component, the SoCs help build a robust device edge, shielded from sophisticated software, side-channel, and physical attacks. A balanced set of integrated IO and connectivity features such as MIPI-CSI/DSI interfaces, Gigabit Ethernet, 1588 TSN, CAN, and advanced power management, deliver scalable compute across consumer and industrial-grade systems, establishing a new benchmark in secure AI-native processing for the device edge.

The SL2610 product line of SoCs supports the Synaptics Astra IoT platform, delivering a unified experience through standards-based approaches, open software frameworks, full-featured AI toolkits, and market-ready evaluation systems.

In combination with Synaptics' best-in-class wireless connectivity portfolio, the SL2610 product line enables cost-optimized system solutions with disruptive performance-per-watt benefits for the IoT.

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1. Block Diagram

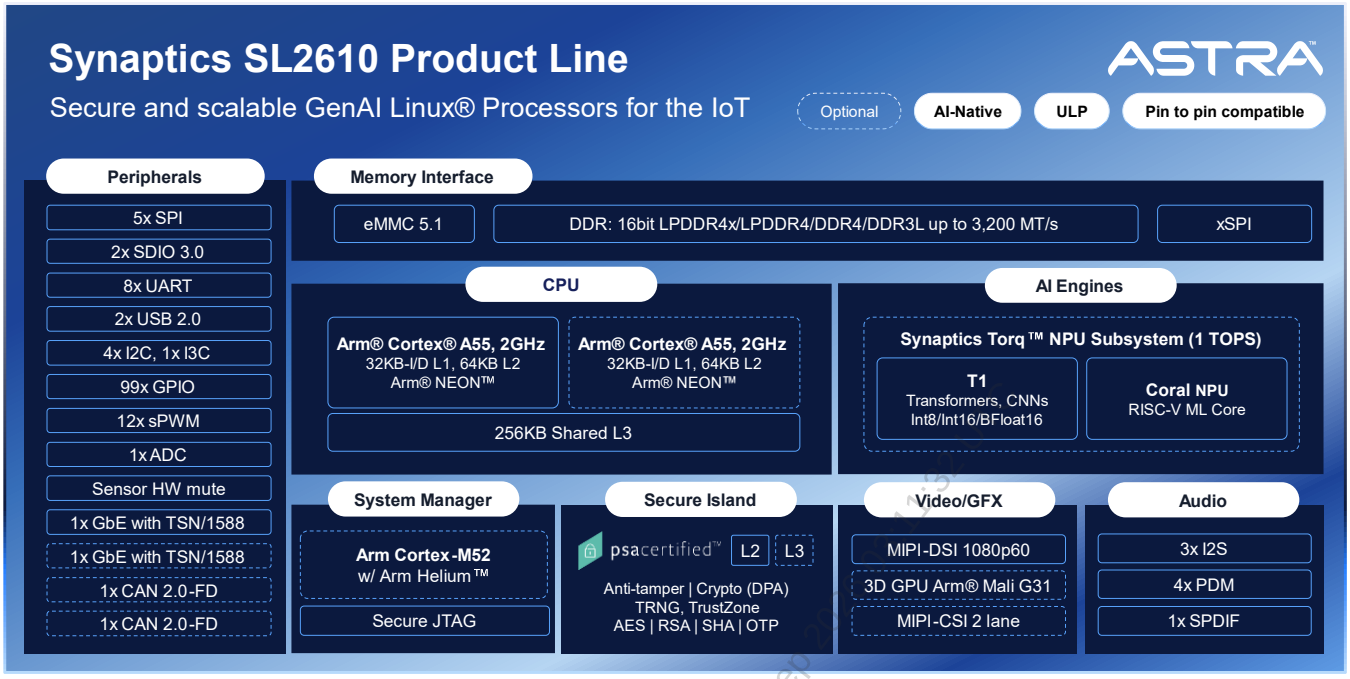

Figure 1. SL2610 Product Line of SoCs high-level block diagram

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2. Features

2.1. CPU

- Dual-core Arm® Cortex®-A55 processor
- Up to 2.0 GHz per core[1]
  - Supports per-core power gating. Dynamic voltage/frequency scaling (DVFS) applies to the entire A55 CPU subsystem (not per-core)
- 32KB I-Cache / 32KB D-Cache, 64KB L2 Cache per core
- Shared 256KB L3 Cache
- Dedicated NEON™ and FPU per core
- Arm® CoreSight™-compatible debug interface
- TrustZone® technology with Synaptics TEE software
- Supports standard toolchains (ARM, GNU)

2.2. Security

- Fully firewalled secure CPU
- Secure boot with RSA digital signature verification from eMMC/xSPI
- On-chip 32 Kbit anti-fuse OTP
- True random number generator
- Hardware accelerators for AES, RSA, SHA, ECC and HASH
- JTAG access control through authentication
- Memory and I/O space access control
- SynaPROT support
- Designed for PSA Level 3 certification RoT component
- Secure access for Arm Cortex®-M52 and A55 processors
- Anti-tamper protection

2.3. NPU

- Synaptics Torq™ NPU for localized neural network/machine learning applications
  - Up to 1 TOPS
- HW support of transformers
- Vision, audio and sensor fusion workloads
- Support for int8, int16, and BFLOAT16 data types
- An integrated Coral NPU RISC-V core allows for arbitrary layer execution
- Utilizes MLIR-based open-source IREE compiler that allows easy targeting of customer networks to NPU
- Supports TensorFlow™ Lite inferencing via the SyNAP™ toolkit

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[1] All parts are designed to operate up to 2GHz through DVFS feature. If application requires continuous operation at 2GHz, reach out to Synaptics team for a software update.

2.4. Low Power Processor

- Arm® Cortex®-M52 processor
- Up to 200 MHz
- 64 KB ROM
- 256 KB RAM with ECC

2.4.1. Standby Mode System Manager

- SM CPU with SynaPROT support
- xSPI with 2x Chip Selects, 2x TWSI (I^2C) interfaces, 1x SPI interface, Integrated temperature sensor, and JTAG for debugging
- Multiple GPIOs available in standby mode for low-power operation
- Up to 12x Smart PWMs (sPWMs), 1 x ADC (8 channels), and 2x CAN-FD interfaces
- I3C host and target interfaces, 2x PDM interfaces
- Four UART interfaces in the SM domain
- 7x WDT (3 in SoC domain, 3 in SM domain, 1 in AON domain)
- 22 Timers total: 16 in SoC domain, 5 in SM domain, 1 in AON domain
- Supports 32 kHz for buffered output

2.5. GPU

- 3D GPU Mali™-G31
- Single-pixel shader core with one execution engine
- Supports display resolutions up to Full HD 60 fps
- Clock frequency up to 800 MHz
- Supports OpenGL® ES™ 3.2, OpenCL™ 3.0, EGL™ 1.5, Vulkan® 1.3

2.6. Memory Interface

- DRAM Controllers
  - 16-bit DDR3L-1866, DDR4, and LPDDR4x-3200 support
  - Spread Spectrum Clocking
  - Inline ECC support
  - Retention support
  - DDR3L: Up to 1GB, single rank
  - LPDDR4/4x: Up to 2GB, single rank, single channel
  - DDR4: Up to 4GB, single rank
  - Out-of-order transaction issue to optimize DRAM utilization
- eMMC 5.1 Controller
  - x1, x4, or x8-bit interface

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2.7. Video / Display Interfaces

- Dual display
  - Simultaneous SPI and MIPI displays with different content
- MIPI DSI®
  - 4-lane DPHY
  - Supports command mode and video mode
  - Up to 1080p60 resolution and refresh rate

2.8. Audio / Video Input

- MIPI CSI RX in SoC domain
  - One 2-lane interface
  - Supports up to 2160p30 resolution
  - HDR camera support
  - Maximum up to 1.5 Gbps
  - Two virtual channels
  - Multidrop support
- Digital Image Interface (DII)
  - 8-bit parallel camera interface
  - Supports up to 1 Megapixel at >15 fps
- TDM/I2S Interface
  - Three fully bidirectional interfaces, each supporting up to 16 channels
  - Supports sample rates of 8, 96, 192, and 384 kHz with slot sizes of 8, 16, 24, or 32 bits
  - At 192 kHz, TDM interface supports up to 8 channels
- Supports external MCLK input to the audio subsystem or provides internal MCLK output for an external codec
- Support up to 8 digital mics: 4× PDM stereo interfaces in the SoC domain, or 1× PDM stereo interface in the SM domain (not concurrent)
- Dedicated audio DMA supporting TDM, I2S, and PDM
- Hardware audio mute and camera mute support via dedicated control pins

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2.9. Peripherals

Note: Peripherals are accessible from both the SM and SoC domains.

- Two USB 2.0 interfaces in the SoC domain
- Two SDIO 3.0 ports in the SoC domain
  - One SDIO 3.0 port, up to 200 MHz single data rate (SDR104), 1.8V only
  - Second SDIO supports up to 100 MHz operation with 1.8V I/Os only
- Four TWSI 2-wire buses (I^2C compatible)
  - Two TWSI interfaces in the SM domain
  - Two TWSI interfaces in the SoC domain
- 8 UARTs:
  - Four high-speed UART interfaces in the SoC domain
  - Three high-speed UARTs and one low-speed UART interface in the SM domain

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- 5 SPI controllers (up to 50 MHz Host / 25 MHz Target)
  - One SPI in the SM domain supports Controller or Target mode
  - Four SPIs in the SoC domain
  - Each interface supports up to four target devices
- xSPI with 2 Chip Selects in the SM domain
  - Supports up to 8-bit data at 150 MHz DDR
  - 1.8V I/Os only
  - Compatible with 4-byte addressing Serial NOR and NAND (up to 8-bit)
- 99 shared GPIO pins
  - 39 GPIOs in the standby domain, including 5 Always-On (AON) that support wakeup
  - Remaining GPIOs in the SoC domain
- Rectangular Keyboard matrix controller supporting up to 80 keys (8x10)
- Up to 12 sPWM (smart PWM) modules in the SM domain, each with:
  - Up to 12 counters
  - Seven selectable operating modes:
    - Timer/Counter with Compare/Capture
    - Quadrature Decoding
    - sPWM / Stepper Motor Control (SMC) for pointer instruments
    - sPWM with Dead Time / Three-Phase Motor Control (e.g., BLDC)
    - Pseudo-Random sPWM
    - Shift Register Mode
  - 16-bit or 32-bit counters
  - Up, down, and up/down counting modes
  - Clock Pre-scaling
  - Two capture and compare functions
  - Double buffering for compare/capture and period registers
  - Two output trigger signals
  - Interrupt support on Terminal Count and Capture/Compare
- ADC in the SM domain
  - 11-bit resolution
  - Up to 5 MS/s sampling rate
  - Up to eight dedicated single-ended inputs
  - Full-scale 1.8V (VREF= 1.2V or VREF = 1.8V with external supply)
- On-chip temperature sensor
- 2x Control Area Network (CAN-FD)
  - Conforms with CAN Protocol 2.0 A, B and ISO11898-1
  - Full CAN FD support (up to 64 data bytes)
  - Parity/ECC check for Message RAM
  - Speed up to 8 Mbps
  - Time synchronization support
  - No PHY on-chip
  - CAN-PHY 1.8V I/O interface

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- Ethernet
  - 2x 802.3 (G)MAC with RGMII and RMII interface support
  - MDIO host interface for external PHY/switch configuration
  - IEEE 802.3az Energy Efficient Ethernet compliant
  - LAN wake-up frame (magic packet) detection
  - MAC statistics support
  - IEEE 1588 PTP for accurate timestamping
  - IEEE 802.1AS-Rev (AVB/TSN) support
  - Hardware-based 802.1 p/q VLAN tagging
  - 25 MHz clock output

2.10. Boot Options

- eMMC, xSPI (xSPI NOR and xSPI NAND), USB

2.11. JTAG

- CoreSight™ Debug support
- Boundary scan support

2.12. Power Saving

- Power gating for each A55 core
- DDR self-refresh support
- Power gating for GPU
- Power gating for NPU
- Dynamic Voltage and Frequency Scaling (DVFS)

2.13. Package and Layout

- Package: 13 mm x 12 mm FCBGA Type, 0.4 mm ball pitch (effective 0.8 mm ball pitch)
  - Ball pattern allows standard PCB fab rules (no HDI rules required)

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Table 1. SL2610 Product Line Feature Summary

PRODUCT FAMILY / FEATURES	SL2611	SL2613	SL2615	SL2617	SL2619
Compute Engines					
Arm-Cortex A55 CPU	Single Core	Single Core	Dual Core	Dual Core	Dual Core
Arm-Cortex M52 MCU	Optional	Yes	Optional	Yes	Yes
NPU	No	Optional	Optional	Yes	Yes
GPU	No	Optional	Optional	Yes	Yes
Memory					
A55 caches	32KB I$ + 32KB D$ L1 / 64KB L2 / 256KB L3				
M52 on-chip memory	512KB (optional)	512KB	512KB (optional)	512KB	512KB
Program/Data	xSPI/eMMC				
DDR3L/DDR4/LPDDR4/4x	16-bit data, up to 4GB				
Inline ECC	No	Optional	No	Optional	Yes
Security					
PSA L2	Yes				
PSA L3[1]	No	Optional	No	Optional	Yes
Sensor HW mute	Yes				
Peripherals					
Display	No	1x MIPI DSI (optional)	1x MIPI DSI (optional)	1x MIPI DSI	1x MIPI DSI
	1x SPI				
MIPI-CSI	No	Optional	No	Optional	Yes
CAN	Optional	Optional	Optional	Optional	Yes
1st GbE	Yes				

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PRODUCT FAMILY / FEATURES	SL2611	SL2613	SL2615	SL2617	SL2619
2nd GbE	No	No	Optional	No	Yes
GPIO	99				
I2S	3				
SPDIF	1				
SDIO 3.0	2				
USB 2.0	2				
Smart PWM	12				
ADC	11 bit, 5 Msps				
UART	8				
I2C	4				
SPI	5				
I3C	1				
PDM	4				
Grade & Package					
Package	13x12 FCBGA, pin-to-pin compatible				
Consumer	Yes (T_A 0 to +70 ° C / T_J -40 to +85 ° C)				
Industrial	Yes (T_A -40 to +85 ° C / T_J -40 to +125 ° C)				

1. Designed for PSA Level 3 certification.

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2.14. Related Content

Part Number	Document Title
506-001443-01	Synaptics General Guide for Soldering SMD to PC Boards Application Note
506-001454-01	Synaptics General ESD/EOS Control Methods Application Note

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3. Pin Information

3.1. Pin Assignments

Note: Due to the high pin count, the package is illustrated across multiple pages (Figure 2 through Figure 7).

	1	2	3	4	5	6	7	8	9	10	11	
A		VSS	GPIO[27]			GPIO[29]			GPIO[40]		VSS	A
B	VSS	GPIO[28]	GPIO[24]	GPIO[23]		GPIO[30]	GPIO[32]		GPIO[36]	GPIO[37]	GPIO[41]	B
C		M0_DQ[8]			GPIO[26]	GPIO[25]	GPIO[31]	GPIO[33]	GPIO[35]			C
D	M0_DQS1n	M0_DQS1p	VSS	M0_DM[1]					VSS		GPIO[39]	D
E		M0_DQ[9]				VSS	VDD_CORE_FB					E
F	M0_DQ[13]	M0_DQ[10]	M0_DQ[14]	M0_DQ[11]				CPUPLL_AVDD1P8		GPIO[34]	VSS	F
G	M0_DQS0p	M0_DQS0n	VSS	M0_DQ[15]		M0_DQ[12]		VSS				G
H		M0_DQ[0]										H
J	M0_DQ[1]	M0_DQ[5]	M0_DQ[2]	VSS	M0_DQ[3]	M0_DM[0]		VSS	VDDQ	VSS	VSS	J
K		M0_DQ[4]										K
L		M0_DQ[6]	VSS		M0_ODT	M0_DQ[7]		VSS	VDDQ	VDDQLP	VDDQLP	L
M	M0_CSn	M0_RASn	M0_CKn									M
N			M0_CKp	VSS	M0_WEn	M0_CKE		M0_CAL	VSS	VDDQ		N
P	M0_BG[1]	M0_CASn									VSS	P
R		M0_BA[1]	M0_A[5]	M0_A[12]		VSS		VSS	VDDQ			R
T											VDDQ	T
U	M0_A[13]	M0_A[10]	M0_A[7]	VSS		M0_ACTn	M0_BG[0]	VSS	VDDQ		VSS	U
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. Top View (1 of 6)

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Note: Due to the high pin count, the package is illustrated across multiple pages (see Figure 2 through Figure 7).

	1	2	3	4	5	6	7	8	9	10	11	
V		M0_A[4]	M0_BA[0]									V
W			M0_A[0]	VSS		M0_A[3]	M0_A[1]	VSS	VDDQ	VDDQ	VSS	W
Y	M0_A[6]	M0_A[9]				VSS						Y
AA		M0_A[8]	M0_A[2]	M0_RSTn		M0_AVDD1P8		VSS		VSS	VSS	AA
AB			M0_A[11]		VSS							AB
AC	USB2_1_VBUS	USB2_1_Dn	VSS		USB2_1_DVDD		VSS		VSS		VSS	AC
AD		USB2_1_Dp	USB2_1_VR_AVDD3P3	VSS	USB2_1_AVDD3P3		USB2_0_DVDD		USB2_0_AVDD3P3		eMMC_VDDIO1P8	AD
AE	USB2_1_REXT	USB2_0_Dn							USB2_0_VR_AVDD3P3	VSS		AE
AF		USB2_0_Dp	VSS		VSS	eMMC_DAT[3]	eMMC_CMD			eMMC_DAT[4]		AF
AG	VSS	USB2_0_REXT	eMMC_DAT[0]		eMMC_DAT[1]		eMMC_CLK	eMMC_RSTn	eMMC_DAT[5]	eMMC_DAT[7]		AG
AH		USB2_0_ID	USB2_0_VBUS		eMMC_DAT[2]			eMMC_STRB		eMMC_DAT[6]		AH
	1	2	3	4	5	6	7	8	9	10	11	

Figure 3. Top View (2 of 6)

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Note: Due to the high pin count, the package is illustrated across multiple pages (see Figure 2 through Figure 7).

	12	13	14	15	16	17	18	19	20	21	22	
A		GPIO[45]			GPIO[53]		GPIO[57]			SM_GPIO[32]		A
B	GPIO[42]	GPIO[43]	GPIO[47]		GPIO[52]	GPIO[56]	GPIO[59]	GPIO[58]		SM_GPIO[33]	SM_GPIO[38]	B
C		GPIO[44]	GPIO[46]	GPIO[50]		GPIO[54]		GPIO[55]	VSS	SM_GPIO[34]	SM_GPIO[36]	C
D			VSS	GPIO[51]		VSS				VSS	SM_GPIO[37]	D
E												E
F		GPIO[38]		GPIO[48]		GPIO[49]		SM_GPIO[31]		SM_GPIO[35]		F
G		VSS		VSS		VSS		VSS		VSS		G
H										SM_VDDIO1P8		H
J		VDD_CORE		VDD_CORE		VDD_CORE	VSS	VDD_CORE	VSS	SM_VDD_CORE		J
K												K
L	VSS		VDDIO1P8	VDDIO1P8	VDDIO1P8	VSS	VDD_CORE	VDD_CORE	VSS	SM_VDD_CORE		L
M												M
N	VDDQLP		VDD_CORE	VDD_CORE	VSS	VSS		VDD_CORE	VSS	SM_VDD_CORE		N
P	VDDQLP											P
R			VDD_CORE	VDD_CORE		VSS		VDD_CORE	VSS	SM_VDD_CORE		R
T	VDDQLP											T
U	VSS	VDD_CORE		VSS		VDD_CORE		VDD_CORE	VSS	SM_VDD_CORE		U
	12	13	14	15	16	17	18	19	20	21	22	

Figure 4. Top View (3 of 6)

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Note: Due to the high pin count, the package is illustrated across multiple pages (see Figure 2 through Figure 7).

	12	13	14	15	16	17	18	19	20	21	22	
V												V
W	VSS	VDD_CORE		VSS		VDD_CORE		VDD_CORE		VDD_CORE		W
Y						VSS						Y
AA		VDD_CORE		VDD_CORE		VSS		MIPI_DSI_REXT		VSS		AA
AB												AB
AC		VSS		VSS		MIPI_CSI_REXT		MIPI_DSI_AVDD1P8		SYSPLL_AVDD1P8		AC
AD		SDIO_VDDIO1P8		VSS		MIPI_CSI_AVDD				VSS		AD
AE	VSS			MIPI_CSI_AVDD1P8				VSS		AVPLL_AVDD1P8		AE
AF	SDIO1_CLK	SDIO1_DAT[3]	SDIO1_DAT0	VSS		VSS		MIPI_DSI_AVDD	VSS		VSS	AF
AG	SDIO1_CMD	SDIO1_DAT[1]		MIPI_CSI_D1p	MIPI_CSI_D1n	MIPI_CSI_D0n		MIPI_CSI_CKn	MIPI_DSI_D3p	MIPI_DSI_D3n	MIPI_DSI_D2p	AG
AH		SDIO1_DAT[2]		VSS		MIPI_CSI_D0p		MIPI_CSI_CKp			MIPI_DSI_D2n	AH
	12	13	14	15	16	17	18	19	20	21	22	

Figure 5. Top View (4 of 6)

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Note: Due to the high pin count, the package is illustrated across multiple pages (see Figure 2 through Figure 7).

	23	24	25	26	27	28	29	30	31	32	
A		SM_GPIO[4]		VSS		SM_ADCI[2]		VSS			A
B		SM_GPIO[5]	SM_GPIO[6]	SM_ADCI[0]	SM_ADCI[1]	SM_ADCI[3]	SM_ADCI[4]	SM_ADCI[5]	VSS		B
C		SM_GPIO[3]						SM_ADCI[6]			C
D		SM_GPIO[11]		VSS	SMTSEN_AVDD1P8	SM_ADC_AVSS		SM_ADCI[7]	VSS		D
E						SM_ADC_AVDD1P8		SM_XTAL32K_I			E
F	SM_GPIO[10]		VSS	SMOTP_AVDD1P8		VSS		SM_XTAL32K_O	SM_XTAL_O		F
G	SM_GPIO[9]							VSS	SM_XTAL_I		G
H			SM_VDDIO1P8	VSS		VSS	SM_GPIO[30]	SM_GPIO[29]			H
J	SM_VDD_CORE				SMOSC_VDDIO1P8		SM_GPIO[28]				J
K			VSS		SMPLL_AVDD1P8		SM_GPIO[27]				K
L	SM_VDD_CORE		VSS				SM_GPIO[26]	SM_GPIO[22]	SM_GPIO[21]		L
M			SM_VDDIO1P8		SM_GPIO[23]		SM_GPIO[24]	SM_GPIO[20]			M
N	VSS							SM_GPIO[17]	SM_GPIO[19]		N
P			VSS	SM_GPIO[25]		SM_GPIO[18]	SM_GPIO[14]	SM_GPIO[15]			P
R	VSS		SM_VDDIO1P8	VSS		VSS	SM_GPIO[16]				R
T							SM_AUDIO_MUTE	SM_GPIO[1]	SM_GPIO[7]		T
U	SM_VDDIO1P8		SM_GPIO[13]	SM_GPIO[8]		SM_GPIO[12]	SM_RSTn	SM_GPIO[2]			U
	23	24	25	26	27	28	29	30	31	32	

Figure 6. Top View (5 of 6)

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Note: Due to the high pin count, the package is illustrated across multiple pages (see Figure 2 through Figure 7).

	23	24	25	26	27	28	29	30	31	32	
V								SM_GPIO[0]	SM_POR_EN		V
W	VDDIO1P8		CAMERA_MUTE	SM_TRSTn		VSS	GPIO[3]	SM_TCK			W
Y											Y
AA	VDDIO1P8	VSS	GPIO[8]	GPIO[7]		VSS	GPIO[1]	GPIO[2]	GPIO[0]		AA
AB					VSS	GPIO[9]		GPIO[4]			AB
AC		VSS	GPIO[15]		GPIO[13]			GPIO[6]	GPIO[5]		AC
AD							VSS	GPIO[11]			AD
AE		GPIO[12]			VSS			GPIO[10]			AE
AF	MIPI_DSI_CKp	MIPI_DSI_CKn		VSS	GPIO[21]	GPIO[22]	VSS	GPIO[14]	GPIO[19]		AF
AG		MIPI_DSI_D1n		MIPI_DSI_D0p		GPIO[17]	GPIO[18]	GPIO[16]	VSS		AG
AH		MIPI_DSI_D1p		MIPI_DSI_D0n		GPIO[20]		VSS			AH
	23	24	25	26	27	28	29	30	31	32	

Figure 7. Top View (6 of 6)

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3.2. Pin Descriptions

Table 2. Pin Type Definitions

Pin Type	Definitions
I	Input only
O	Output only
I/O	Input and output
Analog	Analog Pin
CMOS	Complementary metal oxide semiconductor
SSTL	Stub Series Terminated Logic
PWR	Power Supply
GND	Ground Pin
Iu	Input with internal pull-up
Id	Input with internal pull-down
I/Ood	Input/Output pin, Open-Drain type
I/Ouod	Input/Output pin with internal pull-up, Open-Drain type
I/Odod	Input/Output pin with internal pull-down, Open-Drain type
Ouod	Output pin with internal pull-up, Open-Drain type
Ou	Output pin with internal pull-up

Note: A lowercase n at the end of a signal name indicates an active-low signal.

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Table 3. Interface Prefixes

Pin Type	Definitions
LPDDR4x/DDR4/ DDR3L memory channel 0	M0_
System Manager	SM_
Camera Interface	CAM_
CAN-FD	CAN0_, CAN1_
eMMC	eMMC_
I²S	I2S1_, I2S2_, I2S3_
Keyboard	KEY_
PDM	PDM_
RGMII Interface	RGMII1_, RGMII2_
RMII Interface	RMII1_, RMII2_
SDIO	SDIO1_, SDIO2_
SPI	SPI1_, SPI2_, SPI3_, SPI4_, SPI5_
TWSI	TW0_, TW1_, TW2_, TW3_
UART	URT0_, URT1_, URT2_, URT3_, URT4_, URT5_, URT6_, URT7_
USB 2.0	USB2_0_, USB2_1_
Quad/Octa SPI Interface	xSPI_
Power for digital domain	VDD_
Power for analog domain	AVDD_, AVDD2_
Ground for analog domain	AVSS_

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Table 4. System Manager (SM), OPT1

Pin #	Pin Name	Pin Type	Description
U29	SM_RSTn	Iu, CMOS	SoC Active low reset input with internal pullup.
W30	SM_TCK	Id, CMOS	SM JTAG Clock.
W26	SM_TRSTn	Id, CMOS	SM JTAG Reset.
V30	SM_TMS	Iu, CMOS	SM JTAG Mode select signal (Arm or chip JTAG).
T30	SM_TDI	Iu, CMOS	SM JTAG SDATA IN.
U30	SM_TDO	Iu, CMOS	SM JTAG SDATA OUT.
T29	SM_AUDIO_MUTE	Id, CMOS	FORCE Audio MUTE selection. 0: No mute. 1: Mute local digital microphones and I2S1,I2S2 and I2S3.
V31	SM_POR_EN	Iu, CMOS	Power-on reset enable. 0: Bypass on-chip power-on reset generator. 1: Enable on-chip power-on reset generator.

Table 5. SM Analog and Oscillator/Crystal Interfaces

Pin Location(s)	Signal	Pin Type	Description
B26	SM_ADCI[0]	I, Analog	ADC input. Full input range 1.8V.
B27	SM_ADCI[1]	I, Analog	ADC input. Full input range 1.8V.
A28	SM_ADCI[2]	I, Analog	ADC input. Full input range 1.8V.
B28	SM_ADCI[3]	I, Analog	ADC input. Full input range 1.8V.
B29	SM_ADCI[4]	I, Analog	ADC input. Full input range 1.8V.
B30	SM_ADCI[5]	I, Analog	ADC input. Full input range 1.8V.
C30	SM_ADCI[6]	I, Analog	ADC input. Full input range 1.8V.
D30	SM_ADCI[7]	I, Analog	ADC input. Full input range 1.8V.
G31	SM_XTAL_I	I, Analog	Oscillator/Crystal Input 25 MHz.
F31	SM_XTAL_O	I/O, Analog	Crystal inverted output.
E30	SM_XTAL32K_I	I, Analog	Oscillator/Crystal Input 32 kHz.
F30	SM_XTAL32K_O	I/O, Analog	Crystal inverted output.

Table 6. SM I3C Controller OPT3, OPT5

Pin #	Pin Name	Pin Type	Description
C24, U28	SM_I3C_MS_SCL	I/Ood, CMOS	I3C Clock.
A24, U25	SM_I3C_MS_SDA	I/Ood, CMOS	I3C Data Signal.

Table 7. SM Control Area Network Flexible Data (CAN-FD)

Pin #	Pin Name	Pin Type	Description
F10, P29, R29, T31	SM_CAN0_RX	I, CMOS	CAN0-FD receive data input.
C8, N30, P30, U26	SM_CAN0_TX	O, CMOS	CAN0-FD transmit data output.
AG29, F13, F19	SM_CAN1_RX	I, CMOS	CAN1-FD receive data input.
A21, AF31, B10	SM_CAN1_TX	O, CMOS	CAN1-FD transmit data output.

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Table 8. SM Timer Control Smart PWM (sPWM) Alternative Interfaces

Pin #	Pin Name	Pin Type	Description
A24, F19	SM_sPWM[0]	I/O, CMOS	Pulse-Width Modulation input/output data 0.
A21, B24	SM_sPWM[1]	I/O, CMOS	Pulse-Width Modulation input/output data 1.
B21, B25	SM_sPWM[2]	I/O, CMOS	Pulse-Width Modulation input/output data 2.
C21, G23	SM_sPWM[3]	I/O, CMOS	Pulse-Width Modulation input/output data 3.
F21, F23	SM_sPWM[4]	I/O, CMOS	Pulse-Width Modulation input/output data 4.
C22, D24	SM_sPWM[5]	I/O, CMOS	Pulse-Width Modulation input/output data 5.
D22, U28	SM_sPWM[6]	I/O, CMOS	Pulse-Width Modulation input/output data 6.
B22, R29	SM_sPWM[7]	I/O, CMOS	Pulse-Width Modulation input/output data 7.
C24, N30	SM_sPWM[8]	I/O, CMOS	Pulse-Width Modulation input/output data 8.
T30, T31	SM_sPWM[9]	I/O, CMOS	Pulse-Width Modulation input/output data 9.
P29, V30	SM_sPWM[10]	I/O, CMOS	Pulse-Width Modulation input/output data 10.
P30, U30	SM_sPWM[11]	I/O, CMOS	Pulse-Width Modulation input/output data 11.

Table 9. SM SPI1 Controller Interface, OPT2

Pin #	Pin Name	Pin Type	Description
C24	SM_SPI1_SS0n	O, CMOS	SPI1 chip select 0 for first device.
A24	SM_SPI1_SS1n	O, CMOS	SPI1 chip select 1 for second device.
B24	SM_SPI1_SS2n	O, CMOS	SPI1 chip select 2 for third device.
B25	SM_SPI1_SS3n	O, CMOS	SPI1 chip select 3 for fourth device.
F23	SM_SPI1_SCLK	O, CMOS	SPI1 serial clock.
D24	SM_SPI1_SDI	I, CMOS	SPI1 serial data input.
G23	SM_SPI1_SDO	I/O, CMOS	SPI1 serial data output.

Table 10. SM SPI1 Target Interface, OPT3

Pin #	Pin Name	Pin Type	Description
B25	SM_SPI1S_SS0n	I, CMOS	SPI1 chip select
F23	SM_SPI1S_SCLK	I, CMOS	SPI1 serial clock input.
D24	SM_SPI1S_SDI	I, CMOS	SPI1 serial data input.
G23	SM_SPI1S_SDO	I/O, CMOS	SPI1 serial data output.

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Table 11. SoC SPI Controller Alternative Interfaces

Pin #	Pin Name	Pin Type	Description
AG30	SPI2_SS0n	O, CMOS	SPI2 chip select 0 for first device.
AG28	SPI2_SS1n	O, CMOS	SPI2 chip select 1 for second device.
AG29	SPI2_SS2n	O, CMOS	SPI2 chip select 2 for third device.
AF31	SPI2_SS3n	O, CMOS	SPI2 chip select 3 for fourth device.
AF27	SPI2_SCLK	O, CMOS	SPI2 serial clock.
AF28	SPI2_SDI	I, CMOS	SPI2 serial data input.
AH28	SPI2_SDO	I/O, CMOS	SPI2 serial data output.
AA31, D15	SPI3_SS0n	O, CMOS	SPI3 chip select 0 for first device.
W29, C8, C15	SPI3_SS1n	O, CMOS	SPI3 chip select 1 for second device.
B4, C7, F17	SPI3_SS2n	O, CMOS	SPI3 chip select 2 for third device.
B3, B7, F15	SPI3_SS3n	O, CMOS	SPI3 chip select 3 for fourth device.
AA29, A16	SPI3_SCLK	O, CMOS	SPI3 serial clock.
AB30, C17	SPI3_SDI	I, CMOS	SPI3 serial data input.
AA30, B16	SPI3_SDO	I/O, CMOS	SPI3 serial data output.
B13, B17, C9	SPI4_SS0n	O, CMOS	SPI4 chip select 0 for first device.
C8, C19	SPI4_SS1n	O, CMOS	SPI4 chip select 1 for second device.
A9, B16, C7, F15	SPI4_SS2n	O, CMOS	SPI4 chip select 2 for third device.
A16, B7, D11, F17	SPI4_SS3n	O, CMOS	SPI4 chip select 3 for fourth device.
B6, B12, B19	SPI4_SCLK	O, CMOS	SPI4 serial clock.
A6, B18, C13	SPI4_SDI	I, CMOS	SPI4 serial data input.
A18, B9	SPI4_SDO	I/O, CMOS	SPI4 serial data output.
F15	SPI5_SS0n	O, CMOS	SPI5 chip select 0 for first device.
D11	SPI5_SS1n	O, CMOS	SPI5 chip select 1 for second device.
A9	SPI5_SS2n	O, CMOS	SPI5 chip select 2 for third device.
C7	SPI5_SS3n	O, CMOS	SPI5 chip select 3 for fourth device.
B11, C15	SPI5_SCLK	O, CMOS	SPI5 serial clock.
B10, C19	SPI5_SDI	I, CMOS	SPI5 serial data input.
F13, F17	SPI5_SDO	I/O, CMOS	SPI5 serial data output.

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Table 12. SDIO1 Alternative Interface

Pin #	Pin Name	Pin Type	Description
AF14	SDIO1_DAT[0]	I/O, CMOS	Data[0]. Busy from card; DI in SPI mode.
AG13	SDIO1_DAT[1]	I/O, CMOS	Data[1]. Int from card.
AH13	SDIO1_DAT[2]	I/O, CMOS	Data[2]. Read wait from card.
AF13	SDIO1_DAT[3]	I/O, CMOS	Data[3]. SSn in SPI mode.
AF12	SDIO1_CLK	O, CMOS	Output clock. CLK in SPI mode.
AG12	SDIO1_CMD	I/O, CMOS	Command/Response. DO in SPI mode.
AF28, C14	SDIO1_CDn	I, CMOS	Card Detect. 0 = Detect.
AE24, B14	SDIO1_WP	I, CMOS	Write Protect. 1 = Write protect.

Table 13. SDIO2 Alternative Interface, OTP4

Pin #	Pin Name	Pin Type	Description
AF31	SDIO2_DAT[0]	I/O, CMOS	Data[0]. Busy from card; DI in SPI mode.
AG29	SDIO2_DAT[1]	I/O, CMOS	Data[1]. Int from card.
AG28	SDIO2_DAT[2]	I/O, CMOS	Data[2]. Read wait from card.
AG30	SDIO2_DAT[3]	I/O, CMOS	Data[3]. SSn in SPI mode.
AF27	SDIO2_CLK	O, CMOS	Output clock. CLK in SPI mode.
AH28	SDIO2_CMD	I/O, CMOS	Command/Response. DO in SPI mode.
AF28	SDIO2_CDn	I, CMOS	Card Detect. 0 = Detect.
AE24	SDIO2_WP	I, CMOS	Write Protect. 1 = Write protect.

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Table 14. SM Buffered Clock Output Alternative Interfaces, OPT4, OPT8

Pin #	Pin Name	Pin Type	Description
U25, U26	SM_CLKOUT	O, CMOS	Buffered Clock output (32 kHz) – AON GPO
H29, L29	SM_CLKOUT	O, CMOS	Buffered Clock output (32 kHz)

Table 15. DDR3L/DDR4/LPDDR4/LPDDR4x Calibration

Pin #	Pin Name	Pin Type	Description
N8	M0_CAL	I, Analog	DDR3L/DDR4/LPDDR4/LPDDR4x Calibration pin. Connect to VSS (DDR3L/DDR4) or 1.1V VDDQ (LPDDR4) or 0.6V VDDQL (LPDDR4x) via a 120 Ohm ±1% resistor.

Table 16. M0 Memory Interface Pin Mux

Pin #	Pin Name	LPDDR4 Signal	DDR4 Signal	DDR3L Signal
AA4	M0_RSTn	M0_LPDDR4_RSTn	M0_DDR4_RSTn	M0_DDR3L_RSTn
N8	M0_CAL	M0_CAL	M0_CAL	M0_CAL
W3	M0_A[0]	NC	M0_DDR4_A[0]	M0_DDR3L_A[5]
W7	M0_A[1]	NC	M0_DDR4_A[1]	M0_DDR3L_BA[0]
AA3	M0_A[2]	M0_LPDDR4_A[0]	M0_DDR4_A[2]	M0_DDR3L_A[13]
W6	M0_A[3]	NC	M0_DDR4_A[3]	M0_DDR3L_BA[2]
V2	M0_A[4]	M0_LPDDR4_A[5]	M0_DDR4_A[4]	M0_DDR3L_A[3]
R3	M0_A[5]	NC	M0_DDR4_A[5]	M0_DDR3L_A[8]
Y1	M0_A[6]	M0_LPDDR4_A[2]	M0_DDR4_A[6]	M0_DDR3L_A[9]
U3	M0_A[7]	NC	M0_DDR4_A[7]	M0_DDR3L_A[14]
AA2	M0_A[8]	M0_LPDDR4_A[1]	M0_DDR4_A[8]	M0_DDR3L_A[11]
Y2	M0_A[9]	NC	M0_DDR4_A[9]	M0_DDR3L_A[1]
U2	M0_A[10]	M0_LPDDR4_A[3]	M0_DDR4_A[10]	M0_DDR3L_A[12]
AB3	M0_A[11]	NC	M0_DDR4_A[11]	M0_DDR3L_A[7]
R4	M0_A[12]	NC	M0_DDR4_A[12]	M0_DDR3L_WEn
U1	M0_A[13]	M0_LPDDR4_A[4]	M0_DDR4_A[13]	M0_DDR3L_A[0]
U6	M0_ACTn	NC	M0_DDR4_ACTn	M0_DDR3L_CASn
V3	M0_BA[0]	NC	M0_DDR4_BA[0]	M0_DDR3L_A[2]
R2	M0_BA[1]	NC	M0_DDR4_BA[1]	M0_DDR3L_A[6]
U7	M0_BG[0]	NC	M0_DDR4_BG[0]	M0_DDR3L_A[15]
P1	M0_BG[1]	NC	M0_DDR4_BG[1]	M0_DDR3L_BA[1]
P2	M0_CASn	NC	M0_DDR4_CASn	M0_DDR3L_A[4]
N6	M0_CKE	M0_LPDDR4_CKE	M0_DDR4_CKE	M0_DDR3L_CKE
M3	M0_CKn	M0_LPDDR4_CKn	M0_DDR4_CKn	M0_DDR3L_CKn
N3	M0_CKp	M0_LPDDR4_CKp	M0_DDR4_CKp	M0_DDR3L_CKp
M1	M0_CSn	M0_LPDDR4_CSn	M0_DDR4_CSn	M0_DDR3L_CSn
J6	M0_DM[0]	M0_LPDDR4_DM[1]	M0_DDR4_DM[0]	M0_DDR3L_DM[0]
D4	M0_DM[1]	M0_LPDDR4_DM[0]	M0_DDR4_DM[1]	M0_DDR3L_DM[1]
H2	M0_DQ[0]	M0_LPDDR4_DQ[8]	M0_DDR4_DQ[0]	M0_DDR3L_DQ[0]
J1	M0_DQ[1]	M0_LPDDR4_DQ15]	M0_DDR4_DQ[1]	M0_DDR3L_DQ[3]
J3	M0_DQ[2]	M0_LPDDR4_DQ[14]	M0_DDR4_DQ[2]	M0_DDR3L_DQ[2]
J5	M0_DQ[3]	M0_LPDDR4_DQ[11]	M0_DDR4_DQ[3]	M0_DDR3L_DQ[1]
K2	M0_DQ[4]	M0_LPDDR4_DQ[10]	M0_DDR4_DQ[4]	M0_DDR3L_DQ[5]
J2	M0_DQ[5]	M0_LPDDR4_DQ[9]	M0_DDR4_DQ[5]	M0_DDR3L_DQ[4]
L2	M0_DQ[6]	M0_LPDDR4_DQ[12]	M0_DDR4_DQ[6]	M0_DDR3L_DQ[7]

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Pin #	Pin Name	LPDDR4 Signal	DDR4 Signal	DDR3L Signal
L6	M0_DQ[7]	M0_LPDDR4_DQ[13]	M0_DDR4_DQ[7]	M0_DDR3L_DQ[6]
C2	M0_DQ[8]	M0_LPDDR4_DQ[0]	M0_DDR4_DQ[8]	M0_DDR3L_DQ[15]
E2	M0_DQ[9]	M0_LPDDR4_DQ[1]	M0_DDR4_DQ[9]	M0_DDR3L_DQ[12]
F2	M0_DQ[10]	M0_LPDDR4_DQ[7]	M0_DDR4_DQ[10]	M0_DDR3L_DQ[14]
F4	M0_DQ[11]	M0_LPDDR4_DQ[5]	M0_DDR4_DQ[11]	M0_DDR3L_DQ[10]
G6	M0_DQ[12]	M0_LPDDR4_DQ[3]	M0_DDR4_DQ[12]	M0_DDR3L_DQ[13]
F1	M0_DQ[13]	M0_LPDDR4_DQ[6]	M0_DDR4_DQ[13]	M0_DDR3L_DQ[8]
F3	M0_DQ[14]	M0_LPDDR4_DQ[2]	M0_DDR4_DQ[14]	M0_DDR3L_DQ[9]
G4	M0_DQ[15]	M0_LPDDR4_DQ[4]	M0_DDR4_DQ[15]	M0_DDR3L_DQ[11]
G2	M0_DQS0n	M0_LPDDR4_DQS1n	M0_DDR4_DQS0n	M0_DDR3L_DQS0n
G1	M0_DQS0p	M0_LPDDR4_DQS1p	M0_DDR4_DQS0p	M0_DDR3L_DQS0p
D1	M0_DQS1n	M0_LPDDR4_DQS0n	M0_DDR4_DQS1n	M0_DDR3L_DQS1n
D2	M0_DQS1p	M0_LPDDR4_DQS0p	M0_DDR4_DQS1p	M0_DDR3L_DQS1p
L5	M0_ODT	M0_LPDDR4_ODT	M0_DDR4_ODT	M0_DDR3L_ODT
M2	M0_RASn	NC	M0_DDR4_RASn	M0_DDR3L_A[10]
N5	M0_WEn	NC	M0_DDR4_WEn	M0_DDR3L_RASn Row active

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Table 17. Memory Interface in LPDDR4 Mode

Pin #	Signal Name	Pin Type	Description
AA4	MO_LPDDR4_RSTn	O, HS_LVCMOS	MO reset, active low.
N8	MO_CAL	I, Analog	LPDDR4/4x Calibration pad. Connect to 1.1V VDDQ (LPDDR4) or 0.6V VDDQL (LPDDR4x) via a 120 ±1% ohm resistor.
N3	MO_LPDDR4_CKp	O, HS_LVCMOS	MO LPDDR4_CK+ clock positive.
M3	MO_LPDDR4_CKn	O, HS_LVCMOS	MO LPDDR4_CK- clock negative.
N6	MO_LPDDR4_CKE	O, HS_LVCMOS	MO LPDDR4_CKE clock enable.
M1	MO_LPDDR4_CSn	O, HS_LVCMOS	MO LPDDR4_CSn chip select.
AA3	MO_LPDDR4_A[0]	O, HS_LVCMOS	MO LPDDR4 ADDR[0].
AA2	MO_LPDDR4_A[1]	O, HS_LVCMOS	MO LPDDR4 ADDR[1].
Y1	MO_LPDDR4_A[2]	O, HS_LVCMOS	MO LPDDR4 ADDR[2].
U2	MO_LPDDR4_A[3]	O, HS_LVCMOS	MO LPDDR4 ADDR[3].
U1	MO_LPDDR4_A[4]	O, HS_LVCMOS	MO LPDDR4 ADDR[4].
V2	MO_LPDDR4_A[5]	O, HS_LVCMOS	MO LPDDR4 ADDR[5].
D4	MO_LPDDR4_DM[0]	O, HS_LVCMOS	MO LPDDR4 Data mask BYTE[0].
J6	MO_LPDDR4_DM[1]	O, HS_LVCMOS	MO LPDDR4 Data mask BYTE[1].
C2	MO_LPDDR4_DQ[0]	I/O, HS_LVCMOS	MO LPDDR4 DQ[0].
E2	MO_LPDDR4_DQ[1]	I/O, HS_LVCMOS	MO LPDDR4 DQ[1].
F3	MO_LPDDR4_DQ[2]	I/O, HS_LVCMOS	MO LPDDR4 DQ[2].
G6	MO_LPDDR4_DQ[3]	I/O, HS_LVCMOS	MO LPDDR4 DQ[3].
G4	MO_LPDDR4_DQ[4]	I/O, HS_LVCMOS	MO LPDDR4 DQ[4].
F4	MO_LPDDR4_DQ[5]	I/O, HS_LVCMOS	MO LPDDR4 DQ[5].
F1	MO_LPDDR4_DQ[6]	I/O, HS_LVCMOS	MO LPDDR4 DQ[6].
F2	MO_LPDDR4_DQ[7]	I/O, HS_LVCMOS	MO LPDDR4 DQ[7].
H2	MO_LPDDR4_DQ[8]	I/O, HS_LVCMOS	MO LPDDR4 DQ[8].
J2	MO_LPDDR4_DQ[9]	I/O, HS_LVCMOS	MO LPDDR4 DQ[9].
K2	MO_LPDDR4_DQ[10]	I/O, HS_LVCMOS	MO LPDDR4 DQ[10].
J5	MO_LPDDR4_DQ[11]	I/O, HS_LVCMOS	MO LPDDR4 DQ[11].
L2	MO_LPDDR4_DQ[12]	I/O, HS_LVCMOS	MO LPDDR4 DQ[12].
L6	MO_LPDDR4_DQ[13]	I/O, HS_LVCMOS	MO LPDDR4 DQ[13].
J3	MO_LPDDR4_DQ[14]	I/O, HS_LVCMOS	MO LPDDR4 DQ[14].
J1	MO_LPDDR4_DQ[15]	I/O, HS_LVCMOS	MO LPDDR4 DQ[15].
D2	MO_LPDDR4_DQS0p	I/O, HS_LVCMOS	MO LPDDR4 DQS0p BYTE 0.
D1	MO_LPDDR4_DQS0n	I/O, HS_LVCMOS	MO LPDDR4 DQS0n BYTE 0.
G1	MO_LPDDR4_DQS1p	I/O, HS_LVCMOS	MO LPDDR4 DQSp BYTE 1.
G2	MO_LPDDR4_DQS1n	I/O, HS_LVCMOS	MO LPDDR4 DQSn BYTE 1.

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Table 18. Memory Interface in DDR4 Mode

Pin #	Signal Name	Pin Type	Description
AA4	M0_RSTn	O, SSTL12	M0_DDR4_RSTn. This pin is active low.
N8	M0_CAL	I, Analog	DDR4/DDR3L Calibration pad. Connect to VSS via a 120 ±1% ohm resistor.
N3	M0_ DDR4_CKp	O, SSTL12	M0_DDR4_CKp.
M3	M0_ DDR4_CKn	O, SSTL12	M0_DDR4_CKn.
N6	M0_ DDR4_CKE	O, SSTL12	M0_DDR4 Clock enable.
M1	M0_ DDR4_CSn	O, SSTL12	M0_DDR4 Chip select.
W3	M0_DDR4_A[0]	O, SSTL12	M0_DDR4_A[0].
W7	M0_DDR4_A[1]	O, SSTL12	M0_DDR4_A[1].
AA3	M0_DDR4_A[2]	O, SSTL12	M0_DDR4_A[2].
W6	M0_DDR4_A[3]	O, SSTL12	M0_DDR4_A[3].
V2	M0_DDR4_A[4]	O, SSTL12	M0_DDR4_A[4].
R3	M0_DDR4_A[5][	O, SSTL12	M0_DDR4_A[5].
Y1	M0_DDR4_A[6]	O, SSTL12	M0_DDR4_A[6].
U3	M0_DDR4_A[7]	O, SSTL12	M0_DDR4_A[7].
AA2	M0_DDR4_A[8]	O, SSTL12	M0_DDR4_A[8].
Y2	M0_DDR4_A[9]	O, SSTL12	M0_DDR4_A[9].
U2	M0_DDR4_A[10]	O, SSTL12	M0_DDR4_A[10].
AB3	M0_DDR4_A[11]	O, SSTL12	M0_DDR4_A[11].
R4	M0_DDR4_A[12]	O, SSTL12	M0_DDR4_A[12].
U1	M0_DDR4_A[13]	O, SSTL12	M0_DDR4_A[13].
N5	M0_ DDR4_WEn	O, SSTL12	M0_DDR4 Write enable or M0_A[14].
U6	M0_DDR4_ACTn	O, SSTL12	M0_DDR4_ACTn.
V3	M0_DDR4_BA[0]	O, SSTL12	M0_DDR4_BA0 Bank Select[0]
R2	M0_DDR4_BA[1]	O, SSTL12	M0_DDR4_BA1 Bank Select[1]
U7	M0_DDR4_BG[0]	O, SSTL12	M0_DDR4_BG0 Bank Group[0].
P1	M0_DDR4_BG[1]	O, SSTL12	M0_DDR4_BG1 Bank Group[1].
P2	M0_DDR4_CASn	O, SSTL12	M0_DDR4 Column activate or M0_A[15].
J6	M0_ DDR4_DM[0]	I/O, POD12	M0_DDR4 Data mask BYTE[0].
D4	M0_ DDR4_DM[1]	I/O, POD12	M0_DDR4 Data mask BYTE[1].
H2	M0_ DDR4_DQ[0]	I/O, POD12	M0_DDR4_DQ[0].
J1	M0_ DDR4_DQ[1]	I/O, POD12	M0_DDR4_DQ[1].
J3	M0_ DDR4_DQ[2]	I/O, POD12	M0_DDR4_DQ[2].
J5	M0_ DDR4_DQ[3]	I/O, POD12	M0_DDR4_DQ[3].
K2	M0_ DDR4_DQ[4]	I/O, POD12	M0_DDR4_DQ[4].
J2	M0_ DDR4_DQ[5]	I/O, POD12	M0_DDR4_DQ[5].

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Pin #	Signal Name	Pin Type	Description
L2	M0_ DDR4_DQ[6]	I/O, POD12	M0_DDR4_DQ[6].
L6	M0_ DDR4_DQ[7]	I/O, POD12	M0_DDR4_DQ[7].
C2	M0_ DDR4_DQ[8]	I/O, POD12	M0_DDR4_DQ[8].
E2	M0_ DDR4_DQ[9]	I/O, POD12	M0_DDR4_DQ[9].
F2	M0_ DDR4_DQ[10]	I/O, POD12	M0_DDR4_DQ[10].
F4	M0_ DDR4_DQ[11]	I/O, POD12	M0_DDR4_DQ[11].
G6	M0_ DDR4_DQ[12]	I/O, POD12	M0_DDR4_DQ[12].
F1	M0_ DDR4_DQ[13]	I/O, POD12	M0_DDR4_DQ[13].
F3	M0_ DDR4_DQ[14]	I/O, POD12	M0_DDR4_DQ[14].
G4	M0_ DDR4_DQ[15]	I/O, POD12	M0_DDR4_DQ[15].
G2	M0_ DDR4_DQS0n	I/O, POD12	M0 DDR4 DQS0n BYTE 0.
G1	M0_ DDR4_DQS0p	I/O, POD12	M0 DDR4 DQS0p BYTE 0.
D1	M0_ DDR4_DQS1n	I/O, POD12	M0 DDR4 DQS1n BYTE 1.
D2	M0_ DDR4_DQS1p	I/O, POD12	M0 DDR4 DQS1p BYTE 1.
L5	M0_ DDR4_ODT	O, SSTL12	M0_DDR4 On die termination.
M2	M0_ DDR4_RASn	O, SSTL12	M0_DDR4 Row activate.

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Table 19. Memory Interface in DDR3L Mode

Pin #	Signal Name	Pin Type	Description
AA4	M0_RSTn	O, SSTL15	M0_DDR3L_RSTn RESETn for DDR3L
N8	M0_CAL	I, Analog	DDR4/DDR3L Calibration pad. Connect to VSS via a 120 ±1% Ohm resistor.
N3	M0_DDR3L_CKp	O, SSTL15	M0_DDR3L_CKp Positive
M3	M0_DDR3L_CKn	O, SSTL15	M0_DDR3L_CKn Negative
N6	M0_DDR3L_CKE	O, SSTL15	M0_DDR3L_CKE Clock enable
M1	M0_DDR3L_CSn	O, SSTL15	M0_DDR3L_CSn Chip select
U1	M0_DDR3L_A[0]	O, SSTL15	M0_DDR3L_A[0]
Y2	M0_DDR3L_A[1]	O, SSTL15	M0_DDR3L_A[1]
V3	M0_DDR3L_A[2]	O, SSTL15	M0_DDR3L_A[2]
V2	M0_DDR3L_A[3]	O, SSTL15	M0_DDR3L_A[3]
P2	M0_DDR3L_A[4]	O, SSTL15	M0_DDR3L_A[4]
W3	M0_DDR3L_A[5]	O, SSTL15	M0_DDR3L_A[5]
R2	M0_DDR3L_A[6]	O, SSTL15	M0_DDR3L_A[6]
AB3	M0_DDR3L_A[7]	O, SSTL15	M0_DDR3L_A[7]
R3	M0_DDR3L_A[8]	O, SSTL15	M0_DDR3L_A[8]
Y1	M0_DDR3L_A[9]	O, SSTL15	M0_DDR3L_A[9]
M2	M0_DDR3L_A[10]	O, SSTL15	M0_DDR3L_A[10]

Pin #	Signal Name	Pin Type	Description
AA2	M0_DDR3L_A[11]	O, SSTL15	M0_DDR3L_A[11]
U2	M0_DDR3L_A[12]	O, SSTL15	M0_DDR3L_A[12]
AA3	M0_DDR3L_A[13]	O, SSTL15	M0_DDR3L_A[13]
U3	M0_DDR3L_A[14]	O, SSTL15	M0_DDR3L_A[14]
U7	M0_DDR3L_A[15]	O, SSTL15	M0_DDR3L_A[15]
W7	M0_DDR3L_BA[0]	O, SSTL15	M0_DDR3L_BA0 Bank select[0]
P1	M0_DDR3L_BA[1]	O, SSTL15	M0_DDR3L_BA1 Bank select[1]
W6	M0_DDR3L_BA[2]	O, SSTL15	M0_DDR3L_BA2 Bank select[2]
U6	M0_DDR3L_CASn	O, SSTL15	M0_DDR3L_CASn Column active
N5	M0_DDR3L_RASn	O, SSTL15	M0_DDR3L_RASn Row active
R4	M0_DDR3L_WEn	O, SSTL15	M0_DDR3L_WEn Write enable
J6	M0_DDR3L_DM[0]	O, SSTL15	M0_DDR3L_DM0 Data mask BYTE[0]
D4	M0_DDR3L_DM[1]	O, SSTL15	M0_DDR3L_DM1 Data mask BYTE[1]
H2	M0_DDR3L_DQ[0]	I/O, SSTL15	M0_DDR3L_DQ[0]
J5	M0_DDR3L_DQ[1]	I/O, SSTL15	M0_DDR3L_DQ[1]
J3	M0_DDR3L_DQ[2]	I/O, SSTL15	M0_DDR3L_DQ[2]
J1	M0_DDR3L_DQ[3]	I/O, SSTL15	M0_DDR3L_DQ[3]
J2	M0_DDR3L_DQ[4]	I/O, SSTL15	M0_DDR3L_DQ[4]
K2	M0_DDR3L_DQ[5]	I/O, SSTL15	M0_DDR3L_DQ[5]
L6	M0_DDR3L_DQ[6]	I/O, SSTL15	M0_DDR3L_DQ[6]
L2	M0_DDR3L_DQ[7]	I/O, SSTL15	M0_DDR3L_DQ[7]
F1	M0_DDR3L_DQ[8]	I/O, SSTL15	M0_DDR3L_DQ[8]
F3	M0_DDR3L_DQ[9]	I/O, SSTL15	M0_DDR3L_DQ[9]
F4	M0_DDR3L_DQ[10]	I/O, SSTL15	M0_DDR3L_DQ[10]
G4	M0_DDR3L_DQ[11]	I/O, SSTL15	M0_DDR3L_DQ[11]
E2	M0_DDR3L_DQ[12]	I/O, SSTL15	M0_DDR3L_DQ[12]
G6	M0_DDR3L_DQ[13]	I/O, SSTL15	M0_DDR3L_DQ[13]
F2	M0_DDR3L_DQ[14]	I/O, SSTL15	M0_DDR3L_DQ[14]
C2	M0_DDR3L_DQ[15]	I/O, SSTL15	M0_DDR3L_DQ[15]
G1	M0_DDR3L_DQS0p	I/O, SSTL15	M0_DDR3L_DQS0p positive BYTE0
G2	M0_DDR3L_DQS0n	I/O, SSTL15	M0_DDR3L_DQS0n negative BYTE0
D2	M0_DDR3L_DQS1p	I/O, SSTL15	M0_DDR3L_DQS1p positive BYTE1
D1	M0_DDR3L_DQS1n	I/O, SSTL15	M0_DDR3L_DQS1n negative BYTE1
L5	M0_DDR3L_ODT	O, SSTL15	M0_DDR3L_ODT One die termination

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Table 20. SM UART Interface

Pin #	Pin Name	Pin Type	Description
T30, T31, F19	SM_URT0_RXD	I, CMOS	UART0 RX
A21, N30, U26, V30	SM_URT0_TXD	O, CMOS	UART0 TX
C22, H30, P29	SM_URT0_CTSn	I, CMOS	UART0 CTSN
F21, J29, P30	SM_URT0_RTSn	O, CMOS	UART0 RTSN
A6, C6, F19, R29, T31	SM_URT1_RXD	I, CMOS	UART1 RX
A21, B6, C5, N30, U26	SM_URT1_TXD	O, CMOS	UART1 TX
B2, B14, C22, H30, P29	SM_URT1_CTSn	I, CMOS	UART1 CTSN
A3, C14, F21, J29, P30	SM_URT1_RTSn	O, CMOS	UART1 RTSN
C21, K29	SM_URT2_RXD	I, CMOS	UART2 RX
B21, L29	SM_URT2_TXD	O, CMOS	UART2 TX
C22, H30	SM_URT2_CTSn	I, CMOS	UART2 CTSN
F21, J29	SM_URT2_RTSn	O, CMOS	UART2 RTSN
C22, H30	SM_URT3_RXD	I, CMOS	UART3 RX
F21, J29	SM_URT3_TXD	O, CMOS	UART3 TX
C21, K29	SM_URT3_CTSn	I, CMOS	UART3 CTSN
B21, L29	SM_URT3_RTSn	O, CMOS	UART3 RTSN
B21, L29	SM_URT3_DE	O, CMOS	UART3 DE
C21, K29	SM_URT3_REn	O, CMOS	UART3 REN

Table 21. SoC UART Interface

Pin #	Pin Name	Pin Type	Description
B2	URT4_RXD	I, CMOS	UART4 RX
A3	URT4_TXD	O, CMOS	UART4 TX
A6	URT4_DE	O, CMOS	UART4 DE
B6	URT4_REn	O, CMOS	UART4 REn
C6, C9	URT5_RXD	I, CMOS	UART5 RX
B9, C5	URT5_TXD	O, CMOS	UART5 TX
D11	URT6_RXD	I, CMOS	UART6 RX
A9	URT6_TXD	O, CMOS	UART6 TX
B12	URT7_RXD	I, CMOS	UART7 RX
C13	URT7_TXD	O, CMOS	UART7 TX

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Table 22. SM Two-Wire Serial Interface

Pin #	Pin Name	Pin Type	Description
B22, U25	SM_TW0_SDA	I/Ood, CMOS	TWSI0 Serial data
D22, U28	SM_TW0_SCL	I/Ood, CMOS	TWSI0 Serial clock
A24, P30	SM_TW1_SDA	I/Ood, CMOS	TWSI1 Serial data
C24, P29	SM_TW1_SCL	I/Ood, CMOS	TWSI1 Serial clock

Table 23. SoC Two-Wire Serial Interface, OPT2

Pin #	Pin Name	Pin Type	Description
B3	TW2_SDA	I/Ood, CMOS	TWSI0 Serial data
B4	TW2_SCL	I/Ood, CMOS	TWSI0 Serial clock
B2	TW3_SDA	I/Ood, CMOS	TWSI1 Serial data
A3	TW3_SCL	I/Ood, CMOS	TWSI1 Serial clock

Table 24. Audio Alternative Interface (I2S/TDM), OPT2, OPT4

Pin #	Pin Name	Pin Type	Description
AA29	I2S1_BCLK	I/O, CMOS	Interface #1 Audio bit clock
AA31	I2S1_LRCK	I/O, CMOS	Interface #1 Audio WS or LR select
W29	I2S1_MCLK	I/O, CMOS	Interface #1 Audio Host clock
AA30	I2S1_DO	O, CMOS	Interface #1 Data out
AB30	I2S1_DI	I, CMOS	Interface #1 Data In
AC30	I2S2_BCLK	I/O, CMOS	Interface #2 Audio bit clock
AC31	I2S2_LRCK	I/O, CMOS	Interface #2 Audio WS or LR select
AD30, U30	I2S2_MCLK	I/O, CMOS	Interface #2 Audio Host clock
AA26	I2S2_DO	O, CMOS	Interface #2 Data out.
AA25	I2S2_DI	I, CMOS	Interface #2 Data in.
AC27	I2S3_BCLK	I/O, CMOS	Interface #3 Audio bit clock.
AE24	I2S3_LRCK	I/O, CMOS	Interface #3 Audio WS or LR select.
AF30	I2S3_DO	O, CMOS	Interface #3 Data out.
AC25	I2S3_DI	I, CMOS	Interface #3 Data in.

Table 25. Audio S/PDIF Alternative Interfaces

Pin #	Pin Name	Pin Type	Description
AB30, AC31, AA25, AC25	SPDIFI	I, CMOS	S/PDIF input
AA30, AC30, AA26, AF30	SPDIFO	O, CMOS	S/PDIF output

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Table 26. SM Audio Interface (PDM)

Pin #	Pin Name	Pin Type	Description
A21, AA26, AD30, D22, U30	SM_PDM_CLKIO	O, CMOS	PDM Clock out
AC25, B22, F19, V30	SM_PDM_DI[0]	I, CMOS	PDM Data in channel 0

Table 27. SoC Audio Interface (PDM)

Pin #	Pin Name	Pin Type	Description
AB28, AC27	PDM_DI[1]	I, CMOS	PDM Data in channel 1
AE30, AG29	PDM_DI[2]	I, CMOS	PDM Data in channel 2
AF30, AF31	PDM_DI[3]	I, CMOS	PDM Data in channel 3

Table 28. xSPI Interface, OPT2

Pin #	Pin Name	Pin Type	Description
P28	SM_xSPI_CS0n	O, CMOS	xSPI chip select 0.
L29	SM_xSPI_CS1n	O, CMOS	xSPI chip select 1 for second device.
M27	SM_xSPI_CLK	O, CMOS	xSPI serial single ended/differential clock.
M29	SM_xSPI_CLKn	O, CMOS	xSPI serial differential clock. xSPI Loopback signal in none-DQS Mode.
P26	SM_xSPI_DQS	I/O, CMOS	xSPI read-write data strobe.
N31	SM_xSPI_DAT[0]	I/O, CMOS	xSPI data input/output.
M30	SM_xSPI_DAT[1]	I/O, CMOS	xSPI data input/output.
L31	SM_xSPI_DAT[2]	I/O, CMOS	xSPI data input/output.
L30	SM_xSPI_DAT[3]	I/O, CMOS	xSPI data input/output.
K29	SM_xSPI_DAT[4]	I/O, CMOS	xSPI data input/output.
J29	SM_xSPI_DAT[5]	I/O, CMOS	xSPI data input/output.
H30	SM_xSPI_DAT[6]	I/O, CMOS	xSPI data input/output.
H29	SM_xSPI_DAT[7]	I/O, CMOS	xSPI data input/output.

Table 29. USB 2.0 Interface, Port 0

Pin #	Pin Name	Pin Type	Description
AF2	USB2_0_Dp	I/O, Analog	USB 2.0 Data Positive.
AE2	USB2_0_Dn	I/O, Analog	USB 2.0 Data Negative.
AG2	USB2_0_REXT	I, Analog	USB external reference resistor. Connect a 200 ohm ±1% resistor to VSS.
AH3	USB2_0_VBUS	I, Analog	Connect an external 30 kohm ±1% series resistor to USB 2.0 VBUS.
AH2	USB2_0_ID	I, Analog	USB 2.0 Port ID pin. This pin should be left floating or connected to GND.

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Table 30. USB 2.0 Interface, Port 1

Pin #	Pin Name	Pin Type	Description
AD2	USB2_1_Dp	I/O, Analog	USB 2.0 Data Positive.
AC2	USB2_1_Dn	I/O, Analog	USB 2.0 Data Negative.
AE1	USB2_1_REXT	I, Analog	USB external reference resistor. Connect a 200 ohm ±1% resistor to VSS.
AC1	USB2_1_VBUS	I, Analog	Connect an external 30 kohm ±1% series resistor to USB 2.0 VBUS.

Table 31. eMMC 5.1 Interface

Pin #	Pin Name	Pin Type	Description
AG7	eMMC_CLK	O, CMOS	Output clock.
AF7	eMMC_CMD	I/O, CMOS	Command/Response.
AH8	eMMC_STRB	I, CMOS	Read Strobe
AG8	eMMC_RSTn	O, CMOS	Hardware reset.
AG3	eMMC_DAT[0]	I/O, CMOS	Data[0].
AG5	eMMC_DAT[1]	I/O, CMOS	Data[1].
AH5	eMMC_DAT[2]	I/O, CMOS	Data[2].
AF6	eMMC_DAT[3]	I/O, CMOS	Data[3].
AF10	eMMC_DAT[4]	I/O, CMOS	Data[4].
AG9	eMMC_DAT[5]	I/O, CMOS	Data[5].
AH10	eMMC_DAT[6]	I/O, CMOS	Data[6].
AG10	eMMC_DAT[7]	I/O, CMOS	Data[7].

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Table 32. MIPI-CSI Pins—SL2611, SL2613, SL2617, SL2619; SL2615 Hardware De-featured Tie-offs

Pin #	Pin Name	Pin Type	Description	SL2615 (De-featured tie-offs)
AE15	MIPI_CSI_AVDD1P8	PWR	Analog VDD 1.8V for MIPI CSI PHY.	GND
AD17	MIPI_CSI_AVDD (0.8V)	PWR	MIPI CSI Analog VDD 0.8V	VDD_CORE (0.8 V)
AH19	MIPI_CSI_CKp	I, Analog	MIPI CSI CLK positive.	GND or NC
AG19	MIPI_CSI_CKn	I, Analog	MIPI CSI CLK negative.	GND or NC
AH17	MIPI_CSI_D0p	I, Analog	MIPI CSI Data Lane 0 positive.	GND or NC
AG17	MIPI_CSI_D0n	I, Analog	MIPI CSI Data Lane 0 negative.	GND or NC
AG15	MIPI_CSI_D1p	I, Analog	MIPI CSI Data Lane 1 positive.	GND or NC
AG16	MIPI_CSI_D1n	I, Analog	MIPI CSI Data Lane 1 negative.	GND or NC
AC17	MIPI_CSI_REXT	I, Analog	MIPI CSI reference resistor connection. Connect to VSS via a 200 Ω when CSI enabled.	GND or NC (do not populate 200 Ω)
W25	CAMERA_MUTE	Id, CMOS	FORCE Camera MUTE selection. 0: No mute. 1: Mute Camera	—

Note: SL2615 - CSI not supported (hardware de-featured).

Table 33. Parallel Camera Interface (CAM) Pins, OPT3

Pin #	Pin Name	Pin Type	Description
AC31	CAM_PIXCLK	I, CMOS	Camera interface bit clock.
AC30	CAM_HSYNC	I, CMOS	Camera interface horizontal synchronization signal.
AA25	CAM_VSYNC	I, CMOS	Camera interface vertical synchronization signal.
AB28	CAM_DAT[0]	I, CMOS	Camera interface data 0 input.
AE30	CAM_DAT[1]	I, CMOS	Camera interface data 1 input.
AD30	CAM_DAT[2]	I, CMOS	Camera interface data 2 input.
AE24	CAM_DAT[3]	I, CMOS	Camera interface data 3 input.
AC25	CAM_DAT[4]	I, CMOS	Camera interface data 4 input.
AG28	CAM_DAT[5]	I, CMOS	Camera interface data 5 input.
AG29	CAM_DAT[6]	I, CMOS	Camera interface data 6 input.
AF31	CAM_DAT[7]	I, CMOS	Camera interface data 7 input.

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Table 34. RGMII Interface, 1.8V Interface, OPT2

Pin #	Pin Name	Pin Type	Description
C8	RGMII1_TXD[0]	O, CMOS	RGMII port 1 TX Data 0.
F10	RGMII1_TXD[1]	O, CMOS	RGMII port 1 TX Data 1.
C9	RGMII1_TXD[2]	O, CMOS	RGMII port 1 TX Data 2.
B9	RGMII1_TXD[3]	O, CMOS	RGMII port 1 TX Data 3.
B10	RGMII1_RXD[0]	I, CMOS	RGMII port 1 RX Data 0.
F13	RGMII1_RXD[1]	I, CMOS	RGMII port 1 RX Data 1.
D11	RGMII1_RXD[2]	I, CMOS	RGMII port 1 RX Data 2.
A9	RGMII1_RXD[3]	I, CMOS	RGMII port 1 RX Data 3.
B12	RGMII1_TXC	O, CMOS	RGMII port 1 TX Clock Output.
B13	RGMII1_TXCTL	O, CMOS	RGMII port 1 TX Control.
B11	RGMII1_RXC	I, CMOS	RGMII port 1 RX Clock Input.
C13	RGMII1_RXCTL	I, CMOS	RGMII port 1 RX Control.
A13	RGMII1_CLKOUT	O, CMOS	RGMII PHY Clock Reference Output.
F15	RGMII2_TXD[0]	O, CMOS	RGMII port 2 TX Data 0.
F17	RGMII2_TXD[1]	O, CMOS	RGMII port 2 TX Data 1.
C15	RGMII2_TXD[2]	O, CMOS	RGMII port 2 TX Data 2.
D15	RGMII2_TXD[3]	O, CMOS	RGMII port 2 TX Data 3.
B16	RGMII2_RXD[0]	I, CMOS	RGMII port 2 RX Data 0.
A16	RGMII2_RXD[1]	I, CMOS	RGMII port 2 RX Data 1.
C17	RGMII2_RXD[2]	I, CMOS	RGMII port 2 RX Data 2.
C19	RGMII2_RXD[3]	I, CMOS	RGMII port 2 RX Data 3.
A18	RGMII2_TXC	O, CMOS	RGMII port 2 TX Clock Output.
B19	RGMII2_TXCTL	O, CMOS	RGMII port 2 TX Control.
B17	RGMII2_RXC	I, CMOS	RGMII port 2 RX Clock Input.
B18	RGMII2_RXCTL	I, CMOS	RGMII port 2 RX Control.

Table 35. RMII Interface, Port 1, 1.8V, OPT3

Pin #	Pin Name	Pin Type	Description
C8	RMII1_TXD[0]	O, CMOS	RMII1_TXD[0] TX Data 0.
F10	RMII1_TXD[1]	O, CMOS	RMII1_TXD[1] TX Data 1.
B10	RMII1_RXD[0]	I, CMOS	RMII1_RXD[0] RX Data 0.
F13	RMII1_RXD[1]	I, CMOS	RMII1_RXD[1] RX Data 1.
B13	RMII1_TXEN	O, CMOS	RMII1_TXEN Transmit Enable Output.
B11	RMII1_CRSDV	I, CMOS	RMII1_CRSDV Carrier Sense/Receive Data Valid Input.
A13	RMII1_REFCLK	I/O, CMOS	RMII1_REFCLK PHY Clock Reference Output.

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Table 36. RMII Interface, Port 2, 1.8V Interface, OPT3, OTP5

Pin #	Pin Name	Pin Type	Description
C9	RMII2_TXD[0]	O, CMOS	RMII2_TXD[0] TX Data 0.
B9	RMII2_TXD[1]	O, CMOS	RMII2_TXD[1] TX Data 1.
D11	RMII2_RXD[0]	I, CMOS	RMII2_RXD[0] RX Data 0.
A9	RMII2_RXD[1]	I, CMOS	RMII2_RXD[1] RX Data 1.
C13	RMII2_TXEN	O, CMOS	RMII2_TXEN Transmit Enable Output.
B12	RMII2_CRSDV	I, CMOS	RMII2_CRSDV Carrier Sense/Receive Data Valid Input.
B14	RMII2_REFCLK	I/O, CMOS	RMII2_REFCLK PHY Clock Reference Output.

Table 37. Keyboard Alternative Interface

Pin #	Signal Name	Pin Type	Description
AC31, B4	KEY_ROW[0]	I, CMOS	Keyboard Row input.
AC30, B3	KEY_ROW[1]	I, CMOS	Keyboard Row input.
AA26, C6, C22, H30	KEY_ROW[2]	I, CMOS	Keyboard Row input.
AA25, F21, J29	KEY_ROW[3]	I, CMOS	Keyboard Row input.
A6, C21, K29	KEY_ROW[4]	I, CMOS	Keyboard Row input.
B6, B21, L29	KEY_ROW[5]	I, CMOS	Keyboard Row input.
D11, D22, P26, T31	KEY_ROW[6]	I, CMOS	Keyboard Row input.
A9, F19, T30	KEY_ROW[7]	I, CMOS	Keyboard Row input.
B12, B14	KEY_ROW[8]	I, CMOS	Keyboard Row input.
C13, C14	KEY_ROW[9]	I, CMOS	Keyboard Row input.
A21, C14, V30	KEY_COL[0]	I/O, CMOS	Keyboard Column driver.
B14, C6, T30	KEY_COL[1]	I/O, CMOS	Keyboard Column driver.
B3, L29	KEY_COL[2]	I/O, CMOS	Keyboard Column driver.
B4, K29	KEY_COL[3]	I/O, CMOS	Keyboard Column driver.
A6, AA25, J29	KEY_COL[4]	I/O, CMOS	Keyboard Column driver.
AA26, B6, H30	KEY_COL[5]	I/O, CMOS	Keyboard Column driver.
AC30, H29	KEY_COL[6]	I/O, CMOS	Keyboard Column driver.
AC31, C9	KEY_COL[7]	I/O, CMOS	Keyboard Column driver.

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Table 38. MIPI Display Serial (DSI) Interface

Pin #	Pin Name	Pin Type	Description
AA19	MIPI_DSI_REXT	O, Analog	MIPI DSI reference resistor connection. Connect to VSS via a 200 ohm resistor.
AF23	MIPI_DSI_CKp	O, Analog	MIPI DSI differential Clock positive output.
AF24	MIPI_DSI_CKn	O, Analog	MIPI DSI differential Clock negative output.
AG26	MIPI_DSI_D0p	I/O, Analog	MIPI DSI Data lane 0 positive.
AH26	MIPI_DSI_D0n	I/O, Analog	MIPI DSI Data lane 0 negative.
AH24	MIPI_DSI_D1p	I/O, Analog	MIPI DSI Data lane 1 positive.
AG24	MIPI_DSI_D1n	I/O, Analog	MIPI DSI Data lane 1 negative.
AG22	MIPI_DSI_D2p	I/O, Analog	MIPI DSI Data lane 2 positive.
AH22	MIPI_DSI_D2n	I/O, Analog	MIPI DSI Data lane 2 negative.
AG20	MIPI_DSI_D3p	I/O, Analog	MIPI DSI Data lane 3 positive.
AG21	MIPI_DSI_D3n	I/O, Analog	MIPI DSI Data lane 3 negative.

Table 39. SM General Purpose I/O Interface

Pin #	Pin Name	Pin Type	Description
V30	SM_GPIO[0]	I/O, CMOS	SM AON General purpose I/O.
T30	SM_GPIO[1]	I/O, CMOS	SM AON General purpose I/O.
U30	SM_GPIO[2]	I/O, CMOS	SM AON General purpose I/O.
C24	SM_GPIO[3]	I/O, CMOS	SM General purpose I/O.
A24	SM_GPIO[4]	I/O, CMOS	SM General purpose I/O.
B24	SM_GPIO[5]	I/O, CMOS	SM General purpose I/O.
B25	SM_GPIO[6]	I/O, CMOS	SM General purpose I/O.
T31	SM_GPIO[7]	I/O, CMOS	SM AON General purpose I/O.
U26	SM_GPIO[8]	I/O, CMOS	SM AON General purpose I/O.
G23	SM_GPIO[9]	I/O, CMOS	SM General purpose I/O.
F23	SM_GPIO[10]	I/O, CMOS	SM General purpose I/O.
D24	SM_GPIO[11]	I/O, CMOS	SM General purpose I/O.
U28	SM_GPIO[12]	I/O, CMOS	SM AON General purpose I/O.
U25	SM_GPIO[13]	I/O, CMOS	SM AON General purpose I/O.
P29	SM_GPIO[14]	I/O, CMOS	SM General purpose I/O.
P30	SM_GPIO[15]	I/O, CMOS	SM General purpose I/O.
R29	SM_GPIO[16]	I/O, CMOS	SM AON General purpose I/O.
N30	SM_GPIO[17]	I/O, CMOS	SM General purpose I/O.
P28	SM_GPIO[18]	I/O, CMOS	SM General purpose I/O.
N31	SM_GPIO[19]	I/O, CMOS	SM General purpose I/O.
M30	SM_GPIO[20]	I/O, CMOS	SM General purpose I/O.

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Pin #	Pin Name	Pin Type	Description
L31	SM_GPIO[21]	I/O, CMOS	SM General purpose I/O.
L30	SM_GPIO[22]	I/O, CMOS	SM General purpose I/O.
M27	SM_GPIO[23]	I/O, CMOS	SM General purpose I/O.
M29	SM_GPIO[24]	I/O, CMOS	SM General purpose I/O.
P26	SM_GPIO[25]	I/O, CMOS	SM General purpose I/O.
L29	SM_GPIO[26]	I/O, CMOS	SM General purpose I/O.
K29	SM_GPIO[27]	I/O, CMOS	SM General purpose I/O.
J29	SM_GPIO[28]	I/O, CMOS	SM General purpose I/O.
H30	SM_GPIO[29]	I/O, CMOS	SM General purpose I/O.
H29	SM_GPIO[30]	I/O, CMOS	SM General purpose I/O.
F19	SM_GPIO[31]	I/O, CMOS	SM General purpose I/O.
A21	SM_GPIO[32]	I/O, CMOS	SM General purpose I/O.
B21	SM_GPIO[33]	I/O, CMOS	SM General purpose I/O.
C21	SM_GPIO[34]	I/O, CMOS	SM General purpose I/O.
F21	SM_GPIO[35]	I/O, CMOS	SM General purpose I/O.
C22	SM_GPIO[36]	I/O, CMOS	SM General purpose I/O.
D22	SM_GPIO[37]	I/O, CMOS	SM General purpose I/O.
B22	SM_GPIO[38]	I/O, CMOS	SM General purpose I/O.

Table 40. General Purpose I/O Interface

Pin #	Pin Name	Pin Type	Description
AA31	GPIO[0]	I/O, CMOS	General purpose I/O.
AA29	GPIO[1]	I/O, CMOS	General purpose I/O.
AA30	GPIO[2]	I/O, CMOS	General purpose I/O.
W29	GPIO[3]	I/O, CMOS	General purpose I/O.
AB30	GPIO[4]	I/O, CMOS	General purpose I/O.
AC31	GPIO[5]	I/O, CMOS	General purpose I/O.
AC30	GPIO[6]	I/O, CMOS	General purpose I/O.
AA26	GPIO[7]	I/O, CMOS	General purpose I/O.
AA25	GPIO[8]	I/O, CMOS	General purpose I/O.
AB28	GPIO[9]	I/O, CMOS	General purpose I/O.
AE30	GPIO[10]	I/O, CMOS	General purpose I/O.
AD30	GPIO[11]	I/O, CMOS	General purpose I/O.
AE24	GPIO[12]	I/O, CMOS	General purpose I/O.
AC27	GPIO[13]	I/O, CMOS	General purpose I/O.
AF30	GPIO[14]	I/O, CMOS	General purpose I/O.
AC25	GPIO[15]	I/O, CMOS	General purpose I/O.

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Pin #	Pin Name	Pin Type	Description
AG30	GPIO[16]	I/O, CMOS	General purpose I/O.
AG28	GPIO[17]	I/O, CMOS	General purpose I/O.
AG29	GPIO[18]	I/O, CMOS	General purpose I/O.
AF31	GPIO[19]	I/O, CMOS	General purpose I/O.
AH28	GPIO[20]	I/O, CMOS	General purpose I/O.
AF27	GPIO[21]	I/O, CMOS	General purpose I/O.
AF28	GPIO[22]	I/O, CMOS	General purpose I/O.
B4	GPIO[23]	I/O, CMOS	General purpose I/O.
B3	GPIO[24]	I/O, CMOS	General purpose I/O.
C6	GPIO[25]	I/O, CMOS	General purpose I/O.
C5	GPIO[26]	I/O, CMOS	General purpose I/O.
A3	GPIO[27]	I/O, CMOS	General purpose I/O.
B2	GPIO[28]	I/O, CMOS	General purpose I/O.
A6	GPIO[29]	I/O, CMOS	General purpose I/O.
B6	GPIO[30]	I/O, CMOS	General purpose I/O.
C7	GPIO[31]	I/O, CMOS	General purpose I/O.
B7	GPIO[32]	I/O, CMOS	General purpose I/O.
C8	GPIO[33]	I/O, CMOS	General purpose I/O.
F10	GPIO[34]	I/O, CMOS	General purpose I/O.
C9	GPIO[35]	I/O, CMOS	General purpose I/O.
B9	GPIO[36]	I/O, CMOS	General purpose I/O.
B10	GPIO[37]	I/O, CMOS	General purpose I/O.
F13	GPIO[38]	I/O, CMOS	General purpose I/O.
D11	GPIO[39]	I/O, CMOS	General purpose I/O.
A9	GPIO[40]	I/O, CMOS	General purpose I/O.
B11	GPIO[41]	I/O, CMOS	General purpose I/O.
B12	GPIO[42]	I/O, CMOS	General purpose I/O.
B13	GPIO[43]	I/O, CMOS	General purpose I/O.
C13	GPIO[44]	I/O, CMOS	General purpose I/O.
A13	GPIO[45]	I/O, CMOS	General purpose I/O.
C14	GPIO[46]	I/O, CMOS	General purpose I/O.
B14	GPIO[47]	I/O, CMOS	General purpose I/O.
F15	GPIO[48]	I/O, CMOS	General purpose I/O.
F17	GPIO[49]	I/O, CMOS	General purpose I/O.
C15	GPIO[50]	I/O, CMOS	General purpose I/O.
D15	GPIO[51]	I/O, CMOS	General purpose I/O.
B16	GPIO[52]	I/O, CMOS	General purpose I/O.

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Pin #	Pin Name	Pin Type	Description
A16	GPIO[53]	I/O, CMOS	General purpose I/O.
C17	GPIO[54]	I/O, CMOS	General purpose I/O.
C19	GPIO[55]	I/O, CMOS	General purpose I/O.
B17	GPIO[56]	I/O, CMOS	General purpose I/O.
A18	GPIO[57]	I/O, CMOS	General purpose I/O.
B19	GPIO[58]	I/O, CMOS	General purpose I/O.
B18	GPIO[59]	I/O, CMOS	General purpose I/O.

Table 41. Power - 1.8V

Pin #	Pin Name	Pin Type	Description
AE21	AVPLL_AVDD1P8	PWR	Analog VDD 1.8V AVPLL supply.
F8	CPUPLL_AVDD1P8	PWR	Analog VDD 1.8V CPU PLL supply.
AC21	SYSPLL_AVDD1P8	PWR	Analog VDD 1.8V SYSPLL supply.
D27	SMTSEN_AVDD1P8	PWR	SM Analog VDD 1.8V for temperature sensor.
E28	SM_ADC_AVDD1P8	PWR	SM ADC Analog VDD 1.8V.
H21, H25, M25, R25, U23	SM_VDDIO1P8	PWR	SM VDDIO 1.8V I/O supply.
K27	SMPLL_AVDD1P8	PWR	Analog VDD 1.8V SMPLL supply.
J27	SMOSC_VDDIO1P8	PWR	SM Power for on-chip crystal oscillator.
F26	SMOTP_AVDD1P8	PWR	Analog VDD 1.8V OTP supply.
AC19	MIPI_DSI_AVDD1P8	PWR	Analog VDD 1.8V for MIPI DSI PHY.
AE15	MIPI_CSI_AVDD1P8	PWR	Analog VDD 1.8V for MIPI CSI PHY.
AA6	M0_AVDD1P8	PWR	Analog VDD 1.8V for DDR PHY.
AD11	eMMC_VDDIO1P8	PWR	eMMC 1.8V VDD I/O supply.
AD13	SDIO_VDDIO1P8	PWR	SDIO 1.8V VDD I/O supply.
L14, L15, L16, W23, AA23	VDDIO1P8	PWR	1.8V VDD I/O.

Table 42. Power - 3.3V

Pin #	Pin Name	Pin Type	Description
AD9	USB2_0_AVDD3P3	PWR	3.3V I/O supply for USB2-0.
AE9	USB2_0_VR_AVDD3P3	PWR	Analog VDD (3.3V) for USB2-0.
AD5	USB2_1_AVDD3P3	PWR	3.3V I/O supply for USB2-1.
AD3	USB2_1_VR_AVDD3P3	PWR	Analog VDD (3.3V) for USB2-1.

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Table 43. Power and Ground Pins

Pin #	Pin Name	Pin Type	Description
AD7	USB2_0_DVDD	PWR	USB 2.0 DVDD 0.8V.
AC5	USB2_1_DVDD	PWR	USB2.0 DVDD 0.8V.
AD17	MIPI_CSI_AVDD	PWR	MIPI CSI Analog VDD 0.8V.
AF19	MIPI_DSI_AVDD	PWR	MIPI DSI Analog VDD 0.8V.
J21, J23, L21, L23, N21, R21, U21	SM_VDD_CORE	PWR	SM VDD Core 0.8V.
J9, L9, N10, R9, T11, U9, W9, W10	VDDQ	PWR	I/O power: LPDDR4 at 1.1V, DDR4 1.2V, DDR3L 1.35V.
L10, L11, N12, P12, T12	VDDQLP (Note 2)	PWR	I/O power: LPDDR4x at 0.6V.
AA13, AA15, J13, J15, J17, J19, L18, L19, N14, N15, N19, R14, R15, R19, U13, U17, U19, W13, W17, W19, W21	VDD_CORE	PWR	Core voltage.
E7	VDD_CORE_FB	PWR	Core voltage feedback compensation.
D28	SM_ADC_AVSS	GND	SM ADC analog ground
A2, A11, A26, A30, AA8, AA10, AA11 AA17, AA21, AA24, AA28, AB5, AB27, AC3, AC7, AC9, AC11, AC13, AC15, AC24, AD4, AD15, AD21, AD29, AE10, AE12, AE19, AE27, AF3, AF5, AF15, AF17, AF20, AF22, AF26, AF29, AG1, AG31, AH15, AH30, B1, B31, C20, D3, D9, D14, D17, D21, D26, D31, E6, F11, F25, F28, G3, G8, G13, G15, G17, G19, G21, G30, H26, H28, J4, J8, J10, J11, J18, J20, K25, L3, L8, L12, L17, L20, L25, N4, N9, N16, N17, N20, N23, P11, P25, R6, R8, R17, R20, R23, R26, R28, U4, U8, U11, U12, U15, U20, W4, W8, W11, W12, W15, W28, Y6, Y17	VSS	GND	Core ground.

2. When not in LPDDR4x => VDDQLP must tie to VDDQ.

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3.3. Pin Multiplexing

3.3.1. Pin Multiplexing Signal Descriptions

For complete pin multiplexing details, refer to 3.3.2 Pin Multiplexing Modes.

Table 44. SoC Reset Strapping

Pin #	Pin Mux Name	Primary Pin Name	Pin Type	Description
B13	SOFTWARE_STRAP[0]	GPIO[43]	PU-boot	Strap for software usage.
AF27	SOFTWARE_STRAP[1]	GPIO[21]	PD-boot	Strap for software usage.
C8	SOFTWARE_STRAP[2]	GPIO[33]	PD-boot	Strap for software usage.
B9	SOFTWARE_STRAP[3]	GPIO[36]	PD-boot	Strap for software usage.
N30	PLLBYPS	SM_GPIO[17]/SM_URT1_TXD	PD-boot	SYS/MEM/CPU PLL bypass. • 0: No bypass. • 1: All PLL bypassed.
C5	CPURSTBYPS	GPIO[26]	PD-boot	CPU reset bypass strap. • 0: Enable reset logic inside CPU partition. • 1: Bypass reset logic inside CPU partition.
U26	BOOT_SRC[0]	SM_GPIO[8]/SM_URT0_TXD	PU-boot	CPU boot source bit 0. BOOT_SRC[1:0]: • 00: ROM boot from USB2_0. • 01: ROM boot from xSPI NOR • 10: ROM boot from eMMC. • 11: ROM boot from xSPI NAND
G23	BOOT_SRC[1]	SM_GPIO[9]/SM_SPI1_SDO	PD-boot	CPU boot source bit 1.

1. PU-boot or PD-boot indicates built-in weak pull-up or pull-down that can be disabled by software after boot up.

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3.3.2. Pin Multiplexing Modes

This section describes the various modes related to the multiplexed pins. The primary pin name reflects the pinout name, while the Mode 0, Mode 1, ..., Mode 7 and Strap multiplex names are located in the respective columns.

Figure 8 shows the multiplexed pin naming scheme that is used for the Multiplexed pins.

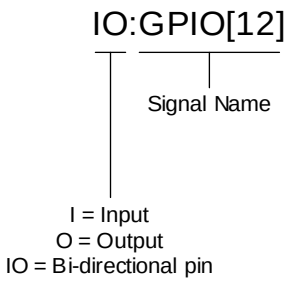

Figure 8. Example of the Multiplexed Pin Naming Scheme

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Table 45. SM and SoC Multiplexing

Pin #	Primary Pin Name	OPT 1	OPT 2	OPT 3	OPT 4	OPT 5	OPT 6	OPT 7	OPT 8	Strap	Pull State [1,2]	AON
T29	SM_AUDIO_MUTE	SM_AUDIO_MUTE	—	—	—	—	—	—	—	—	PD	—
V31	SM_POR_EN	SM_POR_EN	—	—	—	—	—	—	—	—	PU	1
U29	SM_RSTn	SM_RSTn	—	—	—	—	—	—	—	—	PU	1
W30	SM_TCK	SM_TCK	—	—	—	—	—	—	—	—	PD	1
W26	SM_TRSTn	SM_TRSTn	—	—	—	—	—	—	—	—	PD	1
V30	SM_GPIO[0]	SM_TMS	SM_GPIO[0]	SM_URT0_TXD	KEY_COL[0]	—	SM_PDM_DI[0]	SM_sPWM[10]	—	—	PUBoot	1
T30	SM_GPIO[1]	SM_TDI	SM_GPIO[1]	SM_URT0_RXD	KEY_COL[1]	GPIO_TRIG[0]	SM_sPWM[9]	KEY_ROW[7]	—	—	PUBoot	1
U30	SM_GPIO[2]	SM_TDO	SM_GPIO[2]	SM_PDM_CLKIO	I2S2_MCLK	—	—	SM_sPWM[11]	—	—	PUBoot	1
C24	SM_GPIO[3]	SM_GPIO[3]	SM_SPI1_SS0n	SM_TW1_SCL	SM_sPWM[8]	SM_I3C_MS_SCL	—	—	—	—	—	—
A24	SM_GPIO[4]	SM_GPIO[4]	SM_SPI1_SS1n	SM_TW1_SDA	SM_sPWM[0]	SM_I3C_MS_SDA	—	—	—	—	—	—
B24	SM_GPIO[5]	SM_GPIO[5]	SM_SPI1_SS2n	—	SM_sPWM[1]	—	—	—	—	dft_jtag_sel	PDBoot	—
B25	SM_GPIO[6]	SM_GPIO[6]	SM_SPI1_SS3n	SM_SPI1S_SSn	SM_sPWM[2]	—	—	—	—	—	—	—
T31	SM_GPIO[7]	SM_GPIO[7]	SM_URT0_RXD	SM_CAN0_RX	KEY_ROW[6]	GPIO_TRIG[2]	SM_sPWM[9]	SM_URT1_RXD	—	—	—	1
U26	SM_GPIO[8]	SM_GPIO[8]	SM_URT0_TXD	SM_CAN0_TX	SM_CLKOUT	—	—	SM_URT1_TXD	—	boot_src[0]	PUBoot	1
G23	SM_GPIO[9]	SM_GPIO[9]	SM_SPI1_SDO	SM_SPI1S_SDO	SM_sPWM[3]	—	—	—	—	boot_src[1]	PDBoot	—
F23	SM_GPIO[10]	SM_GPIO[10]	SM_SPI1_SCLK	SM_SPI1S_SCLK	SM_sPWM[4]	—	—	—	—	—	—	—
D24	SM_GPIO[11]	SM_GPIO[11]	SM_SPI1_SDI	SM_SPI1S_SDI	SM_sPWM[5]	—	—	—	—	—	—	—
U28	SM_GPIO[12]	SM_GPIO[12]	SM_TW0_SCL	SM_I3C_MS_SCL	SM_sPWM[6]	—	—	—	MCU_DBG_CLK	—	—	1
U25	SM_GPIO[13]	SM_GPIO[13]	SM_TW0_SDA	SM_I3C_MS_SDA	SM_CLKOUT	—	—	—	MCU_DBG_OUT[0]	—	—	1
P29	SM_GPIO[14]	SM_GPIO[14]	SM_TW1_SCL	SM_URT0_CTSn	SM_sPWM[10]	SM_CAN0_RX	—	SM_URT1_CTSn	MCU_DBG_OUT[1]	—	—	—
P30	SM_GPIO[15]	SM_GPIO[15]	SM_TW1_SDA	SM_URT0_RTSn	SM_sPWM[11]	SM_CAN0_TX	—	SM_URT1_RTSn	MCU_DBG_OUT[2]	—	—	—
R29	SM_GPIO[16]	SM_GPIO[16]	SM_URT1_RXD	SM_CAN0_RX	SM_sPWM[7]	—	—	—	—	—	—	1
N30	SM_GPIO[17]	SM_GPIO[17]	SM_URT1_TXD	SM_CAN0_TX	SM_sPWM[8]	—	—	SM_URT0_TXD	—	pll_bypass	PDBoot	—
P28	SM_GPIO[18]	SM_GPIO[18]	SM_xSPI_CS0n	—	—	—	—	—	—	—	—	—
N31	SM_GPIO[19]	SM_GPIO[19]	SM_xSPI_DAT[0]	—	—	—	—	—	—	—	—	—
M30	SM_GPIO[20]	SM_GPIO[20]	SM_xSPI_DAT[1]	—	—	—	—	—	—	—	—	—
L31	SM_GPIO[21]	SM_GPIO[21]	SM_xSPI_DAT[2]	—	—	—	—	—	—	—	—	—
L30	SM_GPIO[22]	SM_GPIO[22]	SM_xSPI_DAT[3]	—	—	—	—	—	—	—	—	—
M27	SM_GPIO[23]	SM_GPIO[23]	SM_xSPI_CLK	—	—	—	—	—	—	—	—	—

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Pin #	Primary Pin Name	OPT 1	OPT 2	OPT 3	OPT 4	OPT 5	OPT 6	OPT 7	OPT 8	Strap	Pull State [1,2]	AON
M29	SM_GPIO[24]	SM_GPIO[24]	SM_xSPI_CLKn	—	—	—	—	—	—	—	—	—
P26	SM_GPIO[25]	SM_GPIO[25]	SM_xSPI_DQS	—	—	—	—	KEY_ROW[6]	—	—	—	—
L29	SM_GPIO[26]	SM_GPIO[26]	SM_xSPI_CS1n	SM_URT2_TXD	KEY_COL[2]	SM_URT3_RTSn	SM_URT3_DE	KEY_ROW[5]	SM_CLKOUT	—	—	—
K29	SM_GPIO[27]	SM_GPIO[27]	SM_xSPI_DAT[4]	SM_URT2_RXD	KEY_COL[3]	SM_URT3_CTSn	SM_URT3_REn	KEY_ROW[4]	—	—	—	—
J29	SM_GPIO[28]	SM_GPIO[28]	SM_xSPI_DAT[5]	SM_URT3_TXD	KEY_COL[4]	SM_URT2_RTSn	SM_URT0_RTSn	KEY_ROW[3]	SM_URT1_RTSn	—	—	—
H30	SM_GPIO[29]	SM_GPIO[29]	SM_xSPI_DAT[6]	SM_URT3_RXD	KEY_COL[5]	SM_URT2_CTSn	SM_URT0_CTSn	KEY_ROW[2]	SM_URT1_CTSn	—	—	—
H29	SM_GPIO[30]	SM_GPIO[30]	SM_xSPI_DAT[7]	—	KEY_COL[6]	—	—	—	SM_CLKOUT	—	—	—
F19	SM_GPIO[31]	SM_GPIO[31]	SM_sPWM[0]	SM_URT1_RXD	KEY_ROW[7]	SM_PDM_DI[0]	SM_URT0_RXD	SM_CAN1_RX	—	—	—	—
A21	SM_GPIO[32]	SM_GPIO[32]	SM_sPWM[1]	SM_URT1_TXD	KEY_COL[0]	SM_PDM_CLKIO	SM_URT0_TXD	SM_CAN1_TX	—	—	—	—
B21	SM_GPIO[33]	SM_GPIO[33]	SM_sPWM[2]	—	SM_URT2_TXD	SM_URT3_RTSn	KEY_ROW[5]	SM_URT3_DE	—	—	—	—
C21	SM_GPIO[34]	SM_GPIO[34]	SM_sPWM[3]	—	SM_URT2_RXD	SM_URT3_CTSn	KEY_ROW[4]	SM_URT3_REn	—	—	—	—
F21	SM_GPIO[35]	SM_GPIO[35]	SM_sPWM[4]	SM_URT1_RTSn	SM_URT3_TXD	SM_URT2_RTSn	KEY_ROW[3]	SM_URT0_RTSn	—	—	—	—
C22	SM_GPIO[36]	SM_GPIO[36]	SM_sPWM[5]	SM_URT1_CTSn	SM_URT3_RXD	SM_URT2_CTSn	KEY_ROW[2]	SM_URT0_CTSn	—	—	—	—
D22	SM_GPIO[37]	SM_GPIO[37]	SM_sPWM[6]	—	SM_TWO_SCL	KEY_ROW[6]	SM_PDM_CLKIO	—	—	—	—	—
B22	SM_GPIO[38]	SM_GPIO[38]	SM_sPWM[7]	—	SM_TWO_SDA	—	SM_PDM_DI[0]	—	—	—	—	—
AA31	GPIO[0]	GPIO[0]	I2S1_LRCK	—	—	—	—	—	SPI3_SS0n	—	—	—
AA29	GPIO[1]	GPIO[1]	I2S1_BCLK	—	—	—	—	—	SPI3_SCLK	—	—	—
AA30	GPIO[2]	GPIO[2]	I2S1_DO	—	—	SPDIFO	—	—	SPI3_SDO	—	—	—
W29	GPIO[3]	GPIO[3]	I2S1_MCLK	—	—	—	—	—	SPI3_SS1n	—	—	—
AB30	GPIO[4]	GPIO[4]	I2S1_DI	—	—	SPDIFI	—	—	SPI3_SDI	—	—	—
AC31	GPIO[5]	GPIO[5]	I2S2_LRCK	CAM_PIXCLK	KEY_ROW[0]	SPDIFI	—	KEY_COL[7]	—	—	—	—
AC30	GPIO[6]	GPIO[6]	I2S2_BCLK	CAM_HSYNC	KEY_ROW[1]	SPDIFO	—	KEY_COL[6]	—	—	—	—
AA26	GPIO[7]	GPIO[7]	I2S2_DO	—	KEY_ROW[2]	SPDIFO	SM_PDM_CLKIO	KEY_COL[5]	—	—	—	—
AA25	GPIO[8]	GPIO[8]	I2S2_DI	CAM_VSYNC	KEY_ROW[3]	SPDIFI	—	KEY_COL[4]	—	—	—	—
AB28	GPIO[9]	GPIO[9]	—	CAM_DAT[0]	—	PDM_DI[1]	—	—	—	—	—	—
AE30	GPIO[10]	GPIO[10]	—	CAM_DAT[1]	—	PDM_DI[2]	DSI_TE	—	—	—	—	—
AD30	GPIO[11]	GPIO[11]	I2S2_MCLK	CAM_DAT[2]	—	SM_PDM_CLKIO	—	—	DBG_CLK	—	—	—
AE24	GPIO[12]	GPIO[12]	I2S3_LRCK	CAM_DAT[3]	SDIO2_WP	SDIO1_WP	—	—	DBG_OUT[0]	—	—	—
AC27	GPIO[13]	GPIO[13]	I2S3_BCLK	PDM_DI[1]	RGMII_PTP_PPS_O	USB2_DRV_VBUS	—	—	DBG_OUT[1]	—	—	—
AF30	GPIO[14]	GPIO[14]	I2S3_DO	—	—	PDM_DI[3]	—	SPDIFO	DBG_OUT[2]	—	—	—
AC25	GPIO[15]	GPIO[15]	I2S3_DI	CAM_DAT[4]	—	SM_PDM_DI[0]	—	SPDIFI	DBG_OUT[3]	—	—	—

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Pin #	Primary Pin Name	OPT 1	OPT 2	OPT 3	OPT 4	OPT 5	OPT 6	OPT 7	OPT 8	Strap	Pull State [1,2]	AON
AG30	GPIO[16]	GPIO[16]	SPI2_SS0n	—	SDIO2_DAT[3]	—	—	—	—	—	—	—
AG28	GPIO[17]	GPIO[17]	SPI2_SS1n	CAM_DAT[5]	SDIO2_DAT[2]	—	DSI_TE	—	—	—	—	—
AG29	GPIO[18]	GPIO[18]	SPI2_SS2n	CAM_DAT[6]	SDIO2_DAT[1]	PDM_DI[2]	SM_CAN1_RX	—	—	—	—	—
AF31	GPIO[19]	GPIO[19]	SPI2_SS3n	CAM_DAT[7]	SDIO2_DAT[0]	PDM_DI[3]	SM_CAN1_TX	—	—	—	—	—
AH28	GPIO[20]	GPIO[20]	SPI2_SDO	—	SDIO2_CMD	—	—	—	—	—	—	—
AF27	GPIO[21]	GPIO[21]	SPI2_SCLK	—	SDIO2_CLK	—	CLKOUT	—	—	software_strap[1]	PDBoot	—
AF28	GPIO[22]	GPIO[22]	SPI2_SDI	—	SDIO2_CDn	SDIO1_CDn	—	—	—	—	—	—
B4	GPIO[23]	GPIO[23]	TW2_SCL	RGMII_MDC	KEY_ROW[0]	—	SPI3_SS2n	KEY_COL[3]	DBG_OUT[4]	—	—	—
B3	GPIO[24]	GPIO[24]	TW2_SDA	RGMII_MDIO	KEY_ROW[1]	—	SPI3_SS3n	KEY_COL[2]	DBG_OUT[5	—	—	—
C6	GPIO[25]	GPIO[25]	URT5_RXD	GPIO_TRIG1	KEY_ROW[2]	SM_URT1_RXD	—	KEY_COL[1]	DBG_OUT[6]	—	—	—
C5	GPIO[26]	GPIO[26]	URT5_TXD	RGMII_PTP_PPS_O	—	SM_URT1_TXD	USB2_DRV_VBUS [3]	—	DBG_OUT[7]	cpu_rst_bypass	PDBoot	
A3	GPIO[27]	GPIO[27]	TW3_SCL	URT4_TXD	—	SM_URT1_RTSn	—	—	—	—	—	—
B2	GPIO[28]	GPIO[28]	TW3_SDA	URT4_RXD	—	SM_URT1_CTSn	—	—	—	—	—	—
A6	GPIO[29]	GPIO[29]	—	URT4_DE	KEY_ROW[4]	SM_URT1_RXD	—	KEY_COL[4]	SPI4_SDI	—	—	—
B6	GPIO[30]	GPIO[30]	—	URT4_REn	KEY_ROW[5]	SM_URT1_TXD	—	KEY_COL[5]	SPI4_SCLK	—	—	—
C7	GPIO[31]	GPIO[31]	—	RGMII_MDC	—	—	SPI5_SS3n	SPI3_SS2n	SPI4_SS2n	—	—	—
B7	GPIO[32]	GPIO[32]	—	RGMII_MDIO	—	—	—	SPI3_SS3n	SPI4_SS3n	—	—	—
C8	GPIO[33]	GPIO[33]	RGMII1_TXD[0]	RMII1_TXD[0]	—	—	SM_CAN0_TX	SPI3_SS1n	SPI4_SS1n	software_strap[2]	PDBoot	
F10	GPIO[34]	GPIO[34]	RGMII1_TXD[1]	RMII1_TXD[1]	—	—	SM_CAN0_RX	—	—	—	—	—
C9	GPIO[35]	GPIO[35]	RGMII1_TXD[2]	RMII2_TXD[0]	KEY_COL[7]	URT5_RXD	—	—	SPI4_SS0n	—	—	—
B9	GPIO[36]	GPIO[36]	RGMII1_TXD[3]	RMII2_TXD[1]	—	URT5_TXD	—	—	SPI4_SDO	software_strap[3]	PDBoot	—
B10	GPIO[37]	GPIO[37]	RGMII1_RXD[0]	RMII1_RXD[0]	—	—	SM_CAN1_TX	—	SPI5_SDI	—	—	—
F13	GPIO[38]	GPIO[38]	RGMII1_RXD[1]	RMII1_RXD[1]	—	—	SM_CAN1_RX	—	SPI5_SDO	—	—	—
D11	GPIO[39]	GPIO[39]	RGMII1_RXD[2]	RMII2_RXD[0]	KEY_ROW[6]	URT6_RXD	SPI5_SS1n	SPI4_SS3n	—	—	—	—
A9	GPIO[40]	GPIO[40]	RGMII1_RXD[3]	RMII2_RXD[1]	KEY_ROW[7]	URT6_TXD	SPI5_SS2n	SPI4_SS2n	—	—	—	—
B11	GPIO[41]	GPIO[41]	RGMII1_RXC	RMII1_CRSDV	—	—	—	—	SPI5_SCLK	—	—	—
B12	GPIO[42]	GPIO[42]	RGMII1_TXC	RMII2_CRSDV	KEY_ROW[8]	URT7_RXD	—	SPI4_SCLK	—	—	—	—
B13	GPIO[43]	GPIO[43]	RGMII1_TXCTL	RMII1_TXEN	—	—	—	SPI4_SS0n	—	software_strap[0]	PUBoot	—
C13	GPIO[44]	GPIO[44]	RGMII1_RXCTL	RMII2_TXEN	KEY_ROW[9]	URT7_TXD	—	SPI4_SDI	—	—	—	—
A13	GPIO[45]	GPIO[45]	RGMII1_CLKOUT	RMII1_REFCLK	—	—	—	—	—	—	—	—
C14	GPIO[46]	GPIO[46]	SDIO1_CDn	SDIO2_CDn	KEY_COL[0]	—	SM_URT1_RTSn	KEY_ROW[9]	DSI_TE	—	—	—

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Pin #	Primary Pin Name	OPT 1	OPT 2	OPT 3	OPT 4	OPT 5	OPT 6	OPT 7	OPT 8	Strap	Pull State [1,2]	AON
B14	GPIO[47]	GPIO[47]	SDIO1_Wp	SDIO2_Wp	KEY_COL[1]	RMII2_REFCLK	SM_URT1_CTSn	KEY_ROW[8]	—	—	—	—
F15	GPIO[48]	GPIO[48]	RGMII2_TXD[0]	—	—	—	SPI5_SSOn	SPI4_SS2n	SPI3_SS3n	—	—	—
F17	GPIO[49]	GPIO[49]	RGMII2_TXD[1]	—	—	—	SPI5_SDO	SPI4_SS3n	SPI3_SS2n	—	—	—
C15	GPIO[50]	GPIO[50]	RGMII2_TXD[2]	—	—	—	SPI5_SCLK	—	SPI3_SS1n	—	—	—
D15	GPIO[51]	GPIO[51]	RGMII2_TXD[3]	—	—	—	—	—	SPI3_SSOn	—	—	—
B16	GPIO[52]	GPIO[52]	RGMII2_RXD[0]	—	—	—	—	SPI4_SS2n	SPI3_SDO	—	—	—
A16	GPIO[53]	GPIO[53]	RGMII2_RXD[1]	—	—	—	—	SPI4_SS3n	SPI3_SCLK	—	—	—
C17	GPIO[54]	GPIO[54]	RGMII2_RXD[2]	—	—	—	—	—	SPI3_SDI	—	—	—
C19	GPIO[55]	GPIO[55]	RGMII2_RXD[3]	—	—	—	SPI5_SDI	—	SPI4_SS1n	—	—	—
B17	GPIO[56]	GPIO[56]	RGMII2_RXC	—	—	—	—	—	SPI4_SSOn	—	—	—
A18	GPIO[57]	GPIO[57]	RGMII2_TXC	—	—	—	—	—	SPI4_SDO	—	—	—
B19	GPIO[58]	GPIO[58]	RGMII2_TXCTL	—	—	—	—	—	SPI4_SCLK	—	—	—
B18	GPIO[59]	GPIO[59]	RGMII2_RXCTL	—	—	—	—	—	SPI4_SDI	—	—	—

1. Could be used to hold PU/PD state during AON.
2. PU/PD: Always ON. PUBoot/PDBoot: Always pulled after reset, but software can disable them afterward.
3. Used as GPIO.
4. SM_GPIO5 – restrict usage to output only, recommend using it as active low for VDD_CORE power enable (used in BOOT-ROM).
5. SM_GPIO24 – restrict usage to output only, recommend using it as active low signal e.g. as a reset signal (used in BOOT-ROM).
6. SM_xSPI_DQS / SM_GPIO[25] – output during ROM-BOOT in xSPI boot mode. Note that the default pinmux in xSPI boot is “xSPI-OPT2”.
7. SM_xSPI_CS1n / SM_GPIO[26] – output during ROM-BOOT in xSPI boot mode. Note that the default pinmux in xSPI boot is “xSPI-OPT2”.

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4. Electrical Specifications

4.1. Absolute Maximum Ratings

Stresses above those listed in the Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 46. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
AVDD1P8	All analog supply voltage at 1.8V	-0.3	—	1.98	
M0_AVDD1P8	Memory 1.8V supply voltage	-0.3	—	1.98	V
VDDIO1P8	All IO supply voltage at 1.8V	-0.3	—	1.98	
AVDD3P3	All USB AVDD3P3 3.3V supply voltage	-0.3	—	3.63	
SM_VDD_CORE	SM Core supply voltage	-0.1	—	0.96	
AVDD	All analog supply voltage at 0.8V	-0.1	—	1.12	
DVDD	All USB DVDD 0.8V core supply voltage	-0.1	—	1.12	
VDD_CORE	Core supply voltage	-0.1	—	1.12	
VDDQ	DDR3L/DDR4/LPDDR4 supply voltage	-0.5	—	1.485	
VDDQLP	LPDDR4x I/O power (Note 3)	-0.3	—	1.485	
V_{IN}	TW0_SCL, TW0_SDA, TW1_SCL, TW1_SDA, TW2_SCL, TW2_SDA, TW3_SCL, TW3_SDA	-0.3	—	1.98	
	Other 1.8V digital I/O pins	-0.3	—	1.98 or VDDIO1P8+0.3, whichever is lower	
V_{OUT}	TW0_SCL, TW0_SDA, TW1_SCL, TW1_SDA, TW2_SCL, TW2_SDA, TW3_SCL, TW3_SDA	-0.3	—	1.98	
	Other 1.8V digital I/O pins	-0.3	—	1.98 or VDDIO1P8+0.3, whichever is lower	
$T_{STORAGE}$	Storage temperature	-55	—	125 (Note 1)	°C
I_{DIS}	VDD_CORE_FB discharge current (Note 2)	—	—	5	mA

1. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.
2. Recommend disabling external fast discharge current at VDD_CORE_FB. Max discharging current to VDD_CORE_FB should be less or equal to 5mA.
3. When not in LPDDR4x => VDDQLP must tie to VDDQ.

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4.2. Recommended Operating Conditions

Table 47. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
AVDD1P8	All analog supply voltage at 1.8V	—	1.71	1.8	1.89	V
MO_AVDD1P8	Memory 1.8V supply voltage	—	1.71	1.8	1.89	
VDDIO1P8	All IO supply voltage at 1.8V	—	1.71	1.8	1.89	
AVDD3P3	All USB AVDD3P3 at 3.3V supply voltage	—	3.135	3.3	3.465	
SM_VDD_CORE	SM Core supply voltage	—	0.72	0.8	0.88	
AVDD	All analog supply voltage at 0.8V	Consumer	0.72	—	0.945	
		Industrial	TBD	—	TBD	
DVDD	All USB DVDD 0.8V core supply voltage	Consumer	0.72	—	0.945	
		Industrial	TBD	—	TBD	
VDD_CORE (Note 1)	Core supply voltage	Consumer	0.72	0.8	0.945	
		Industrial	TBD	0.8	TBD	
VDDQ	I/O supply for DDR3L at 1.35V	—	1.283	1.35	1.418	
	I/O supply for DDR4 at 1.2V	—	1.14	1.2	1.26	
	I/O supply for LPDDR4 at 1.1V	—	1.06	1.1	1.17	
VDDQLP (Note 3)	I/O supply for LPDDR4x at 0.6V	—	0.57	0.6	0.63	
fCLKi	Reference crystal frequency	—	—	25	—	MHz
TA (Note 2)	Ambient operating temperature	Consumer	0	—	70	°C
		Industrial	-40	—	85	°C
TJ	Junction temperature	Consumer	0	—	105	°C
		Industrial	-40	—	125	°C
RUSB2_REXT	USB 2.0 PHY reference current resistor, connect to AVSS	—	—	200± 1%	—	Ohm
RUSB2_VBUS_REXT	USB 2.0 PHY VBUS external series resistor	—	—	30k± 1%	—	Ohm
RMIPI DSI REXT	MIPI DSI reference current resistor, connect to VSS	—	—	200± 1%	—	Ohm
RMIPI CSI REXT	MIPI CSI reference current resistor, connect to VSS	—	—	200± 1%	—	Ohm
RMO_CAL	DDR3L/DDR4 reference current resistor, connect to VSS. For LPDDR4/4x connect to 1.1V VDDQ or 0.6V VDDLQ respectively.	—	—	120± 1%	—	Ohm

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1. The optimum core supply voltage is determined by the individual chip manufacturing process variation. The system software reads an index stored in the on-chip OTP memory and controls the VDD regulator output voltage. The nominal regulation of the VDD regulator should be within ±3%. For details refer to the *PV Compensation Application Note*.
2. The important parameter is maximum junction temperature. The maximum junction temperature needs to be observed in addition to the ambient temperature limits.
3. When not in LPDDR4x, mode, the VDDQLP supply pins should be tied to the VDDQ supply.

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4.3. AC and DC Electrical Characteristics

4.3.1. Digital Pins Operating Conditions

4.3.1.1. Digital Pins Operating Conditions for 1.8 V I/Os

Table 48 describes the digital operating conditions for 1.8V I/Os.

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 48. Digital Operating Conditions for 1.8 V I/Os

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	All 1.8V Digital IO pins	—	0.65*VDDIO1P8	—	1.98	V
V_{IL}	Low level input voltage	All 1.8V Digital IO pins	—	-0.3	—	0.35*VDDIO1P8	
V_{T+}	Low to High Threshold Point with Schmitt Trigger enabled	All 1.8V Digital I/O Signals	—	0.98	1.09	1.21	
		SM_TRSTn, SM_TCK, SM_RSTn, SM_POR_EN, SM_AUDIO_MUTE, CAMERA_MUTE	—	0.95	1.06	1.16	
		SDIO_DAT[3:0]	—	1.07	—	—	
		SDIO_CMD					
		eMMC_DAT[7:0]	—	1.07	—	—	
		eMMC_CMD					
		eMMC_STRB					
V_{T-}	High to Low Threshold Point with Schmitt Trigger enabled	All 1.8V Digital I/O Signals	—	0.76	0.86	0.97	
		SM_TRSTn, SM_TCK, SM_RSTn, SM_POR_EN, SM_AUDIO_MUTE, CAMERA_MUTE	—	0.68	0.76	0.85	
		SDIO_DAT[3:0]	—	—	—	0.68	
		SDIO_CMD					
		eMMC_DAT[7:0]	—	—	—	0.68	
		eMMC_CMD					
		eMMC_STRB					

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Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
R_{PU}	Pull-up Resistor	All 1.8V Digital I/O Signals	—	32k	48k	79k	Ohm
		SM_TRSTn, SM_TCK, SM_RSTn, SM_POR_EN, SM_AUDIO_MUTE, CAMERA_MUTE	—	57k	87k	146k	
R_{PD}	Pull-down Resistor	All 1.8V Digital I/O Signals	—	30k	44k	68k	
		SM_TRSTn, SM_TCK, SM_RSTn, SM_POR_EN, SM_AUDIO_MUTE, CAMERA_MUTE	—	54k	79k	127k	
I_{OL} @ 0.45V	DS[3:0]=0000	All 1.8V Digital I/O pins	—	0.7	1.1	1.4	mA
	DS[3:0]=0001			1.1	1.6	2.1	
	DS[3:0]=0010			2.2	3.2	4.1	
	DS[3:0]=0011			3.3	4.8	6.2	
	DS[3:0]=0100			4.4	6.4	8.2	
	DS[3:0]=0101			5.5	7.9	10.2	
	DS[3:0]=0110			6.6	9.5	12.3	
	DS[3:0]=0111			7.7	11.1	14.3	
	DS[3:0]=1000			8.8	12.6	16.2	
	DS[3:0]=1001			9.8	14.2	18.3	
	DS[3:0]=1010			10.9	15.8	20.3	
	DS[3:0]=1011			12	17.4	22.3	
	DS[3:0]=1100			13.1	18.8	24.1	
	DS[3:0]=1101			14.2	20.4	26.1	
	DS[3:0]=1110			15.2	22	28.1	
	DS[3:0]=1111			16.3	23.5	30.1	

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Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{OH} @ VDDIO-0.45V	DS[3:0]=0000	All 1.8V Digital I/O pins	—	0.7	1.1	1.5	mA
	DS[3:0]=0001			1.1	1.7	2.3	
	DS[3:0]=0010			2.2	3.3	4.5	
	DS[3:0]=0011			3.2	5	6.7	
	DS[3:0]=0100			4.3	6.6	8.9	
	DS[3:0]=0101			5.4	8.2	11.1	
	DS[3:0]=0110			6.4	9.8	13.2	
	DS[3:0]=0111			7.5	11.5	15.4	
	DS[3:0]=1000			8.5	13	17.4	
	DS[3:0]=1001			9.6	14.7	19.6	
	DS[3:0]=1010			10.6	16.3	21.8	
	DS[3:0]=1011			11.7	17.9	23.9	
	DS[3:0]=1100			12.7	19.4	25.9	
	DS[3:0]=1101			13.8	21	28	
	DS[3:0]=1110			14.8	22.6	30	
	DS[3:0]=1111			15.8	24.2	32.2	
Input Capacitance	—	—	—	—	—	3.2	pF
I_I	Input Leakage Current	—	V_I=1.8V or 0V	—	—	±10	µA
I_{OZ}	Tri-state Output Leakage Current	—	V_O=1.8V or 0V	—	—	±10	

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4.3.2. ADC Input

4.3.2.1. ADC Electrical Information

(Applies across the full range of values listed in the Table 34, Recommended Operating Conditions unless specified.)

Table 49. ADC Electrical Specification

Symbol	Parameter	Min	Typ	Max	Units
F_{CLK}	Clock Frequency	—	—	100	MHz
t_{CLK}	Clock Period	10	—	—	ns
T_OUT	Conversion Time	20	—	—	t_{CLK}
V_{ADCIN_FS}	ADC_IN (analog input) full-scale voltage	—	—	1.8	V
—	Resolution	—	11	—	bits
ENOB	Effective Number of Bit	—	TBD	—	bits
INL	Integral Nonlinearity (INL)	-3	—	+3	LSB
DNL	Differential Nonlinearity (DNL)	-1.5	—	+1.5	LSB
C_{IN}	Input Capacitance	—	16	—	pF
f_s	Sampling Rate	—	—	5	MS/s

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4.3.3. SD, SDIO Timing

4.3.3.1. SD, SDIO Default Mode Timing Parameters

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 50. SD, SDIO Default Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	25	25	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	10	—	—	ns
t_{WH}	Clock High time	—	10	—	—	
t_{TLH}	Clock Rise time	—	—	—	10	
t_{THL}	Clock Fall time	—	—	—	10	
Inputs CMD, DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	5	—	—	ns
t_{IH}	Input Hold time	—	5	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output delay time	Data Transfer Mode	0	—	14	ns
t_{ODLY}	Output delay time	Identification Mode	0	—	50	

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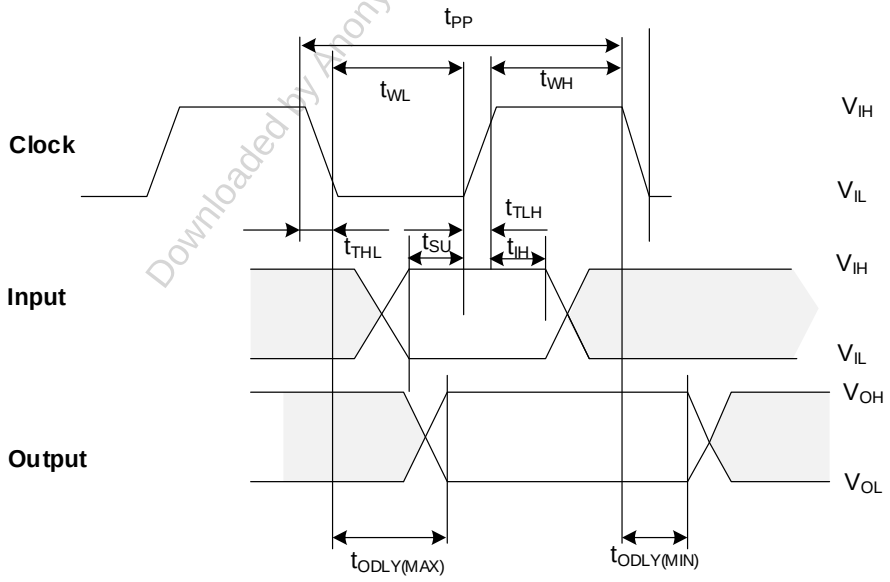

Figure 9. Timing Diagram Data Input/Output Referenced to Clock (Default)

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4.3.3.2. SDIO High-Speed Mode Timing Parameters

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 51. SD, SDIO High-Speed Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	50	50	MHz
t_{WL}	Clock Low time	—	7	—	—	ns
t_{WH}	Clock High time	—	7	—	—	
t_{TLH}	Clock Rise time	—	—	—	3	
t_{THL}	Clock Fall time	—	—	—	3	
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	6	—	—	ns
t_{IH}	Input Hold time	—	2	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Delay time	Data Transfer mode	0	—	14	ns
t_{OH}	Output Hold time	—	2.5	—	—	

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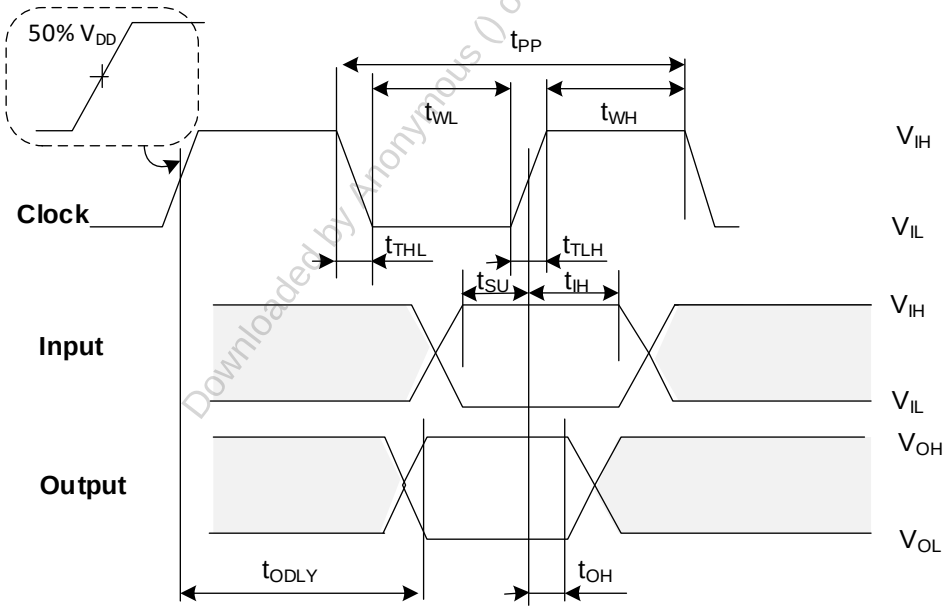

Figure 10. Timing Diagram Data Input/Output Referenced to Clock (High-speed)

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4.3.3.3. SDIO SDR104 Mode Timing parameters

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 52. SD, SDIO SDR104 Mode Timing Parameters

Symbol	Parameter		Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	—	0	208	208	MHz
t_{WL}	Clock Low time	—	—	1.44	—	—	ns
t_{WH}	Clock High time	—	—	1.44	—	—	
t_{TLH}	Clock Rise time	—	—	—	—	0.96	
t_{THL}	Clock Fall time	—	—	—	—	0.96	
Inputs DAT (referenced to Clock):							
t_{ISU}	Input Setup time	—	—	—	—	—	ns
t_{IH}	Input Hold time	—	—	—	—	—	

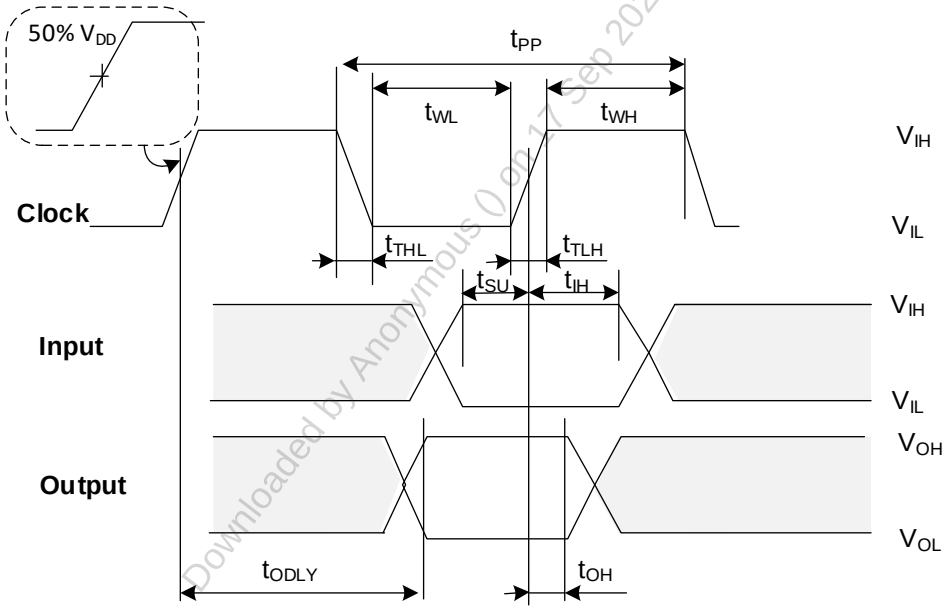

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Figure 11. Timing diagram data I/O referenced to clock (high-speed & SDR104 mode)

4.3.4. Two-Wire Serial Interface (TWSI) Timing

4.3.4.1. TWSI Standard and Fast Mode Timing

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 53. TWSI Standard and Fast Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{TWSI_SCL}	SCL Clock Frequency	100 kHz	—	—	100	kHz
		400 kHz	—	—	400	
T_{TWSI_NS}	Noise Suppression Time at SCL, SDA Inputs	100 kHz	—	—	80	ns
		400 kHz	—	—	80	
T_{TWSI_R}	SCL, SDA Rise time	100 kHz	—	—	1000	
		400 kHz	—	—	300	
T_{TWSI_F}	SCL, SDA Fall Time	100 kHz	—	—	300	
		400 kHz	—	—	300	
T_{TWSI_HIGH}	Clock High Period	100 kHz	4000	—	—	
		400 kHz	600	—	—	
T_{TWSI_LOW}	Clock Low Period	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
$T_{TWSI_SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700	—	—	
		400 kHz	600	—	—	
$T_{TWSI_HD:STA}$	Start Condition Hold Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
$T_{TWSI_SU:STO}$	Stop Condition Setup Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
$T_{TWSI_SU:DAT}$	Data in Setup Time	100 kHz	250	—	—	
		400 kHz	100	—	—	
$T_{TWSI_HD:DAT}$	Data in Hold Time	100 kHz	300	—	—	
		400 kHz	300	—	—	
T_{TWSI_BUF}	Bus Free Time	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
T_{TWSI_DLY}	SCL Low to SDA Data Out Valid	100 kHz	40	—	200	
		400 kHz	40	—	200	

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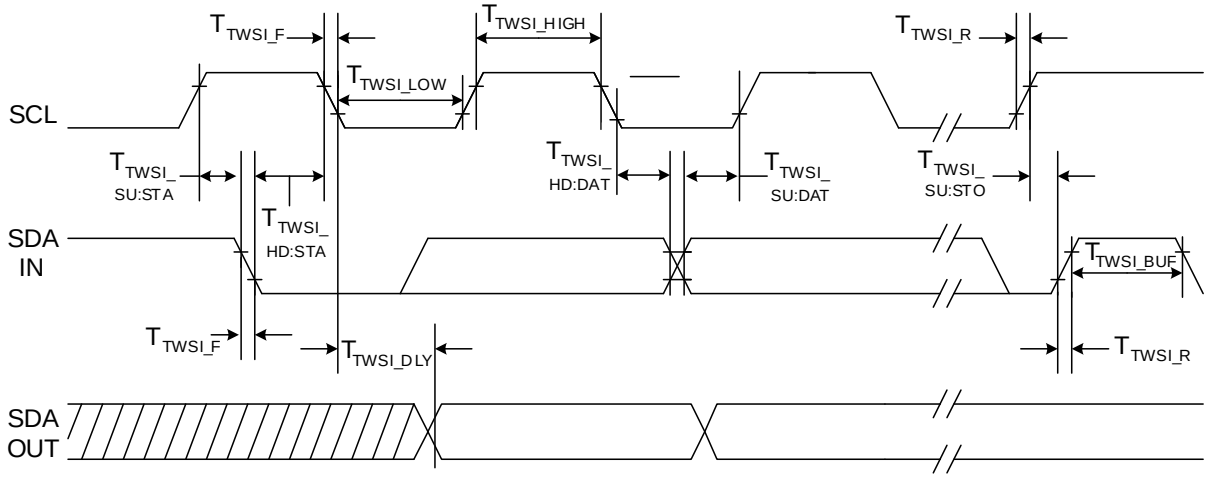

Figure 12. Two-wire serial interface timing

4.3.4.2. TWSI High Speed - transfer rates up to 3.4 Mbits/s

For timing information, refer to the *I²C Bus Specification*.

4.3.5. SPI Timing

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 54. SCLK Cycle Time Configurable Range

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SCLK}	SoC SPI SCLK cycle time	100 MHz SoC SPI controller input clock	20	—	655,340	ns

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Table 55. Motorola SPI Mode 0/2 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	The first SPI cycle in a transfer	—	1.5	—	TSCLK
		Subsequent SPI cycles	—	0.5	—	
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	Other than the last SPI cycle	—	0.5	—	
		The last SPI cycle in a transfer	—	1.0	—	
T_{CH}	SCLK high time	—	—	0.5	—	
T_{CL}	SCLK low time	—	—	0.5	—	
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0.5	—	
		If Tx FIFO is empty	2	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	13.8	—	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	0	—	—	
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	TSCLK
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	0.12	—	1.28	ns

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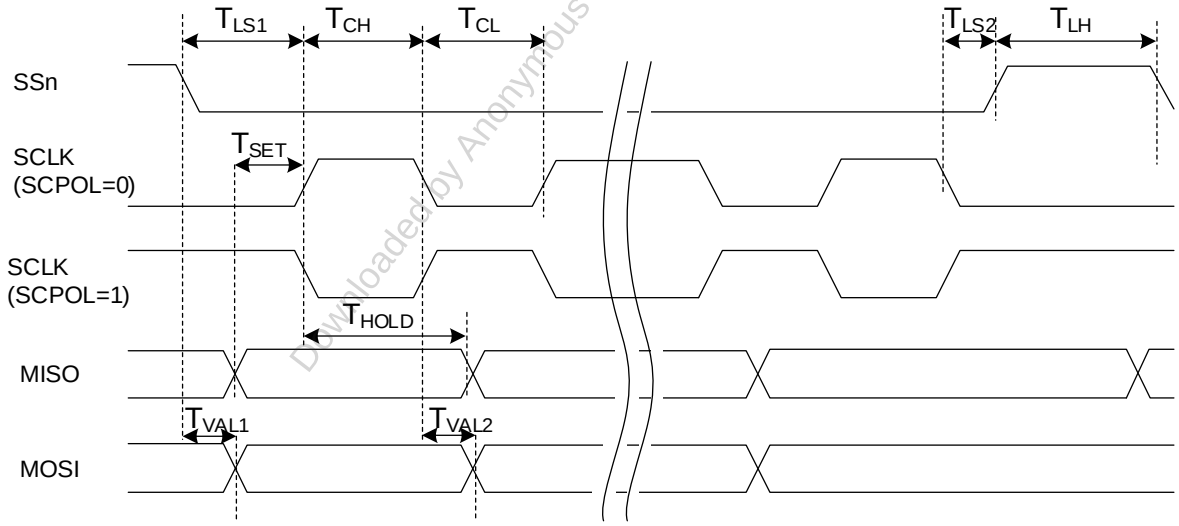

Figure 13. Motorola SPI Mode 0/2 (SCPH = 0)

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(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 56. Motorola SPI Mode 1/3 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	—	—	1.0	—	TSCLK
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	—	—	1.0	—	
T_{CH}	SCLK high time	—	—	0.5	—	
T_{CL}	SCLK low time	—	—	0.5	—	
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0	—	
		If Tx FIFO is empty	1.5	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	—	30	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	—	30	—	
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	TSCLK
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	—	0.5	—	ns

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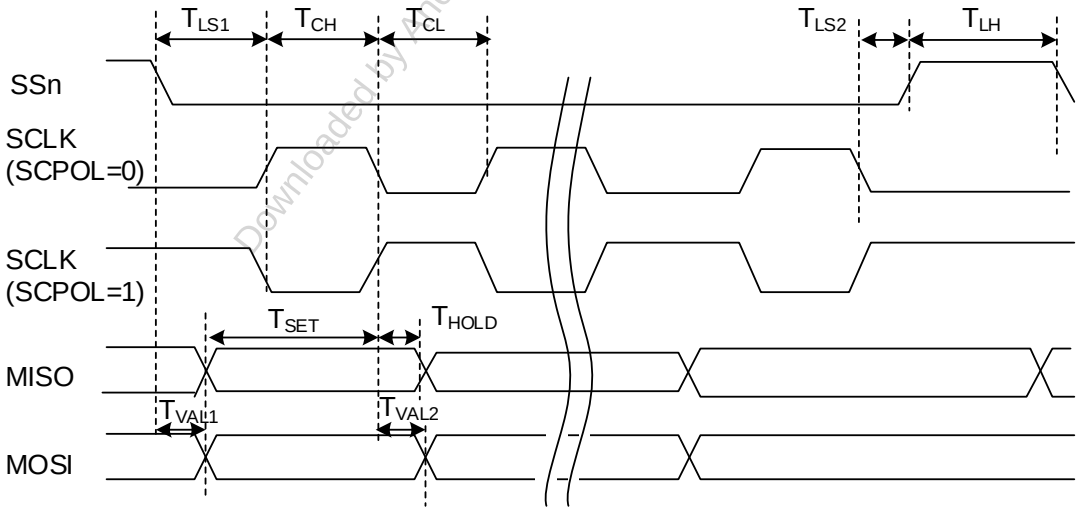

Figure 14. Motorola SPI Mode 1/3 (SCPH = 1)

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4.3.6. UART Timing

Table 57. UART Timing

Symbol	Parameter	Condition	Min	Typ[1]	Max	Units
—	Tx bit width	±5%	—	8.68	—	µs
—	Rx bit width	±5%	—	8.68	—	

1. The typical values are for 115.2 kbaud. Other baud rates may vary.

4.3.7. RGMII Timing

Table 58. RGMII Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{skewT}	Data to Clock output Skew (at transmitter)	-500	0	500	ps
T_{skewR}	Clock to Data input Skew (at receiver)	1.0	—	2.6	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	
$T_{CYCLE_HIGH1000}$	High Time for 1000BASE-T[1]	3.6	4.0	4.4	
T_{RISE}/T_{FALL}	Rise/Fall Time (20–80%)	—	—	0.75	

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{CYCLE} of the lowest speed transitioned between.

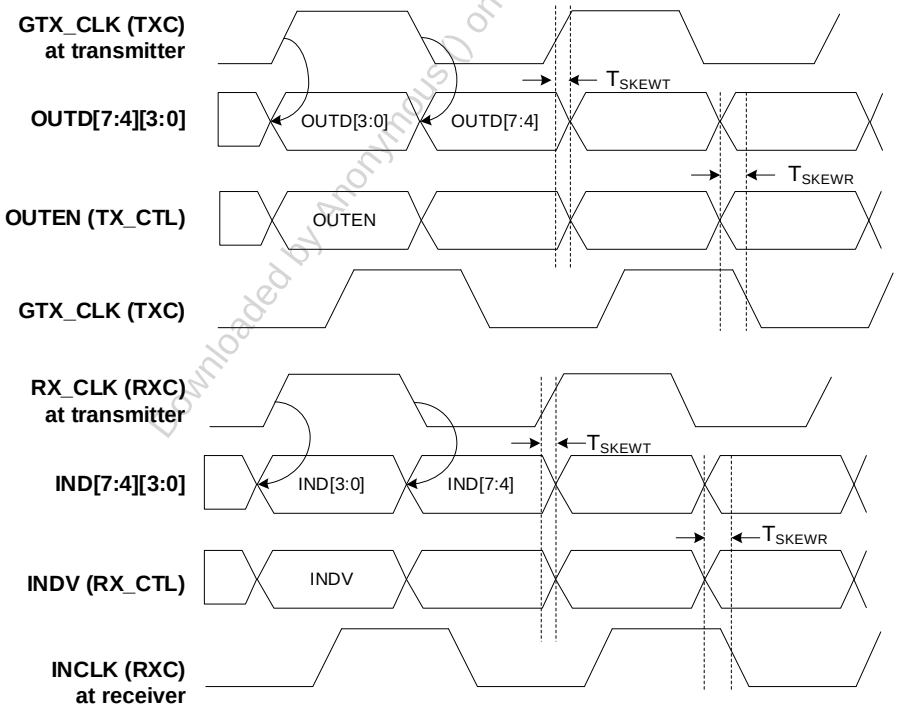

Figure 15. RGMII timing

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4.3.8. RMII Timing

Table 59. RMII Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
D_{REFCLK}	Reference Clock #duty Cycle	35	50	65	%
T_{REFCLK}	Reference Clock Period RMII_REFCLK	—	20	—	ns
T_{SET}	Date Setup Time to RMII_REFCLK rising edge	4	—	—	
T_{HOLD}	Data hold Time after RMII_REFCLK rising edge	2	—	—	
T_{RISE}/T_{FALL}	Rise/Fall Time (20–80%)	—	—	5	

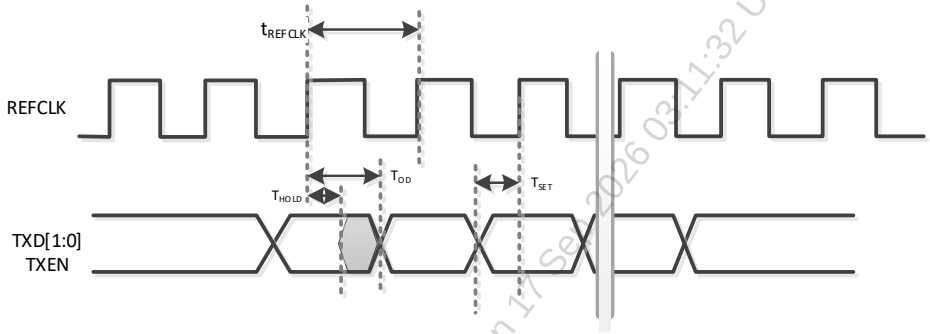

Figure 16. RMII timing

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4.3.9. JTAG Timing

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 60. JTAG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CLK}	Clock cycle	—	—	200	—	ns
$T_{ISTRSTn}$	Set-up time for TRSTn	—	25%	—	—	T_{clk}
$T_{IHTRSTn}$	Hold time for TRSTn	—	0	—	—	ns
T_{ISTDI}	Set-up time for TDI	—	30%	—	—	T_{clk}
T_{IHTDI}	Hold time for TDI	—	0	—	—	ns
T_{OHTDO}	Hold time for TDO	—	0	—	—	ns
T_{OVTDO}	Data valid time for TDO	—	—	—	65%	T_{clk}
T_{RJT}	Rise time for all I/O	20-80%	10	—	—	ns
T_{FJT}	Fall time for all I/Os	80-20%	10	—	—	ns

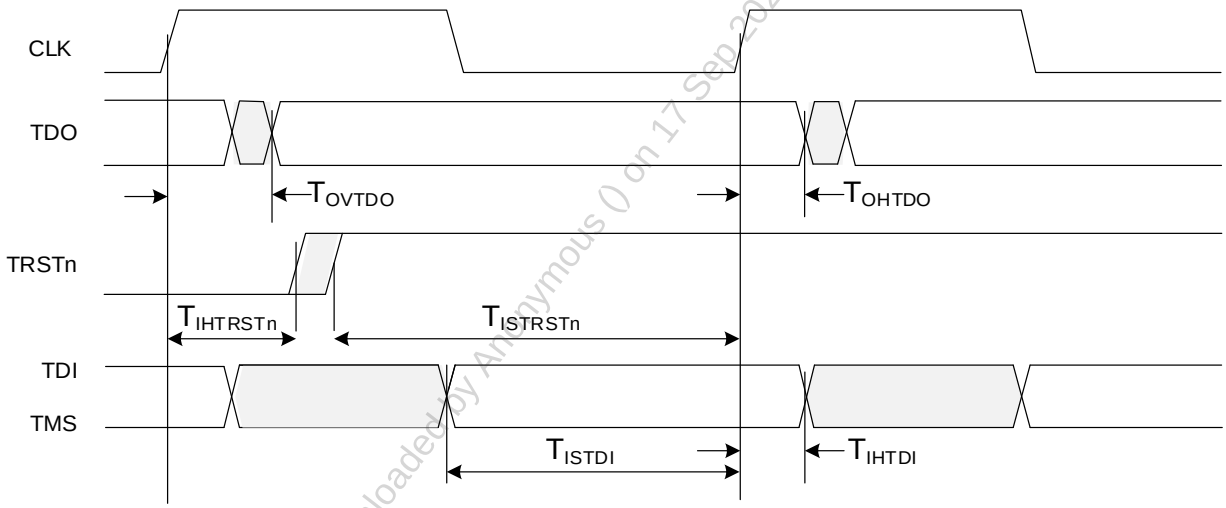

Figure 17. JTAG timing

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4.3.10. I2S Timing

4.3.10.1. I2S Host Mode Timing

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 61. I2S Host Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	16Fs	—	64Fs	Hz
F_{BCLK_PCM}	BCLK Frequency in PCM Mono mode	—	8Fs	—	256Fs	
F_{BCLK_TDM}	BCLK Frequency in TDM mode	—	16Fs	—	256Fs	
F_S	—	—	8	—	192[3]	kHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{SDPD1}	BCLK rising edge to SDATA output valid	—	—	$2^{T}_{AIOSYSCLK}$	—	ns
T_{LRPD}	BCLK rising edge to LRCK valid	—	—	$2^{T}_{AIOSYSCLK}$	—	
T_{SDS}	Set-up time SDATA input with regard to BCLK rising edge	—	—	$-3^{T}_{AIOSYSCLK2}$	—	
T_{SDH}	Hold time SDATA Input with regard to BCLK rising edge	—	—	$4^{T}_{AIOSYSCLK2}$	—	
F_{MCLK}	MCLK (not shown) output frequency	—	6.144	24.576	49.152	MHz
D_{MCLK}	MCLK output duty cycle	—	—	50	—	%

1. BCLK may be inverted for more balanced setup and hold times.
2. Default AIOSYSCLK frequency is 300 MHz.
3. 2-channel 384 kHz.

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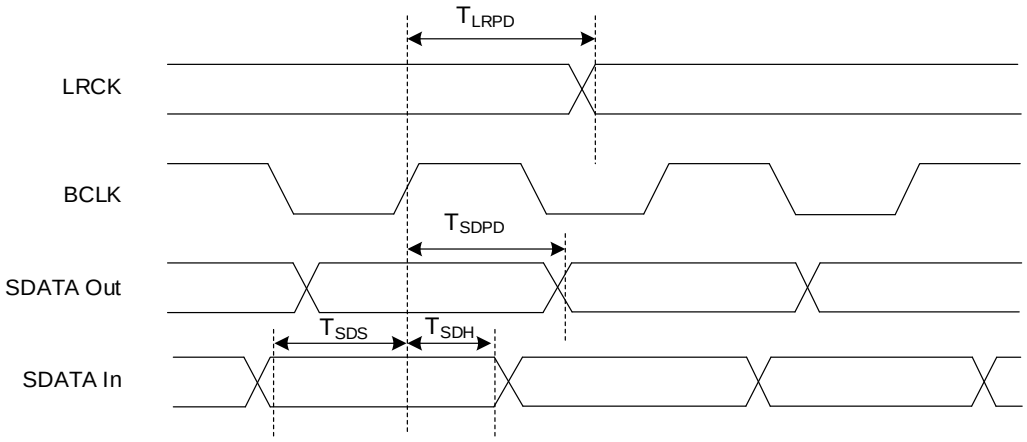

Figure 18. I2S host mode timing

4.3.10.2. I2S Target Mode Timing

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 62. I2S Target Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	16Fs	—	64Fs	Hz
F_{BCLK_PCM}	BCLK Frequency in PCM Mono mode	—	8Fs	—	256Fs	
F_{BCLK_TDM}	BCLK Frequency in TDM mode	—	16Fs	—	256Fs	
F_S	—	—	32	—	192	kHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{LRS}	Setup time LRCK input with regard to BCLK active edge	—	—	$-3T_{AIOSYSCLK1}$	—	ns
T_{LRH}	Hold time LRCK input with regard to BCLK active edge	—	—	$4T_{AIOSYSCLK1}$	—	
T_{SDS}	Setup time SDATA Input with regard to BCLK active edge	—	—	$-3T_{AIOSYSCLK1}$	—	
T_{SDH}	Hold time SDATA Input with regard to BCLK active edge	—	—	$4T_{AIOSYSCLK1}$	—	
F_{MCLK}	MCLK (not shown) input frequency	—	—	24.576	49.152	MHz
D_{MCLK}	MCLK input duty cycle	—	—	50	—	%

1. Default AIOSYSCLK frequency is 300 MHz.

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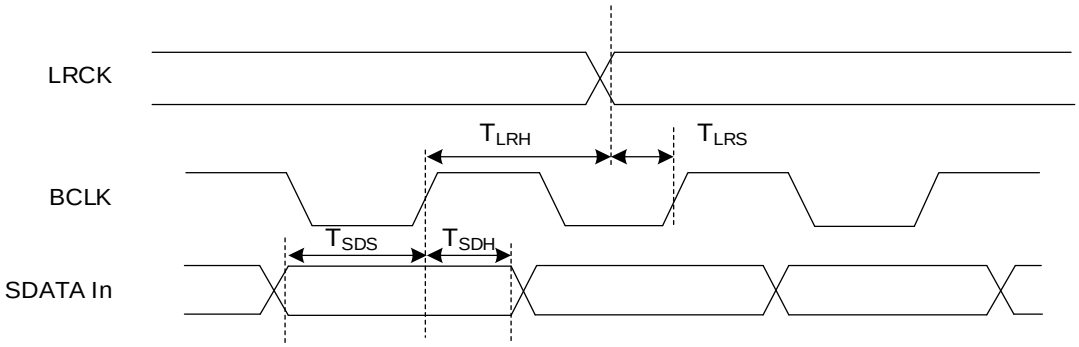

Figure 19. I2S target mode timing

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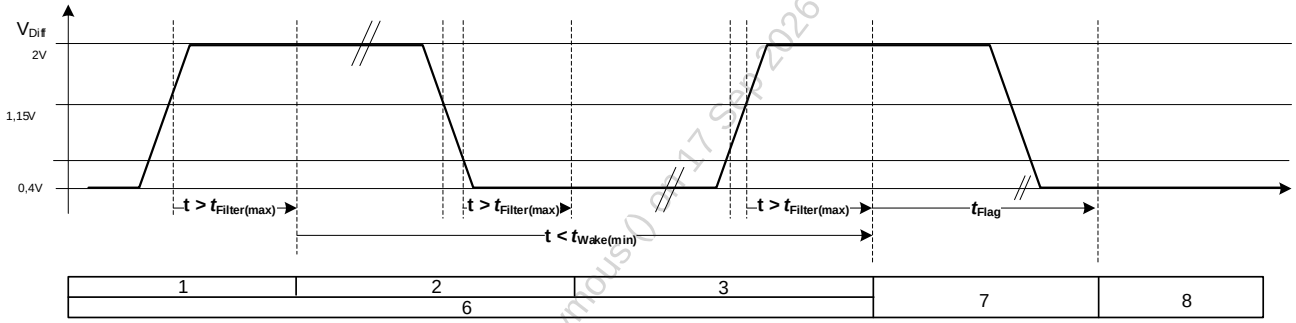
4.3.11. CAN-FD Timing

Table 63. CAN-FD Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
Osc. CAN	Oscillator	Tolerance	—	—	1.58	%
CAN-SPEED	CAN Speed up	—	—	—	8	Mbps
	Full CAN FD	—	—	—	64	Bytes
t_{Filter}	CAN activity filter time, long	—	0.5	—	5	µs
t_{Filter}	CAN activity filter time, short	1.2V <= V_{Diff} <= 3.0V	0.15	—	1.8	
t_{Wake}	Wake-up timeout	-0.5V <= V_{Diff} <= 0.05V	800	—	10,000	
t_{Flag}	Wake-up pattern signaling	-0.5V <= V_{Diff} <= 0.05V	—	—	250	



Keynote: 1 INIT state, 2 in state A, 3 in stage B, 4 in state C, 5 in Wait state, 6 in low-power mode, 7 wake-up detect, 8 wake-up flagged. Refer to ISO 11898-2 for details.

Figure 20. CAN-FD Wake-up control timing

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4.3.12. Timer Counter Smart Pulse-Width Modulator (sPWM) Timing

Table 64. Smart Pulse Width Modulator (sPWM) Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PERIOD}	sPWM	16-bit counter	20 ns	—	16 days	—
		32-bit counter	20ns	—	2824 years	—
—	sPWM Duty Cycle	—	0	—	100	%
—	sPWM Duty Cycle Resolution	—	10ns	—	21sec	—

1. Based on sPWM clock is 100 MHz.

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4.3.13. Temperature Sensor

4.3.13.1. Temperature Sensor Electrical Information

Table 65. Temperature Sensor Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Units
ΔT	Temperature Sensing Range[1]	-40		125	°C
	Resolution	—	0.22°C/LSB	—	—
T_{cycle}	Temperature measurement cycle time	—	310	—	µs
	Temperature Sensor IP variation		±5		°C

1. Actual measurement range is limited by the Ambient operating temperature and Maximum junction temperature specified in Table 47. Recommended Operating Conditions.

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4.3.14. USB 2.0 Timing

4.3.14.1. USB 2.0 DC Characteristics

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 66. USB 2.0 DC Electrical

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	High (driven)	Note[1]	2.0	—	—	V
V_{IHZ}	High (floating)		2.7	—	3.6	
V_{IL}	Low		—	—	0.8	
V_{DI}	Differential Input Sensitivity	|(D+)-(D-)| Note[1]	0.2	—	—	
V_{CM}	Differential Common Mode Range	Includes VDI range Note[1]	0.8	—	2.5	
Input Levels for High-speed						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	—	100	—	150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)	—	525	—	625	
V_{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	—	-50	—	500	
Output Levels for Full-speed						
V_{OL}	Low	Note[1], Note[2]	0.0	—	0.3	V
V_{OH}	High (Driven)	Note[1], Note[3]	2.8	—	3.6	
V_{OSE1}	SE1	—	0.8	—	—	
V_{CRS}	Output Signal Crossover voltage	Note[4]	1.3	—	2.0	
Output Levels for High-speed						
V_{HSOI}	High-speed idle level	—	-10.0	—	10.0	mV
V_{HSOH}	High-speed data signaling high	—	360	—	440	
V_{HSOL}	High-speed data signaling low	—	-10.0	—	10.0	
V_{CHIRPJ}	Chirp J level (differential voltage)	—	700	—	1100	
V_{CHIRPK}	Chirp K level (differential voltage)	—	-900	—	-500	
Input Capacitance for Full-speed						
C_{IND}	Downstream Facing Port	Note[5]	—	—	150	pF
C_{INUB}	Upstream Facing Port (without cable)	Note[6]	—	—	100	

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Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{EDGE}	Transceiver edge rate control capacitance	—	—	—	75	
Terminations						
R_{PU}	Bus pull-up Resistor on Upstream facing port	1.5 kOhm ±5%	1.425	—	1.575	kOhm
R_{PD}	Bus pull-down Resistor on Downstream Facing Port	15 kOhm ±5%	14.25	—	15.75	
Z_{INP}	Input impedance exclusive of pullup/pull-down (for full-speed)	—	300	—	—	
V_{TERM}	Termination voltage for upstream facing port pull-up (R_{PU})	—	3.0	—	3.6	V
Termination in High-speed						
V_{HSTERM}	Termination voltage in high-speed	—	-10	—	10	mV

1. Measured at A or B connector.
2. Measured with RL of 1.425 kohm to 3.6V.3. Measured with RL of 14.25 kohm to GND.
3. Excluding the first transition from the idle state.
4. Measured at A receptacle.6. Measured at B receptacle.

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4.3.14.2. USB 2.0 Source Electrical Characteristics

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 67. USB High-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics						
T_{HSR}	Rise Time (10%–90%)	—	500	—	—	ps
T_{HSF}	Fall Time (10%–90%)	—	500	—	—	
Z_{HSDRV}	Driver Output Resistance (which also serves as high-speed termination)	—	40.5	—	49.5	Ohm
Clock Timings						
T_{HSDRAT}	High-speed Data Rate	—	479.760	—	480.240	Mbps
T_{HSFRAM}	Microframe Interval	—	124.9375	—	125.0625	µs
T_{HSRFI}	Consecutive Microframe Interval Difference	—	—	—	4 highspeed bit times	—

Table 68. USB Full-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics						
T_{FR}	Rise Time	—	4	—	20	ns
T_{FF}	Fall Time	—	4	—	20	
T_{FRFM}	Differential Rise and Fall Time Matching	T_{FR}/T_{FF} Note[1]	90	—	111.11	%
Z_{DRV}	Driver Output Resistance for driver which is not high-speed capable.	—	28	—	44	Ohm
Clock Timings						
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high speed capable.	Average bit rate	11.9940	—	12.0060	Mbps
T_{FDRATE}	Full-speed Data Rate for devices which are high-speed capable.	Average bit rate	11.9700	—	12.0300	
T_{FRAME}	Frame Interval	—	0.9995	—	1.0005	ms
T_{RFI}	Consecutive Frame Interval Jitter	No clock adjustment	—	—	42	ns
Full-speed Data Timings						
T_{DJ1}	Source Jitter Total (including frequency tolerance): To Next Transition	Note[1] Note[2] Note[3]	-3.5	—	3.5	ns
T_{DJ2}	For Paired transitions	Note[4]	-4	—	4	
T_{FDEOP}	Source Jitter for Differential Transition to SEO Transition	Note[3]	-2	—	5	
T_{JR1}	Receiver jitter: To Next Transition	Note[3]	-18.5	—	18.5	
T_{JR2}	For Paired Transitions	—	-9	—	9	
T_{FEOPT}	Source SEO interval of EOP	—	160	—	175	
T_{FEOPR}	Receiver SEO interval of EOP	Note[5]	82	—	—	
T_{FST}	Width of SEO interval during differential transition	—	—	—	14	

1. Excluding the first transition from the idle state.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. For both transitions of differential signaling.
5. Must accept as valid EOP.

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4.3.15. DDR3L / DDR4 / LPDDR4 Timing

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

For DDR3L timing specification, refer to *JEDEC 79-3F* and *JEDEC 79-3-1A.01* standard.

For DDR4 SDRAM specification, refer to *JESD79-4C* standard.

For LPDDR4 SDRAM specification, refer to *JESD209-4A* standard.

4.3.16. eMMC Timing

4.3.16.1. eMMC Timing - Default Bus

(Applies across the full range of values listed in Table 47. Recommended Operating Conditions unless otherwise specified.)

Table 69. eMMC Timing - Default Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode 3	—	0	—	26	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	10	—	—	ns
t_{WH}	Clock High time	—	10	—	—	
t_{TLH}	Clock Rise time	—	—	—	10	
t_{THL}	Clock Fall time	—	—	—	10	
Inputs DAT (referenced to Clock)						
t_{ISU}	Input Setup time	—	3	—	—	ns
t_{IH}	Input Hold time	—	3	—	—	
Outputs CMD, DAT (referenced to Clock)						
t_{ODLY}	Output Delay time	—	3	—	17	ns

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4.3.16.2. eMMC Timing - High-Speed Bus

Table 70. eMMC Timing – High-Speed Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	–	0	–	52	MHz
f_{OD}	Clock Frequency Identification Mode	–	0	–	400	kHz
t_{WL}	Clock Low time	–	6.5	–	–	ns
t_{WH}	Clock High time	–	6.5	–	–	
t_{TLH}	Clock Rise time	–	–	–	–	
t_{THL}	Clock Fall time	–	–	–	–	
Inputs DAT (referenced to Clock)						
t_{ISU}	Input Setup time	–	2.5	–	–	ns
t_{IH}	Input Hold time	–	2.5	–	–	
Outputs CMD, DAT (referenced to Clock)						
t_{ODLY}	Output Delay time	Data Transfer Mode	3	–	–	ns
t_{RISE}	Signal Rise time	–	–	–	–	
t_{FALL}	Signal Fall time	–	–	–	–	

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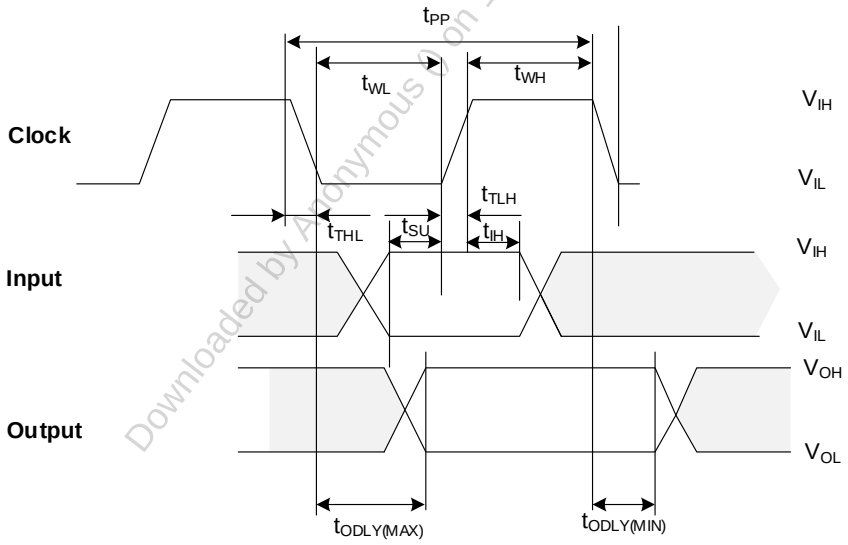

Figure 21. Timing diagram data I/O referenced to clock (default)

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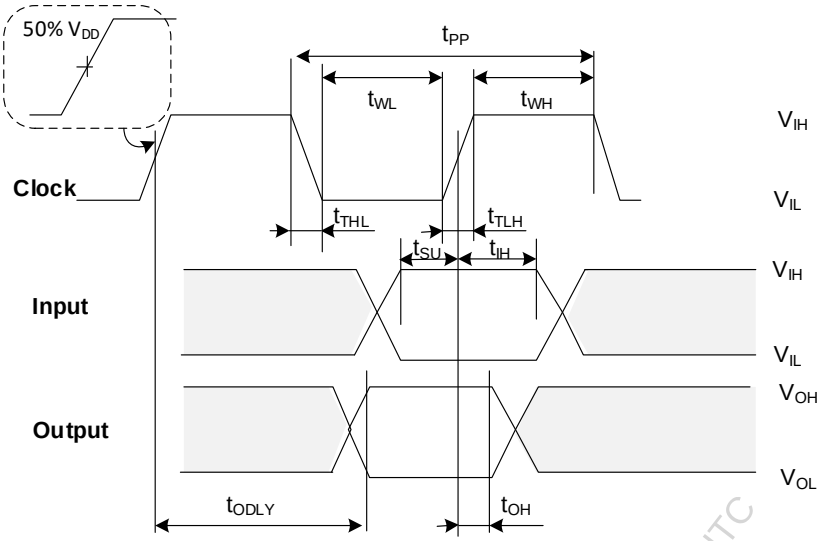

Figure 22. Timing diagram data I/O referenced to clock (high-speed)

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4.3.16.3. eMMC Timing - High-Speed Dual Rate Bus

Table 71. eMMC Timing – High-Speed Dual Rate Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
—	Clock Frequency	—	45	—	55	MHz
Inputs DAT (referenced to Clock)						
t_{ISU}	Input Setup time	—	Note[1]	—	—	ns
t_{IH}	Input Hold time	—	Note[1]	—	—	
Outputs CMD, DAT (referenced to Clock)						
t_{ODLY}	Output Clock Delay	Data Transfer Mode	Note[1]	—	—	ns
t_{RISE}	Signal Rise Time	—	0.4	—	1.32	
t_{FALL}	Signal Fall Time	—	0.4	—	1.32	

1. Refer to *JEDEC Standard No. 84-B51* for eMMC timing specifications.

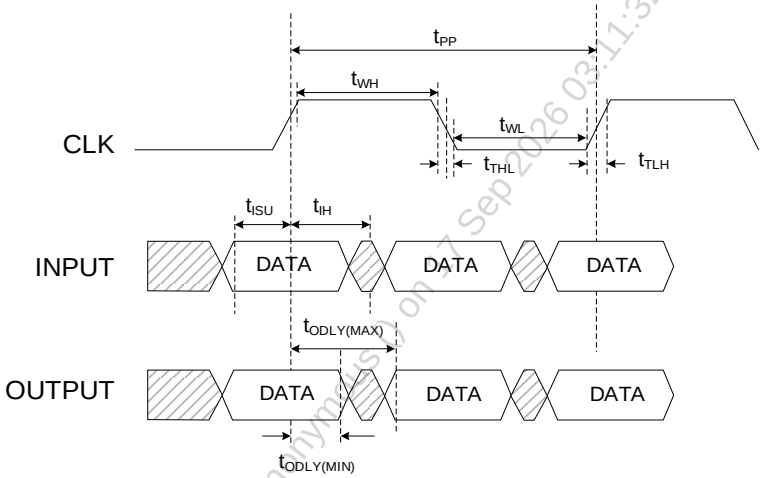

Figure 23. eMMC Timing - High-speed dual-rate interface

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4.3.16.4. eMMC Timing - HS200 Mode & HS400 Mode

Refer to JEDEC Standard No. 84-B51 for eMMC timing specifications.

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4.3.17. MIPI DSI Characteristics

4.3.17.1. Input DC Specifications

Table 72 describes the Input DC Specifications.

Table 72. Input DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
Apply to DATAOP/N Inputs:						
V_I	Input signal voltage range	—	-50	—	1350	mV
I_{LEAK}	Input leakage current	$V_{GNDSH(min)} \le V_I \le V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP receive mode	-10	—	10	µA
V_{GNDSH}	Ground shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Transient pin voltage level	—	-0.15	—	1.45	V
$t_{VOH(absmax)}$	Maximum transient time above $V_{OH(absmax)}$	—	—	—	20	ns

4.3.17.2. MIPI DSI HS Line Drivers DC Specifications

Table 73. MIPI DSI HS Line Drivers DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω ≤ R_L ≤ 125 Ω	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω ≤ R_L ≤ 125 Ω	—	—	14	
V_{CMTX}	Steady-state common-mode output voltage	80 Ω ≤ R_L ≤ 125 Ω	150	200	250	
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	80 Ω ≤ R_L ≤ 125 Ω	—	—	5	
V_{OHHS}	HS output high voltage	80 Ω ≤ R_L ≤ 125 Ω	—	—	360	
Z_{OS}	Single-ended output impedance	—	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch	—	—	—	10	%

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4.3.17.3. MIPI DSI LP Line Drivers DC Specifications

Table 74. MIPI DSI LP Line Drivers DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Output low-level SE voltage	—	-50	—	50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance	—	110	—	—	Ω
$\Delta Z_{OLP(01,10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$\Delta Z_{OLP(00,11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%

4.3.17.4. MIPI DSI LP Line Receiver DC Specifications

Table 75. MIPI DSI LP Line Receiver DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input low voltage, not in ULPS	—	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULPS	—	—	—	300	
V_{IH}	Input high voltage	—	740	—	—	
V_{HYST}	Input hysteresis	—	25	—	—	

4.3.17.5. MIPI DSI Contention Line Receiver DC Specifications

Table 76. MIPI DSI Contention Line Receiver DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ILF}	Input low fault threshold	—	—	—	200	mV
V_{IHF}	Input high fault threshold	—	450	—	—	

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4.3.17.6. MIPI DSI Clock Signal and Data-Clock Timing Specifications

Table 77. MIPI DSI Clock Timing

Symbol	Parameter	Min	Typ	Max	Units	Notes
—	Maximum Serial Data rate (forward direction)	80	—	1500	Mbps	Condition: On DATAP/N outputs. 80 Ω ≤ R_L ≤ 125 Ω
F_{DDRCLK}	DDR CLK frequency	40	—	750	MHz	Condition: On CLKP/N outputs.
T_{DDRCLK}	DDR CLK period	1.33	—	25	ns	Condition: 80 Ω ≤ R_L ≤ 125 Ω
UI_{INST}	UI instantaneous	0.4	—	12.5	ns	The Max value corresponds to a minimum Mbps data rate.
ΔUI	UI variation	-10%	—	10%	UI	—
t_{CDC}	DDR CLK duty cycle	—	50	—	%	Condition: t_{CDC} = t_{CPH} / T_{DDRCLK}
t_{CPH}	DDR CLK high time	—	1	—	UI	—
t_{CPL}	DDR CLK low time	—	1	—	UI	—

4.3.17.7. MIPI DSI HS Line Drivers AC Specifications

Table 78. MIPI DSI HS Line Drivers AC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_r	Differential output signal rise time	—	—	0.30	UI	Condition: 20% to 80%, R_L = 50 Ω For PHY operating at or below 1 Gbps
		—	—	0.35	UI	For PHY operating above 1 Gbps and below or at 1.5 Gbps
		100	—	—	ps	For PHY operating below or at 1.5 Gbps
t_f	Differential output signal fall time	—	—	0.30	UI	Condition: 20% to 80%, R_L = 50 Ω For PHY operating at or below 1 Gbps
		—	—	0.35	UI	For PHY operating above 1 Gbps and below or at 1.5 Gbps
		100	—	—	ps	For PHY operating below or at 1.5 Gbps

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4.3.17.8. MIPI DSI LP Line Driver and Receiver AC Specifications

For MIPI DSI LP line driver and receiver AC specifications, refer to the *MIPI D-PHY Specification v2*.

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4.3.18. MIPI CSI Characteristics

4.3.18.1. Input DC Specifications

Table 79. Input DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
Apply to CLKP/N and DATAP/N Inputs						
V_{PIN}	Pin signal voltage range	-50	—	1350	mV	—
I_{LEAK}	Pin leakage current	-10	—	10	µA	VGNDSH(min) ≤ VPIN ≤ VGNDSH(max) + VOH(absmax) Lane module in LP receive mode
V_{GNDSH}	Ground shift	-50	—	50	mV	—
$V_{PIN(absmax)}$	Transient pin voltage level	-0.15	—	1.45	V	—
$V_{PIN(absmax)}$	Maximum transient time above VOH(absmax)	—	—	20	ns	The voltage overshoot and undershoot beyond the VPIN is only allowed during a single 20ns window after any LP-0 to LP- 1 transition or vice versa. For all other situations the voltage overshoot and undershoot must stay within the VPIN range.

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4.3.18.2. HS Line Receiver DC Specifications

Table 80. HS Line Receiver DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IDTH}	Differential input high voltage threshold	—	—	70	mV	D-PHY spec 1.1 compatibility mode (≤1.5 Gbps)
		—	—	40		In case of High-speed deskew calibration (>1.5 Gbps)
V_{IDTL}	Differential input low voltage threshold	-70	—	—		D-PHY spec 1.1 compatibility mode (≤1.5 Gbps)
		-40	—	—		In case of High-speed deskew calibration (>1.5 Gbps)
V_{IHHS}	Single ended input high voltage	—	—	460		Excluding possible additional RF interference of 100 mV peak sine wave beyond 450 MHz.
V_{ILHS}	Single ended input low voltage	-40	—	—		
V_{CMRXDC}	Input common mode voltage	70	—	330		Excluding possible additional RF interference of 100 mV peak sine wave beyond 450 MHz. This table value includes a ground difference of 50 mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450 MHz.
Z_{ID}	Differential input impedance	80	100	125	Ω	—

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4.3.18.3. LP Line Drivers DC Specifications

Table 81. LP Line Drivers DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{OL}	Output low-level SE voltage	-50	—	50	mV
V_{OH}	Output high-level SE voltage	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance	110	—	—	Ω

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4.3.18.4. LP Line Receiver DC Specifications

Table 82. LP Line Receiver DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input low voltage	—	—	550	mV
V_{IH}	Input high voltage	740	—	—	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULPS	—	—	300	mV
V_{HYST}	Input hysteresis	25	—	—	mV

4.3.18.5. Contention Line Receiver DC Specifications

Table 83. Contention Line Receiver DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{ILF}	Input low fault threshold	—	—	200	mV
V_{IHF}	Input high fault threshold	450	—	—	mV

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4.3.18.6. MIPI CSI Clock Signal and Data-Clock Timing Specifications

Table 84. High Speed Clock Timings

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
—	Maximum Serial Data rate (forward direction)	On DATAP/N outputs. 80 Ω ≤ R_L ≤ 125 Ω	80	—	1.5	Gbps	
F_{DDRCLK}	DDR CLK frequency	On CLKP/N outputs	40	—	750	MHz	
T_{DDRCLK}	DDR CLK period	80 Ω ≤ R_L ≤ 125 Ω	1.333	—	25	ns	
U_{IINST}	UI instantaneous	—	0.667	—	12.5	ns	This value corresponds to a minimum Mbps data rate.
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / T_{DDRCLK}$	—	50	—	%	
t_{CPH}	DDR CLK high time	—	—	1	—	UI	
t_{CPL}	DDR CLK low time	—	—	1	—	UI	
—	DDR CLK / DATA Jitter	—	—	75	—	ps pk-pk	When UI < 1ns, within a single burst.
$T_{SETUP[RX]}$	Data to Clock Setup Time (RX)	—	0.15	—	—	UI	For PHY operating at or below 1 Gbps
$T_{HOLD[RX]}$	Data to Clock Hold Time (RX)	—	0.15	—	—		For PHY operating at or below 1 Gbps

4.3.18.7. MIPI CSI LP Line Drivers AC Specifications

For MIPI CSI LP Line Drivers AC Specifications, refer to the *MIPI D-PHY Specification v2*.

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4.3.18.8. MIPI CSI LP Line Receivers AC Specifications

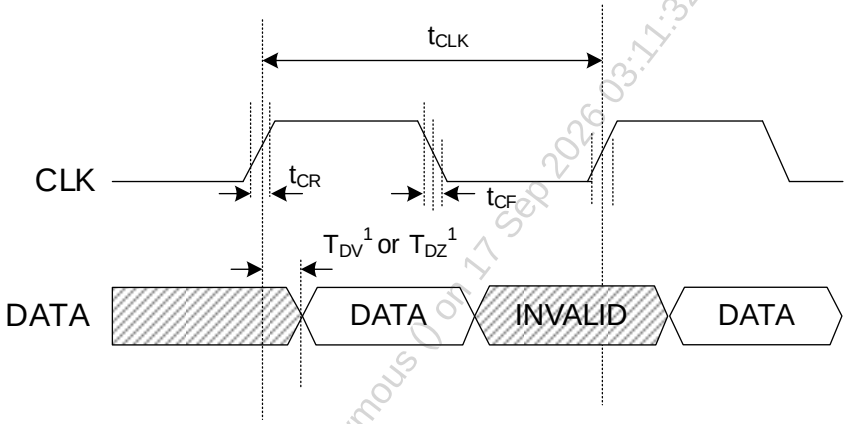
For MIPI CSI LP Line Receivers AC Specifications, refer to the *MIPI D-PHY Specification v2*.

4.3.19. Pulse Density Modulation Timing Characteristics

Table 85. Pulse Density Modulation (Classic PDM) Timing Parameters – SDR Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{CLK}	PDM Clock	—	—	—	FAIOSYSCLK/4[1]	MHz
tD	Clock Duty Cycle	—	—	50	—	%
t_{CR}	Clock Rise Time	10–90%	—	—	TAIOSYSCLK	ns
t_{CF}	Clock Fall Time	90–10%	—	—	TAIOSYSCLK	

1. Default $F_{AIOSYSCLK}$ is 300 MHz.



1. PDM data sampling point is configurable across the t_{CLK} period.

Figure 24. PDM Timing – SDR Mode

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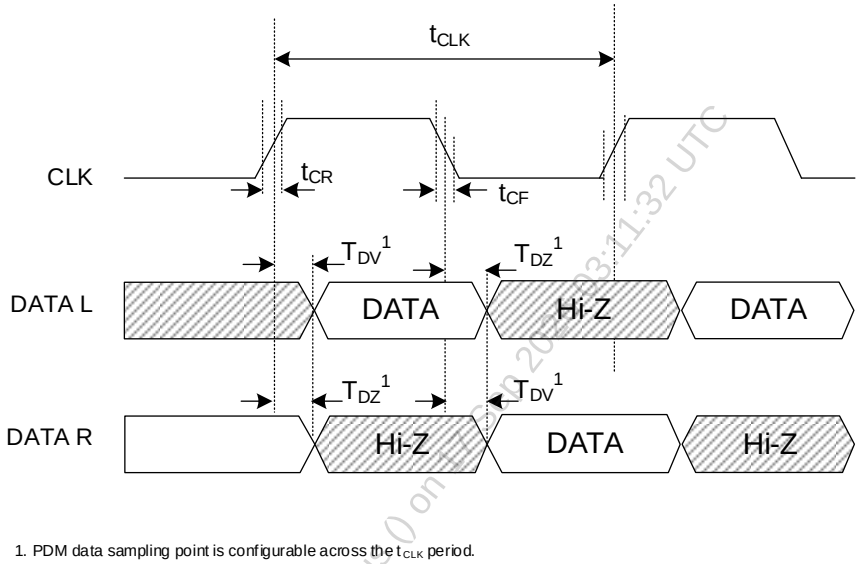
Table 86. Pulse Density Modulation (Half Cycle PDM) Timing Parameters – DDR Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{CLK}	PDM Clock	—	—	—	$F_{AIOSYSCLK}/4$[1]	MHz
tD	Clock Duty Cycle	—	—	50	—	%
t_{CR}	Clock Rise Time	10–90%	—	—	$T_{AIOSYSCLK}$	ns
t_{CF}	Clock Fall Time	90–10%	—	—	$T_{AIOSYSCLK}$	

1. Default $F_{AIOSYSCLK}$ is 300 MHz.



1. PDM data sampling point is configurable across the t_{CLK} period.

Figure 25. PDM timing – DDR Mode

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5. Power Management and System Power

5.1.1. Power-up Sequence

Table 87. SL2610 product line of SoCs Power-up Requirement

Power-up Timing Parameter	Power Rails	Min	Typ	Max	Units
Ramp rate	SM_VCORE, VDD_CORE	—	—	18	mV/uS
	All of DVDD	—	—	18	
	All of AVDD	—	—	18	
	All of VDDIO1P8	—	—	18	
	All of AVDD1P8	—	—	18	
	VDDQLP	—	—	18	
	VDDQ				
	M0_AVDD1P8				
	All AVDD3P3			100	

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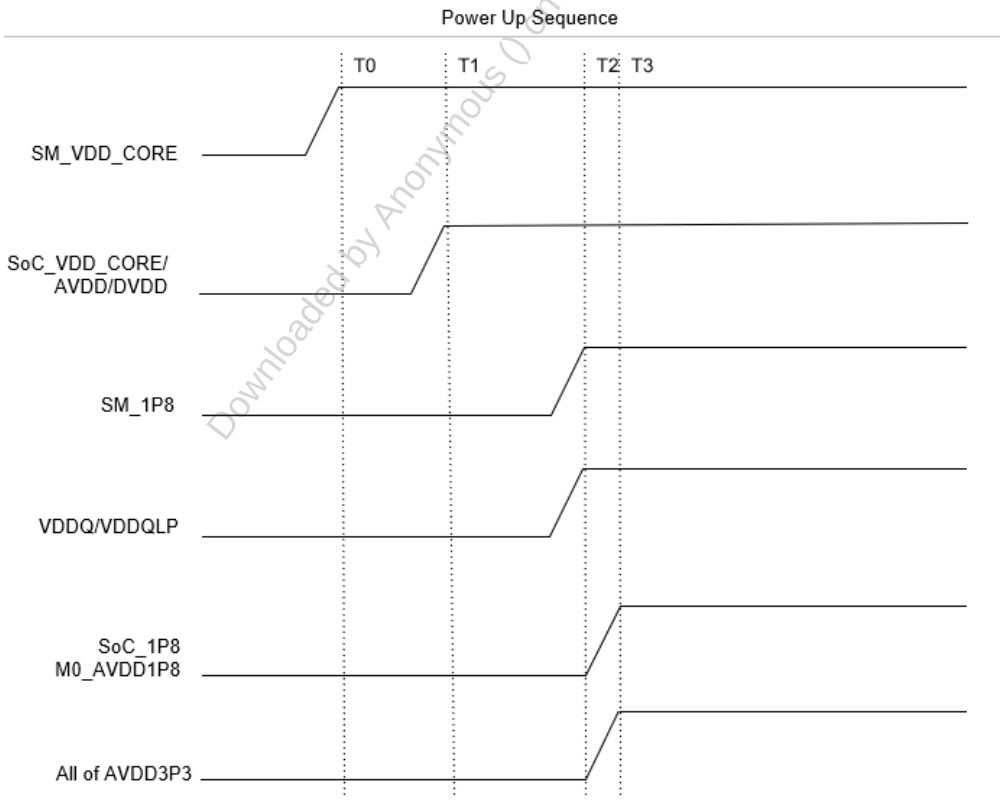

Figure 26. SL2610 product line of SoCs recommended power-up sequence

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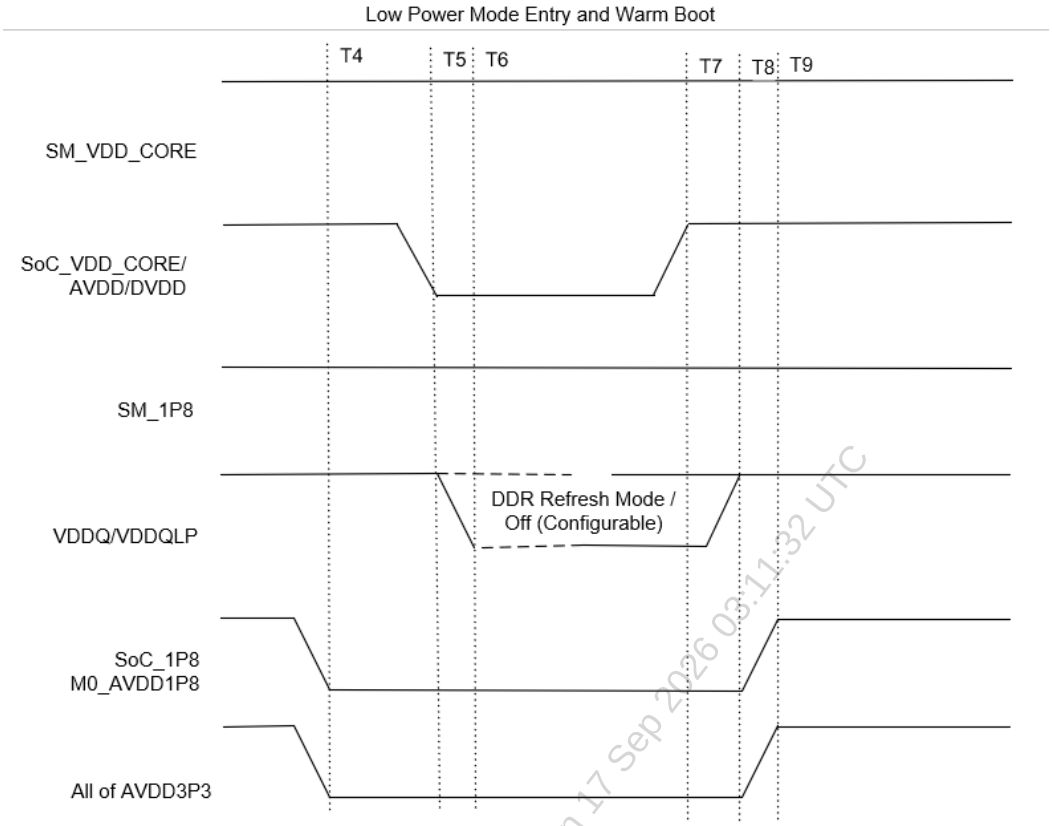

Figure 27. SL2610 product line of SoCs recommended Low Power Mode Entry and Warm Boot

Notes:

1. Each power rail must reach its **full operating voltage (100%)** before the next dependent rail begins ramping up where it is applicable
2. There are **no ordering restrictions** between the **SoC 1.8V** and **SoC 3.3V** supply domains during either power-up or power-down.

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6. Frequency References

6.1.1. Crystal Specifications

Table 88. Crystal Specifications

Parameter	Condition	Typical	Unit
Fundamental Frequency	—	25	MHz
Frequency Tolerance	0 – 70°C (for consumer) -40 – 85°C (for industrial)	<= ± 50	ppm
Load Capacitance	—	8*	pF
Max. ESR	—	60	Ohm
Drive Level	—	35	uW
Mode of Oscillation	—	Fundamental	—

* For more design details, please contact the Synaptics application engineering team.

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7. Subsystems Overview

7.1. External Wireless Connectivity (BT/WLAN)

- SDIO 3.0 for WLAN modules (e.g., Synaptics WIFI Module)
- UART/PCM interfaces for Bluetooth controllers

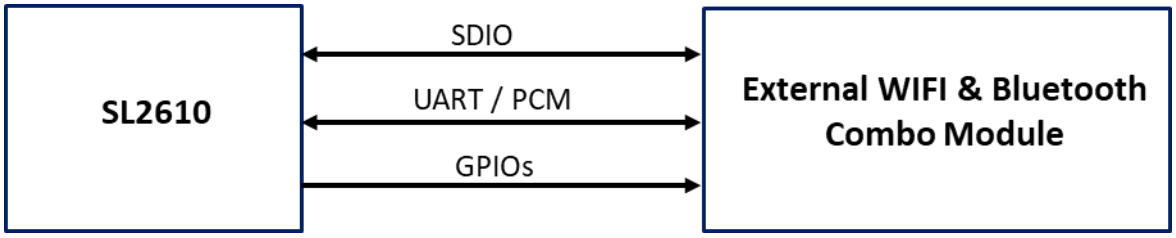

Figure 28. SoC Wi-Fi/Bluetooth Interface

7.2. Display Connection

7.2.1.1. LCD with Display Serial Interface (MIPI)

The SL2610 product line supports interfaces for several types of LCD panels. This section describes the hardware connectivity required for each of the supported interfaces.

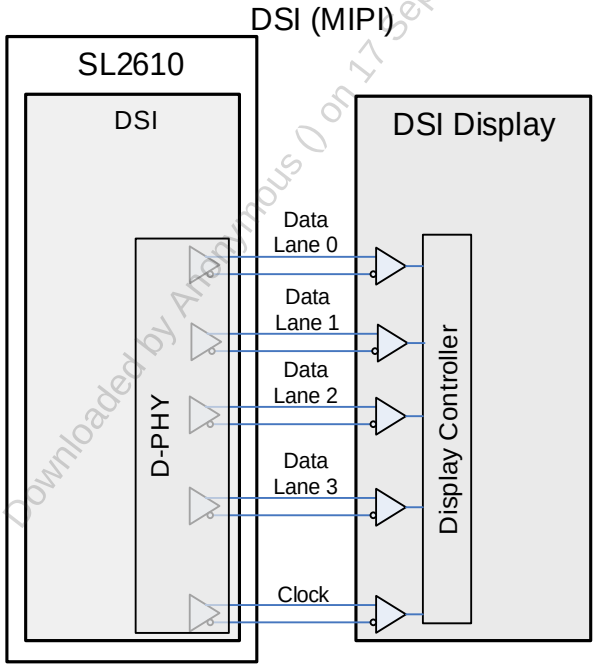

Figure 29. DSI connectivity

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7.3. I3C Host and Target

I3C is a low power, high speed, backwards compatible improvement to the I²C interface. Like I²C, it is a multi-drop bus that uses two wires for the bi-directional transfer of data and commands. However, I3C is designed to provide additional capabilities and improved efficiency compared to I²C. Some key features are:

- Two wire serial interface up to 10 MHz using push-pull
- Legacy I²C device co-existence on the same bus (with some limitations)
- Dynamic addressing while supporting static addressing for legacy I²C devices
- Legacy I²C messaging
- I²C-like single data rate (SDR) messaging
- Multi-host capability
- In-band interrupt support
- Hot-join support
- Support for I3C camera connections for ultra-low power machine vision as per MIPI CSI-2 v4.0 in SM domain

SL2610 product line of SoCs has a single I3C host, the host interface is used to connect I3C and I²C sensors and future AON cameras.

For timing information, refer to the MIPI I3C Specification.

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8. Mechanical and Package Information

8.1. Package Drawing and Dimensions

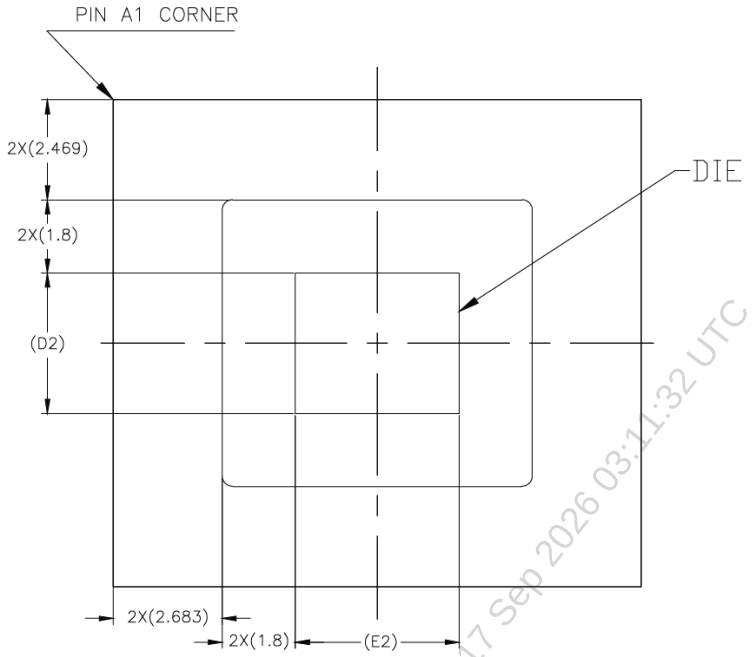

Figure 30. SL2610 product line of SoCs (top view)

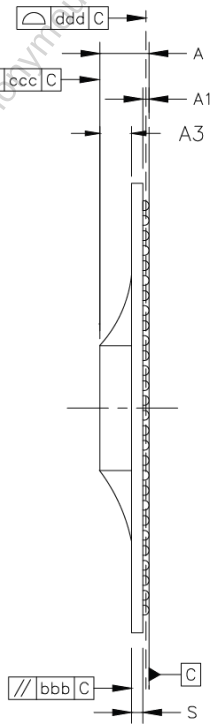

Figure 31. SL2610 product line of SoCs (side view)

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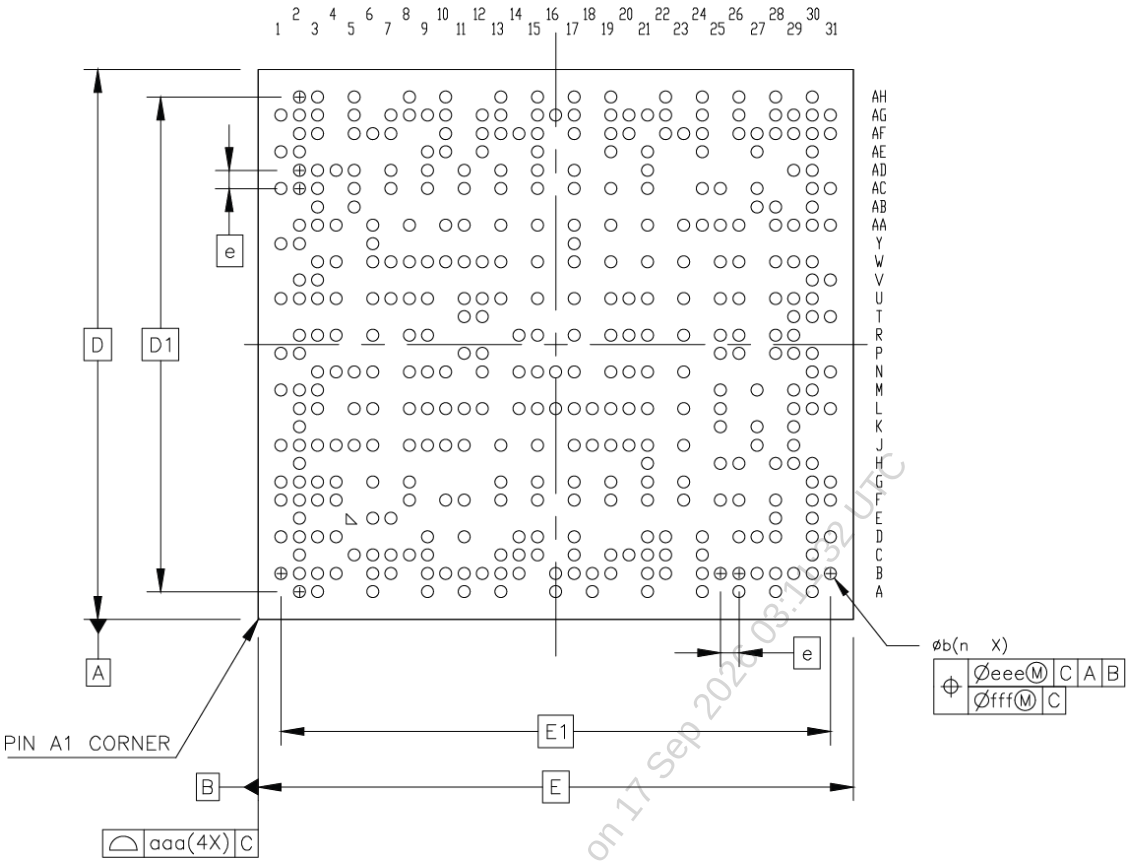

Figure 32. SL2610 product line of SoCs (bottom view)

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Table 89. SL2610 product line of SoCs Dimensions (in mm)

	Symbol	Common Dimensions		
		Min.	Nom.	Max.
Total Thickness	A	1.240	1.310	1.430
Stand Off	A1	0.110	0.160	0.210
Substrate Thickness	S	0.300 (REF)		
Thickness from Substrate Surface to Die Backside	A3	0.850 (REF)		
Body Size	E	13.000 (BSC)		
	D	12.000 (BSC)		
Ball Diameter		0.250		
Ball Width	b	0.200	0.250	0.300
Ball Pitch	e	0.400 (BSC)		
Ball Count	n	393		
Edge Ball Center to Center	E1	12.0 (BSC)		
	D1	10.8 (BSC)		
Expose Die Size	E2	4.035 approx. (BSC)		
	D2	3.462 approx. (BSC)		
Package Edge Tolerance	aaa	0.100		
Substrate Parallelism	bbb	0.200		
Top Parallelism	ccc	0.200		
Coplanarity	ddd	0.080		
Ball Offset (Package)	eee	0.150		
Ball Offset (Ball)	fff	0.050		

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8.2. Package Thermals

For more design details, contact the Synaptics application engineering team.

Table 90. Thermal Conditions[1] for the SL2610 Product Line of SoCs

Symbol	Parameter	Condition	Spec.	Min	Typ	Max	Units
θ_{JA}	Thermal resistance (Note1)–junction to ambient of SL2610 product line of SoCs 393-pin FCBGA package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	16.515	—	°C/W
			Industrial	—	16.141	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/ sec air flow	Consumer	—	16.348	—	
			Industrial	—	16.350	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/ sec air flow	Consumer	—	14.755	—	
			Industrial	—	14.754	—	
ψ_{JT}	Thermal characteristic parameter(Note1)–junction to top center of SL2610 product line of SoCs 393-pin FCBGA package $\psi_{JT} = (T_J - T_{TOP})/P.$ T_{TOP} = Temperature on the top center of the package	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	0.07277	—	
			Industrial	—	0.07281	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/ sec air flow	Consumer	—	0.07416	—	
			Industrial	—	0.07417	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/ sec air flow	Consumer	—	0.07504	—	
			Industrial	—	0.07503	—	

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Symbol	Parameter	Condition	Spec.	Min	Typ	Max	Units
ψ_{JB}	Thermal characteristic parameter (Note 1)–junction to top center of SL2610 product line of SoCs 393-pin FCBGA package $\psi_{JB} = (T_J - T_{BOARD})/P$.	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	2.819	—	°C/W
			Industrial	—	2.817	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/ sec air flow	Consumer	—	6.019	—	
			Industrial	—	6.019	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/ sec air flow	Consumer	—	5.967	—	
			Industrial	—	5.967	—	
θ_{JC}	Thermal resistance (Note 1) –junction to case of the SL2610 product line of SoCs device 393-pin FCBGA package $\theta_{JC} = (T_J - T_C)/ P_{TOP}$ P_{TOP} = Power Dissipation from the top of the package	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	0.327	—	
			Industrial	—	0.327	—	

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Symbol	Parameter	Condition	Spec.	Min	Typ	Max	Units
θ_{JB}	Thermal resistance(Note 1)– junction to board of SL2610 product line of SoCs 393-pin FCBGA package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	2.947	—	
			Industrial	—	2.947	—	

1. For definitions and usage of the thermal parameters in this table, refer to *JESD51-12.01*.

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9. Part Order Numbering / Package Marking

9.1. Part Order Numbering

Table 91 provides a list of the options available for ordering.

Table 91. SL2610 product line of SoCs part order options

Package Type	Part Number [1]	Description
393-pin FCBGA 13x12	**ES Consumer Grade**	
	SL2611AM0A010ECF3T	Engineering sample, Single core 2 GHz A55, M52, 1xGbE, Designed for PSA L2
	SL2615BM1A0B0ECF3T	Engineering sample, Dual core 2 GHz A55, NPU, M52, 3D GPU, CAN, 1xGbE, Designed for PSA L2
	SL2619BM1B3F0ECF3T	Engineering sample, Dual core 2 GHz A55, NPU, M52, 3D GPU, MIPI-CSI, CAN, ECC, 2xGbE, Designed for PSA L3[2]
	MP Consumer Grade	
	SL2611AM0A010MCF3T	Single core 2GHz A55, M52, 1xGbE, Designed for PSA L2
	SL2613AM1A070MCF3T	Single core 2GHz A55, NPU, M52, 3D GPU, MIPI-CSI, 1xGbE, Designed for PSA L2
	SL2615BM1A030MCF3T	Dual core 2GHz A55, NPU, M52, 3D GPU, 1xGbE, Designed for PSA L2
	SL2617BM1A070MCF3T	Dual core 2GHz A55, NPU, M52, 3D GPU, MIPI-CSI, 1xGbE, Designed for PSA L2
	SL2619BM1B3F0MCF3T	Dual core 2GHz A55, NPU, M52, 3D GPU, MIPI-CSI, CAN, ECC, 2xGbE, Designed for PSA L3[2]
	MP Industrial Grade	
	SL2611AM0A090MIF3T	Single core 2GHz A55, M52, CAN, 1xGbE, Designed for PSA L2
	SL2613AM1A0F0MIF3T	Single core 2GHz A55, NPU, M52, 3D GPU, MIPI-CSI, CAN, 1xGbE, Designed for PSA L2
	SL2615BM0A030MIF3T	Dual core 2GHz A55, M52, 3D GPU,1xGbE, Designed for PSA L2
	SL2615BM1A0B0MIF3T	Dual core 2GHz A55, NPU, M52, 3D GPU, CAN,1xGbE, Designed for PSA L2
	SL2615BM0A190MIF3T	Dual core 2GHz A55, M52, CAN,2xGbE, Designed for PSA L2
	SL2617BM1A2F0MIF3T	Dual core 2GHz A55, NPU, M52, 3D GPU, MIPI-CSI, CAN, ECC, 1xGbE, Designed for PSA L2
	SL2619BM1B3F0MIF3T	Dual core 2GHz A55, NPU, M52, 3D GPU, MIPI-CSI, CAN, ECC, 2xGbE, Designed for PSA L3[2]

1. All parts are pin-to-pin compatible with 13x12 FCBGA package with 393 pins.
2. Designed for PSA Level 3 certification.

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Engineering samples:

- Evaluation only—Engineering Samples (ES) are not for commercial products or mass production; buyer use is limited to internal evaluation, testing, and development.
- No warranty—ES are provided “AS IS” with no warranties; the Synaptics is not responsible for failures, inaccuracies, or damages.
- RMAs—Synaptics is not obligated to accept RMAs for ES shipments.

9.2. Package Marking

Figure 33 illustrates a sample package marking and pin 1 location for the SL2610 product line of SoC devices.

Figure 33. Package Marking and Pin 1 Location

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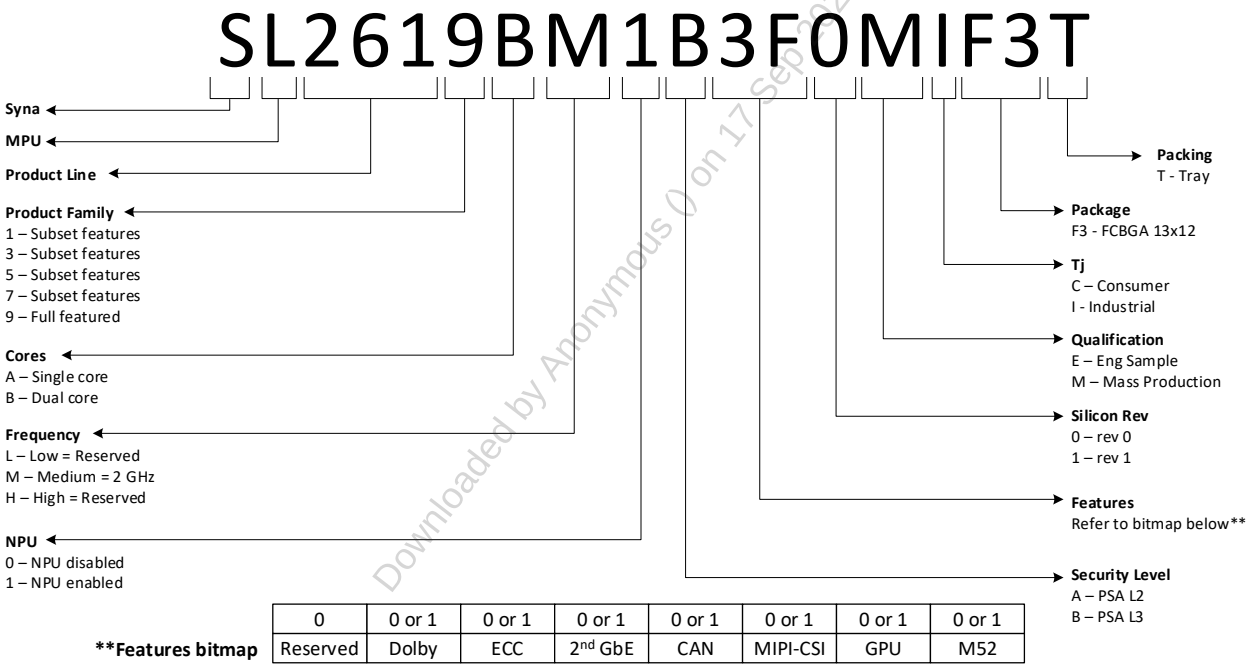
9.3. Synaptics SoC Part Number Ordering Guide



**Features bitmap

0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Reserved	Dolby	ECC	2nd GbE	CAN	MIPI-CSI	GPU	M52

10. Environmental and Regulatory

Environmental qualification and regulatory compliance information is available upon request.

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11. References

The following documents provide reference specifications and standards relevant to the SL2610 product line:

- MIPI D-PHY Specification v2
- JESD79-3E Standard
- JEDEC 79-3F and JEDEC 79-3-1A.01 Standard
- JESD209-4A Standard
- JEDEC Standard No. 84-B51
- MIPI I3C Specification v1.2

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12. Revision History

Revision	Description
A	Initial release. De-featured Tie-offs
B	Updated the following: • 2.1 CPU (clarified per-core power gating and DVFS feature) • 2.8 Audio / Video Input (clarified digital microphones feature) • 2.9 Peripherals (clarified SPI controllers feature) • Table 47. Recommended Operating Conditions • Table 77. MIPI DSI Clock Timing • Corrected Ball Pitch Symbol in Table 89. SL2610 product line of SoCs Dimensions (in mm) • 9.3 Synaptics SoC Part Number Ordering Guide.
C	Updated the following: • Table 1. SL2610 Product Line Feature Summary • 2.1 CPU • 2.2 Security • Table 91. SL2610 product line of SoCs part order options • 9.3 Synaptics SoC Part Number Ordering Guide

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