



Application Note

# Astra™ Machina SL2600 Series Hardware Platform GPIO Pin Multiplexing

Abstract: This document describes the General-Purpose Input/Output (GPIO) pin multiplexing (pinmux) system of the Astra™ Machina SL2600 Series hardware platform. It provides an overview of pin assignments, configuration options, and implementation guidelines to support flexible peripheral integration and optimized system performance.

# Contents

1.	Overview .....	5
1.1.	RDK System Diagram .....	5
1.2.	Pin Multiplexing and Function .....	8
1.3.	40-Pins Header .....	14
1.4.	GPIO Expanders Over I2C .....	14
1.5.	I2C Bus Address Distribution .....	15
2.	References .....	16
3.	Revision History .....	17

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## List of Figures

Figure 1. RDK System Block Diagram.....	7
Figure 2. SL2610 40-Pins Header definition .....	14

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## List of Tables

Table 1. SL2610 GPIO Mapping .....	8
Table 2. GPIO Expanders PIN mapping .....	14
Table 3. I2C Bus Address Distribution.....	15

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# 1. Overview

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The Astra™ Machina SL2600 Series hardware platform includes a versatile General-Purpose Input/Output (GPIO) pin multiplexing (PINMUX) system that enables users to configure pins for a wide range of peripheral functions and optimize overall system performance. This document presents a detailed overview of the SL2610 GPIO pinmux architecture, covering pin assignments, configuration methods, and representative use cases. Designed for both initial setup and advanced configurations, this application note serves as a comprehensive reference for maximizing the flexibility and capabilities of the SL2610 GPIO pinmux system.

## 1.1. RDK System Diagram

The Astra Machina SL2600 Series Reference Development Kit (RDK) is a comprehensive evaluation and prototyping platform designed to accelerate development with the SL2610 system-on-chip (SoC). It provides hardware and software resources that enable developers to explore device features, validate application concepts, and optimize system integration.

Key Features:

- SL2610 SoC Integration – Supports the full GPIO pin multiplexing (PINMUX) system, offering flexible assignment of peripheral interfaces.
- Peripheral Connectivity – Exposes standard interfaces such as CSI, DSI, CAN, UART, SPI, I<sup>2</sup>C, PWM, and GPIO headers for rapid prototyping.
- Expansion Options – Includes connectors for daughter cards or external modules to extend functionality.

The SL2610 RDK is suited for a broad range of use cases, including:

- Peripheral interface evaluation
- System performance benchmarking
- Application prototyping and proof-of-concept development
- Reference design for custom hardware platforms

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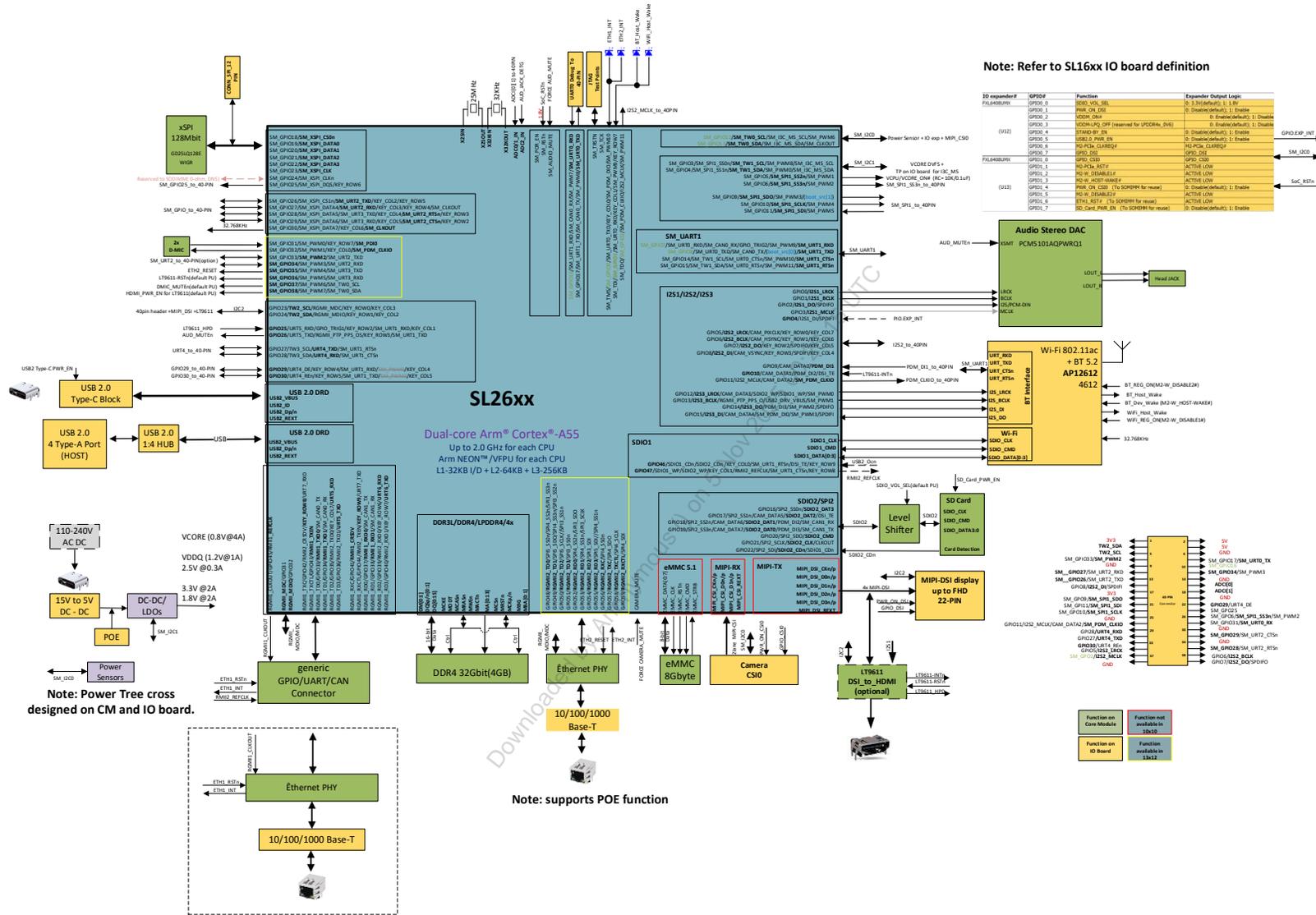


Figure 1. RDK System Block Diagram

## 1.2. Pin Multiplexing and Function

Table 1. SL2610 GPIO Mapping

PAD NAME	OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	STRAP	Pull State	AON	Function Description
SM_AUDIO_MUTE	SM_AUDIO_MUTE	–	–	–	–	–	–	–	–	PD	–	SM_AUDIO_MUTE
SM_POR_EN	SM_POR_EN	–	–	–	–	–	–	–	–	PU	1	SM_POR_EN
SM_RSTn	SM_RSTn	–	–	–	–	–	–	–	–	PU	1	SM_RSTn
SM_TCK	SM_TCK	–	–	–	–	–	–	–	–	PD	1	SM_TCK
SM_TRSTN	SM_TRSTN	–	–	–	–	–	–	–	–	PD	1	SM_TRSTN
SM_GPIO0	SM_TMS	SM_GPIO0	SM_URTO_TXD	KEY_COLO	–	SM_PDM_DIO	SM_PWM10	–	–	PUBoot	1	ETH_1_INT&ETH2_INT
SM_GPIO1	SM_TDI	SM_GPIO1	SM_URTO_RXD	KEY_COL1	GPIO_TRIGO	SM_PWM9	KEY_ROW7	–	–	PUBoot	1	BT_Host_Wake&WiFi_Host_Wake
SM_GPIO2	SM_TDO	SM_GPIO2	SM_PDM_CLKIO	I2S2_MCLK	–	–	SM_PWM11	–	–	PUBoot	1	I2S2_MCLK_to_4OPIN
SM_GPIO3	SM_GPIO3	SM_SPI1_SS0n	SM_TWI_SCL	SM_PWM8	SM_I3C_MS_SCL	–	–	–	–	–	–	I2C For PMIC-Vcore DVFS
SM_GPIO4	SM_GPIO4	SM_SPI1_SS1n	SM_TWI_SDA	SM_PWM0	SM_I3C_MS_SDA	–	–	–	–	–	–	I2C For PMIC-Vcore DVFS
SM_GPIO5	SM_GPIO5	SM_SPI1_SS2n	–	SM_PWM1	–	–	–	–	dft_jtag_sel	PDBoot	–	VCPU/VCORE_ON # (RC= 10K/0.1uF for board level delay)
SM_GPIO6	SM_GPIO6	SM_SPI1_SS3n	SM_SPI1_SS3n	SM_PWM2	–	–	–	–	–	–	–	SM_SPI1_SS3n to 40PIN
SM_GPIO7	SM_GPIO7	SM_URTO_RXD	SM_CANO_RX	KEY_ROW6	GPIO_TRIG2	SM_PWM9	SM_URTI_RXD	–	–	–	1	SM_UART1 to WIFI/BT Module
SM_GPIO8	SM_GPIO8	SM_URTO_TXD	SM_CANO_TX	SM_CLKOUT	–	–	SM_URTI_TXD	–	boot_src[0]	PUBoot	1	SM_UART1 to WIFI/BT Module
SM_GPIO9	SM_GPIO9	SM_SPI1_SDO	SM_SPI1_SDO	SM_PWM3	–	–	–	–	boot_src[1]	PDBoot	–	SM_SPI1_to_40PIN
SM_GPIO10	SM_GPIO10	SM_SPI1_SCLK	SM_SPI1_SCLK	SM_PWM4	–	–	–	–	–	–	–	SM_SPI1_to_40PIN
SM_GPIO11	SM_GPIO11	SM_SPI1_SDI	SM_SPI1_SDI	SM_PWM5	–	–	–	–	–	–	–	SM_SPI1_to_40PIN
SM_GPIO12	SM_GPIO12	SM_TWO_SCL	SM_I3C_MS_SCL	SM_PWM6	–	–	–	MCU_DBG_CLK	–	–	1	Power Sensor + IO exp + MIPI_CSIO

PAD NAME	OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	STRAP	Pull State	AON	Function Description
SM_GPIO13	SM_GPIO13	SM_TWO_SDA	SM_I3C_MS_SDA	SM_CLKOUT	–	–	–	MCU_DBG_OUT0	–	–	1	Power Sensor + IO exp + MIPI_CSIO
SM_GPIO14	SM_GPIO14	SM_TWI_SCL	SM_URTO_CTSn	SM_PWM10	SM_CAN0_RX	–	SM_URTI_CTSn	MCU_DBG_OUT1	–	–	–	SM_UART1 to WIFI/BT Module
SM_GPIO15	SM_GPIO15	SM_TWI_SDA	SM_URTO_RTSn	SM_PWM11	SM_CAN0_TX	–	SM_URTI_RTSn	MCU_DBG_OUT2	–	–	–	SM_UART1 to WIFI/BT Module
SM_GPIO16	SM_GPIO16	SM_URTI_RXD	SM_CAN0_RX	SM_PWM7	–	–	–	–	–	–	1	SM_GPIO16
SM_GPIO17	SM_GPIO17	SM_URTI_TXD	SM_CAN0_TX	SM_PWM8	–	–	SM_URTO_TXD	–	pll_bypass	PDBoot	–	UART0 Debug Port To 40-PIN(Dedicated)
SM_GPIO18	SM_GPIO18	SM_XSPI_CS0n	–	–	–	–	–	–	–	–	–	XSPI 4BIT BOOT for DIAG/UBOOT
SM_GPIO19	SM_GPIO19	SM_XSPI_DATA0	–	–	–	–	–	–	–	–	–	XSPI 4BIT BOOT for DIAG/UBOOT
SM_GPIO20	SM_GPIO20	SM_XSPI_DATA1	–	–	–	–	–	–	–	–	–	XSPI 4BIT BOOT for DIAG/UBOOT
SM_GPIO21	SM_GPIO21	SM_XSPI_DATA2	–	–	–	–	–	–	–	–	–	XSPI 4BIT BOOT for DIAG/UBOOT
SM_GPIO22	SM_GPIO22	SM_XSPI_DATA3	–	–	–	–	–	–	–	–	–	XSPI 4BIT BOOT for DIAG/UBOOT
SM_GPIO23	SM_GPIO23	SM_XSPI_CLK	–	–	–	–	–	–	–	–	–	XSPI 4BIT BOOT for DIAG/UBOOT
SM_GPIO24	SM_GPIO24	SM_XSPI_CLKn	–	–	–	–	–	–	–	–	–	Reserved to SODIMM( 0-ohm, DNS)
SM_GPIO25	SM_GPIO25	SM_XSPI_DQS	–	–	–	–	KEY_ROW6	–	–	–	–	SM_GPIO_to_40-PIN
SM_GPIO26	SM_GPIO26	SM_XSPI_CS1n	SM_URTI2_TXD	KEY_COL2	SM_URTI3_RTSn	SM_URTI3_DE	KEY_ROW5	SM_CLKOUT	–	–	–	SM_GPIO_to_40-PIN
SM_GPIO27	SM_GPIO27	SM_XSPI_DATA4	SM_URTI2_RXD	KEY_COL3	SM_URTI3_CTSn	SM_URTI3_REn	KEY_ROW4	–	–	–	–	SM_GPIO_to_40-PIN
SM_GPIO28	SM_GPIO28	SM_XSPI_DATA5	SM_URTI3_TXD	KEY_COL4	SM_URTI2_RTSn	SM_URTI0_RTSn	KEY_ROW3	SM_URTI_RTSn	–	–	–	SM_GPIO_to_40-PIN
SM_GPIO29	SM_GPIO29	SM_XSPI_DATA6	SM_URTI3_RXD	KEY_COL5	SM_URTI2_CTSn	SM_URTI0_CTSn	KEY_ROW2	SM_URTI_CTSn	–	–	–	SM_GPIO_to_40-PIN
SM_GPIO30	SM_GPIO30	SM_XSPI_DATA7	–	KEY_COL6	–	–	–	SM_CLKOUT	–	–	–	32.768KHz CLOCK to WIFI/BT module
SM_GPIO31	SM_GPIO31	SM_PWM0	SM_URTI1_RXD	KEY_ROW7	SM_PDM_DIO	SM_URTI0_RXD	SM_CANI_RX	–	–	–	–	UART0 Debug Port To 40-PIN (Dedicated)

PAD NAME	OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	STRAP	Pull State	AON	Function Description
SM_GPIO32	SM_GPIO32	SM_PWM1	SM_URTI_TXD	KEY_COLO	SM_PDM_CLKIO	SM_URTO_TXD	SM_CANI_TX	–	–	–	–	SM_PDM_CLKIO
SM_GPIO33	SM_GPIO33	SM_PWM2	–	SM_URT2_TXD	SM_URT3_RTSn	KEY_ROW5	SM_URT3_DE	–	–	–	–	SM_PWM2_to_40-PIN
SM_GPIO34	SM_GPIO34	SM_PWM3	–	SM_URT2_RXD	SM_URT3_CTSn	KEY_ROW4	SM_URT3_REn	–	–	–	–	SM_GPIO_to_40-PIN
SM_GPIO35	SM_GPIO35	SM_PWM4	SM_URTI_RTsn	SM_URT3_TXD	SM_URT2_RTsn	KEY_ROW3	SM_URTO_RTsn	–	–	–	–	ETH2 PHY Reset
SM_GPIO36	SM_GPIO36	SM_PWM5	SM_URTI_CTSn	SM_URT3_RXD	SM_URT2_CTSn	KEY_ROW2	SM_URTO_CTSn	–	–	–	–	LT9611-RSTn(default PU)
SM_GPIO37	SM_GPIO37	SM_PWM6	–	SM_TWO_SCL	KEY_ROW6	SM_PDM_CLKIO	–	–	–	–	–	DMIC_MUTEn(default PU)
SM_GPIO38	SM_GPIO38	SM_PWM7	–	SM_TWO_SDA	–	SM_PDM_DIO	–	–	–	–	–	HDMI_PWR_EN for LT9611(default PU)
GPIO0	GPIO0	I2S1_LRCK	–	–	–	–	–	SPI3_SS0n	–	–	–	I2S1_LRCK to Audio DAC
GPIO1	GPIO1	I2S1_BCLK	–	–	–	–	–	SPI3_SCLK	–	–	–	I2S1_BCK to Audio DAC
GPIO2	GPIO2	I2S1_DO	–	–	SPDIFO	–	–	SPI3_SDO	–	–	–	I2S1_DO to Audio DAC
GPIO3	GPIO3	I2S1_MCLK	–	–	–	–	–	SPI3_SSn	–	–	–	I2S1_MCLK to Audio DAC
GPIO4	GPIO4	I2S1_DI	–	–	SPDIFI	–	–	SPI3_SDI	–	–	–	PIO.EXP_INT
GPIO5	GPIO5	I2S2_LRCK	CAM_PIXCLK	KEY_ROW0	SPDIFI	–	KEY_COL7	–	–	–	–	I2S2_to_40PIN
GPIO6	GPIO6	I2S2_BCLK	CAM_HSYNC	KEY_ROW1	SPDIFO	–	KEY_COL6	–	–	–	–	I2S2_to_40PIN
GPIO7	GPIO7	I2S2_DO	–	KEY_ROW2	SPDIFO	SM_PDM_CLKIO	KEY_COL5	–	–	–	–	I2S2_to_40PIN
GPIO8	GPIO8	I2S2_DI	CAM_VSYNC	KEY_ROW3	SPDIFI	–	KEY_COL4	–	–	–	–	I2S2_to_40PIN
GPIO9	GPIO9	–	CAM_DATA0	–	PDM_DI1	–	–	–	–	–	–	PDM_DI1_to_40PIN
GPIO10	GPIO10	–	CAM_DATA1	–	PDM_DI2	DSI_TE	–	–	–	–	–	LT9611-INTn
GPIO11	GPIO11	I2S2_MCLK	CAM_DATA2	–	SM_PDM_CLKIO	–	–	DBG_CLK	–	–	–	SM_PDM_CLKIO_to_40PIN
GPIO12	GPIO12	I2S3_LRCK	CAM_DATA3	SDIO2_WP	SDIO1_WP	–	–	DBG_OUT0	–	–	–	I2S3 to WIFI/BT Module
GPIO13	GPIO13	I2S3_BCLK	PDM_DI1	RGMII_PTP_PPS_O	USB2_DRV_VBUS	–	–	DBG_OUT1	–	–	–	I2S3 to WIFI/BT Module
GPIO14	GPIO14	I2S3_DO	–	–	PDM_DI3	–	SPDIFO	DBG_OUT2	–	–	–	I2S3 to WIFI/BT Module

PAD NAME	OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	STRAP	Pull State	AON	Function Description
GPIO15	GPIO15	I2S3_DI	CAM_DATA4	–	SM_PDM_DIO	–	SPDIFI	DBG_OUT3	–	–	–	I2S3 to WIFI/BT Module
GPIO16	GPIO16	SPI2_SS0n	–	SDIO2_DAT3	–	–	–	–	–	–	–	SDIO2 to SD Card
GPIO17	GPIO17	SPI2_SS1n	CAM_DATA5	SDIO2_DAT2	–	DSI_TE	–	–	–	–	–	SDIO2 to SD Card
GPIO18	GPIO18	SPI2_SS2n	CAM_DATA6	SDIO2_DAT1	PDM_DI2	SM_CAN1_RX	–	–	–	–	–	SDIO2 to SD Card
GPIO19	GPIO19	SPI2_SS3n	CAM_DATA7	SDIO2_DAT0	PDM_DI3	SM_CAN1_TX	–	–	–	–	–	SDIO2 to SD Card
GPIO20	GPIO20	SPI2_SDO	–	SDIO2_CMD	–	–	–	–	–	–	–	SDIO2 to SD Card
GPIO21	GPIO21	SPI2_SCLK	–	SDIO2_CLK	–	CLKOUT	–	–	software_strap[1]	PDBoot	–	SDIO2 to SD Card
GPIO22	GPIO22	SPI2_SDI	–	SDIO2_CDn	SDIO1_CDn	–	–	–	–	–	–	SDIO2 to SD Card
GPIO23	GPIO23	TW2_SCL	RGMII_MDC	KEY_ROW0	–	SPI3_SS2n	KEY_COL3	DBG_OUT4	–	–	–	TW2_SCL to MIP1_DSI +LT9611 + 40pin header
GPIO24	GPIO24	TW2_SDA	RGMII_MDIO	KEY_ROW1	–	SPI3_SS3n	KEY_COL2	DBG_OUT5	–	–	–	TW2_SDA to MIP1_DSI +LT9611 + 40pin header
GPIO25	GPIO25	URT5_RXD	GPIO_TRIG1	KEY_ROW2	SM_URT1_RXD	–	KEY_COL1	DBG_OUT6	–	–	–	LT9611_HPD
GPIO26	GPIO26	URT5_TXD	RGMII_PTP_PPS_O	–	SM_URT1_TXD	USB2_DRV_VBUS	–	DBG_OUT7	cpu_rst_bypass	PDBoot	–	AUD_MUTEn
GPIO27	GPIO27	TW3_SCL	URT4_TXD	–	SM_URT1_RTSn	–	–	–	–	–	–	URT4_TXD_to_40 PIN
GPIO28	GPIO28	TW3_SDA	URT4_RXD	–	SM_URT1_CTSn	–	–	–	–	–	–	URT4_RXD_to_40 PIN
GPIO29	GPIO29	–	URT4_DE	KEY_ROW4	SM_URT1_RXD	–	KEY_COL4	SPI4_SDI	–	–	–	GPIO29_to_40PIN
GPIO30	GPIO30	–	URT4_REn	KEY_ROW5	SM_URT1_TXD	–	KEY_COL5	SPI4_SCLK	–	–	–	GPIO30 to 40PIN
GPIO31	GPIO31	–	RGMII_MDC	–	–	SPI5_SS3n	SPI3_SS2n	SPI4_SS2n	–	–	–	RGMII_MDC (Connector on CM)
GPIO32	GPIO32	–	RGMII_MDIO	–	–	–	SPI3_SS3n	SPI4_SS3n	–	–	–	RGMII_MDIO (Connector on CM)
GPIO33	GPIO33	RGMII_TDO	RMII1_TXD0	–	–	SM_CANO_TX	SPI3_SS1n	SPI4_SS1n	software_strap[2]	PDBoot	–	RGMII1_TDO (Connector on CM)
GPIO34	GPIO34	RGMII1_TD1	RMII1_TXD1	–	–	SM_CANO_RX	–	–	–	–	–	RGMII1_TD1 (Connector on CM)

PAD NAME	OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	STRAP	Pull State	AON	Function Description
GPIO35	GPIO35	RGMI1_TD2	RMII2_TXDO	KEY_COL7	URT5_RXD	–	–	SPI4_SS0n	–	–	–	RGMI1_TD2 (Connector on CM)
GPIO36	GPIO36	RGMI1_TD3	RMII2_TXD1	–	URT5_TXD	–	–	SPI4_SDO	software_strap[3]	PDBoot	–	RGMI1_TD3 (Connector on CM)
GPIO37	GPIO37	RGMI1_RDO	RMII1_RXDO	–	–	SM_CAN1_TX	–	SPI5_SDI	–	–	–	RGMI1_RDO (Connector on CM)
GPIO38	GPIO38	RGMI1_RD1	RMII1_RXD1	–	–	SM_CAN1_RX	–	SPI5_SDO	–	–	–	RGMI1_RD1 (Connector on CM)
GPIO39	GPIO39	RGMI1_RD2	RMII2_RXDO	KEY_ROW6	URT6_RXD	SPI5_SS1n	SPI4_SS3n	–	–	–	–	RGMI1_RD2 (Connector on CM)
GPIO40	GPIO40	RGMI1_RD3	RMII2_RXD1	KEY_ROW7	URT6_TXD	SPI5_SS2n	SPI4_SS2n	–	–	–	–	RGMI1_RD3 (Connector on CM)
GPIO41	GPIO41	RGMI1_RXC	RMII1_CRSDV	–	–	–	–	SPI5_SCLK	–	–	–	RGMI1_RXC (Connector on CM)
GPIO42	GPIO42	RGMI1_TXC	RMII2_CRSDV	KEY_ROW8	URT7_RXD	–	SPI4_SCLK	–	–	–	–	RGMI1_TXC (Connector on CM)
GPIO43	GPIO43	RGMI1_TXCTL	RMII1_TXEN	–	–	–	SPI4_SS0n	–	software_strap[0]	PUBoot	–	RGMI1_TXCTL (Connector on CM)
GPIO44	GPIO44	RGMI1_RXCTL	RMII2_TXEN	KEY_ROW9	URT7_TXD	–	SPI4_SDI	–	–	–	–	RGMI1_RXCTL (Connector on CM)
GPIO45	GPIO45	RGMI1_CLKOUT	RMII1_REFCLK	–	–	–	–	–	–	–	–	RGMI1_CLKOUT (Connector on CM)
GPIO46	GPIO46	SDIO1_CDn	SDIO2_CDn	KEY_COLO	–	SM_URT1_RTSn	KEY_ROW9	DSI_TE	–	–	–	USB2_Ocn
GPIO47	GPIO47	SDIO1_WP	SDIO2_WP	KEY_COL1	RMII2_REFCLK	SM_URT1_CTSn	KEY_ROW8	–	–	–	–	RMII2_REFCLK
GPIO48	GPIO48	RGMI2_TDO	–	–	–	SPI5_SS0n	SPI4_SS2n	SPI3_SS3n	–	–	–	RGMI2_TDO
GPIO49	GPIO49	RGMI2_TD1	–	–	–	SPI5_SDO	SPI4_SS3n	SPI3_SS2n	–	–	–	RGMI2_TD1
GPIO50	GPIO50	RGMI2_TD2	–	–	–	SPI5_SCLK	–	SPI3_SS1n	–	–	–	RGMI2_TD2
GPIO51	GPIO51	RGMI2_TD3	–	–	–	–	–	SPI3_SS0n	–	–	–	RGMI2_TD3
GPIO52	GPIO52	RGMI2_RDO	–	–	–	–	SPI4_SS2n	SPI3_SDO	–	–	–	RGMI2_RDO

PAD NAME	OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	STRAP	Pull State	AON	Function Description
GPIO53	GPIO53	RGMI2_RD1	–	–	–	–	SPI4_SS3n	SPI3_SCLK	–	–	–	RGMI2_RD1
GPIO54	GPIO54	RGMI2_RD2	–	–	–	–	–	SPI3_SDI	–	–	–	RGMI2_RD2
GPIO55	GPIO55	RGMI2_RD3	–	–	–	SPI5_SDI	–	SPI4_SS1n	–	–	–	RGMI2_RD3
GPIO56	GPIO56	RGMI2_RXC	–	–	–	–	–	SPI4_SSO1n	–	–	–	RGMI2_RXC
GPIO57	GPIO57	RGMI2_TXC	–	–	–	–	–	SPI4_SDO	–	–	–	RGMI2_TXC
GPIO58	GPIO58	RGMI2_TXCTL	–	–	–	–	–	SPI4_SCLK	–	–	–	RGMI2_TXCTL
GPIO59	GPIO59	RGMI2_RXCTL	–	–	–	–	–	SPI4_SDI	–	–	–	RGMI2_RXCTL
CAMERA_MUTE	CAMERA_MUTE	–	–	–	–	–	–	–	–	PD	–	CAMERA_MUTE
EMMC_DATA0	EMMC_DATA0	–	–	–	–	–	–	–	–	–	–	EMMC_DATA0
EMMC_DATA1	EMMC_DATA1	–	–	–	–	–	–	–	–	–	–	EMMC_DATA1
EMMC_DATA2	EMMC_DATA2	–	–	–	–	–	–	–	–	–	–	EMMC_DATA2
EMMC_DATA3	EMMC_DATA3	–	–	–	–	–	–	–	–	–	–	EMMC_DATA3
EMMC_DATA4	EMMC_DATA4	–	–	–	–	–	–	–	–	–	–	EMMC_DATA4
EMMC_DATA5	EMMC_DATA5	–	–	–	–	–	–	–	–	–	–	EMMC_DATA5
EMMC_DATA6	EMMC_DATA6	–	–	–	–	–	–	–	–	–	–	EMMC_DATA6
EMMC_DATA7	EMMC_DATA7	–	–	–	–	–	–	–	–	–	–	EMMC_DATA7
EMMC_CLK	EMMC_CLK	–	–	–	–	–	–	–	–	–	–	EMMC_CLK
EMMC_RSTn	EMMC_RSTn	–	–	–	–	–	–	–	–	–	–	EMMC_RSTn
EMMC_CMD	EMMC_CMD	–	–	–	–	–	–	–	–	–	–	EMMC_CMD
EMMC_STRB	EMMC_STRB	–	–	–	–	–	–	–	–	–	–	EMMC_STRB
SDIO1_CLK	SDIO1_CLK	–	–	–	–	–	–	–	–	–	–	SDIO1_CLK
SDIO1_CMD	SDIO1_CMD	–	–	–	–	–	–	–	–	–	–	SDIO1_CMD
SDIO1_DAT3	SDIO1_DAT3	–	–	–	–	–	–	–	–	–	–	SDIO1_DAT3
SDIO1_DAT2	SDIO1_DAT2	–	–	–	–	–	–	–	–	–	–	SDIO1_DAT2
SDIO1_DAT1	SDIO1_DAT1	–	–	–	–	–	–	–	–	–	–	SDIO1_DAT1
SDIO1_DAT0	SDIO1_DAT0	–	–	–	–	–	–	–	–	–	–	SDIO1_DAT0

### 1.3. 40-Pins Header

A 40-pin General-Purpose Input/Output (GPIO) header with a 0.1-inch (2.54 mm) pin pitch is located along the top edge of the I/O board. Each general-purpose 3.3 V signal pin can be configured through software to support a variety of alternate functions.

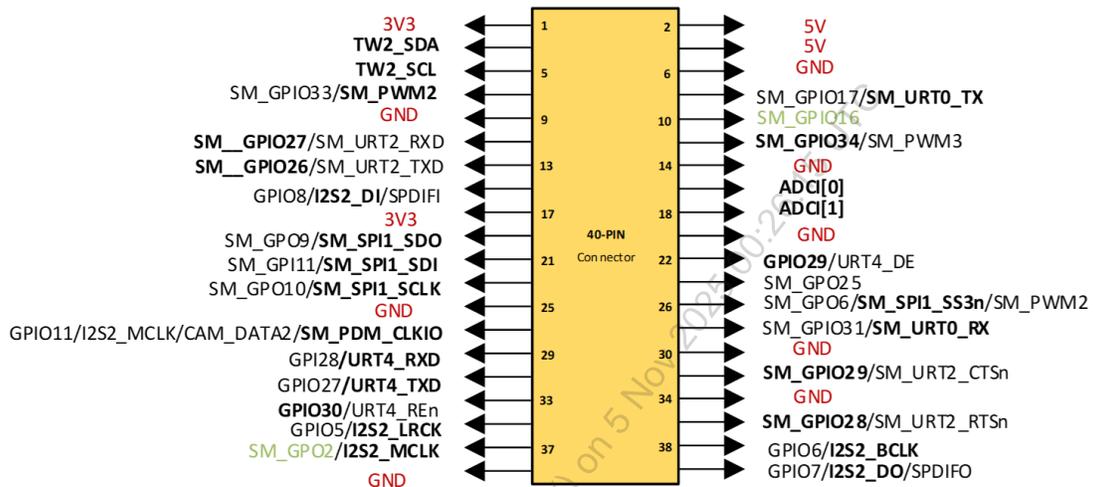


Figure 2. SL2610 40-Pins Header definition

### 1.4. GPIO Expanders Over I2C

Due to the wide range of functions supported by the SL2610 evaluation system, many of the device’s digital pins with GPIO/GPO pin-multiplexing options are allocated to peripheral interfaces and system features. To provide additional control signals, the platform makes extensive use of GPIO expanders supplementing the native GPIO resources of the SL2610.

Table 2. GPIO Expanders PIN mapping

ID expander#	GPIO#	Function	Expander Output Logic
FXL6408UMX (U12)	GPIO0_0	SD00_VOL_SEL	0: 3.3V(default); 1: 1.8V
	GPIO0_1	PWR_ON_DSI	0: Disable(default); 1: Enable
	GPIO0_2	VDDM_ON#	0: Enable(default); 1: Disable
	GPIO0_3	VDDM-LPQ_OFF (reserved for LPDDR4x_DV6)	0: Enable(default); 1: Disable
	GPIO0_4	STAND-BY_EN	0: Disable(default); 1: Enable
	GPIO0_5	USB2_0_PWR_EN	0: Disable(default); 1: Enable
	GPIO0_6	M2-PCIe_CLKREQ#	M2-PCIe_CLKREQ#
	GPIO0_7	GPIO_DSI	GPIO_DSI
FXL6408UMX (U13)	GPIO1_0	GPIO_CS10	GPIO_CS10
	GPIO1_1	M2-PCIe_RST#	ACTIVE LOW
	GPIO1_2	M2-W_DISABLE1#	ACTIVE LOW
	GPIO1_3	M2-W_HOST-WAKE#	ACTIVE LOW
	GPIO1_4	PWR_ON_CS10 (To SOMIMM for reuse)	0: Disable(default); 1: Enable
	GPIO1_5	M2-W_DISABLE2#	ACTIVE LOW
	GPIO1_6	ETH1_RST# (To SOMIMM for reuse)	ACTIVE LOW
	GPIO1_7	SD_Card_PWR_EN (To SOMIMM for reuse)	0: Disable(default); 1: Enable

GPIO.EXP\_INT →  
SM\_I2C0 ↔  
SoC\_RSTn ←

## 1.5. I2C Bus Address Distribution

This section describes the Astra Machina™ platform's use of the I<sup>2</sup>C bus, which is functionally equivalent to the SL2610 Four-Wire Serial Interface (TWSI) bus.

Table 3. I2C Bus Address Distribution

I <sup>2</sup> C/TWSI Bus	Device	Part Number	Target Address (7-bit)	Location
SM_TWO	Connects to MIPI_CSIO	Not applicable	0xXX	SL2610 I/O board
	Connects to Power Sensors	SGM832A/INA3221	0x40/41/42 0x45	SL2610 CM and IO board
	IC GPIO Expander	FXL6408UMX	0x43/0x44	SL2610 IO board
SM_TW1	PMIC for VCORE	SY8827NPKC	0x60	SL2610 CM
TW2	MIPI_DSI Module	Not applicable	0x45	SL2610 IO board
	External device connects to 40PIN connector	Not applicable	0xXX	SL2610 IO board
	DSI_to_HDMI device	LT9611	0x3B	SL2610 CM
TW3	Not Used	Not applicable	n.a	SL2610 IO board

## 2. References

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- *SL2610 Product Line of Embedded Processors Datasheet* (PN: 505-001501-01)
- *Astra Machina SL2600 Series Developer Kit User Guide* (PN: 511-001453-01)

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### 3. Revision History

Revision	Description
A	Initial release.
B	Updated the following: <ul style="list-style-type: none"> <li>• 40PIN definition in Figure 1. RDK System Block Diagram and Figure 2. SL2610 40-Pins Header definition</li> <li>• SM_GPIO16 (OPT7) in Table 1. SL2610 GPIO Mapping.</li> </ul>

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