Application Note

Astra™ Machina SL2600 Series Boundary Scan & JTAG Hardware Interface

Abstract: This application note details the Boundary Scan and JTAG Hardware Interface of SL2600 Series SoC.

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1. Overview

The Astra™ Machina Foundation Series offers evaluation-ready kits that facilitate quick and straightforward prototyping with the Synaptics SL-Series of embedded Linux and Android processors. Featuring a modular design, these kits include interchangeable core compute modules, a standard I/O board and variety of daughter cards for connectivity, debugging, and various I/O configurations.

1.1. Scope

This document offers overview connection interface diagrams for JTAG interface of SL2600 SoC Family.

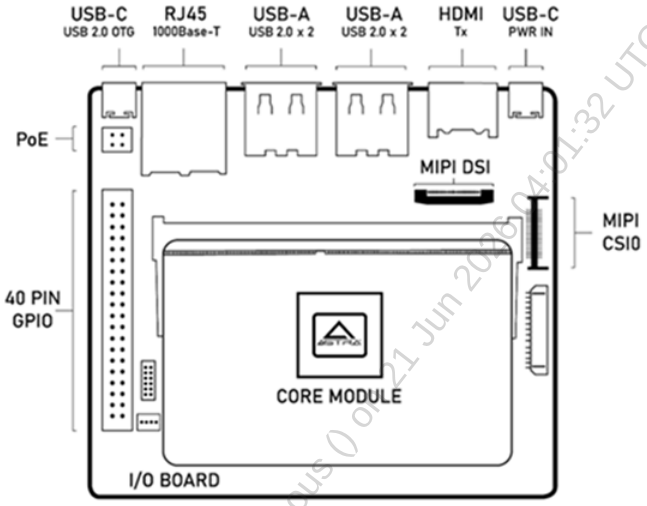


Figure 1. Overview of Astra Machina SL2600 Series

1.2. Astra Foundations JTAG Header Interface Overview

1.2.1. Core Module Hardware Configuration for Enabling Setting JTAG & Boundary Scan Access

Table 1. SL2610 Core Modules Hardware Configuration for enabling JTAG and Boundary Scan

SoC	Pin #	Pull-up Resistor	Condition	Description
SL2610	B24	R31 Stuff	JTAG_SEL = 1	1 = DFT JTAG is selected

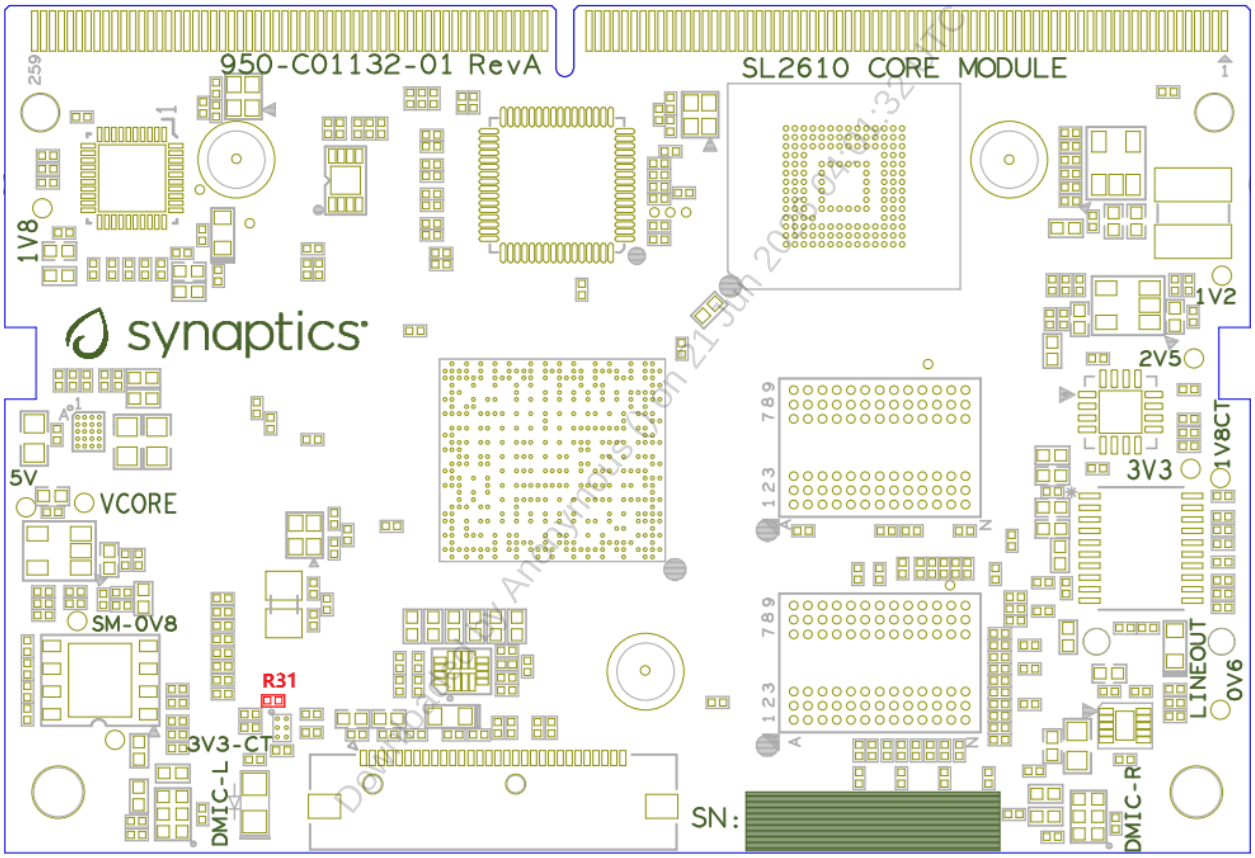


Figure 2. R31 of SL2610 Core Module on Top View

1.2.2. 2x6 Pin Header on I/O Board Interfaces

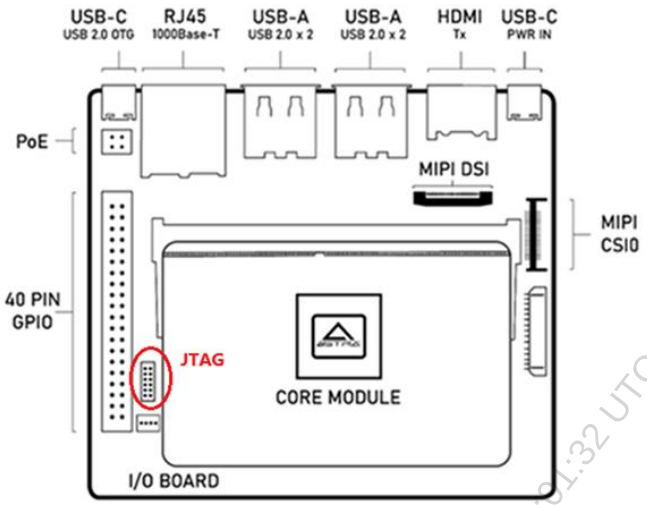
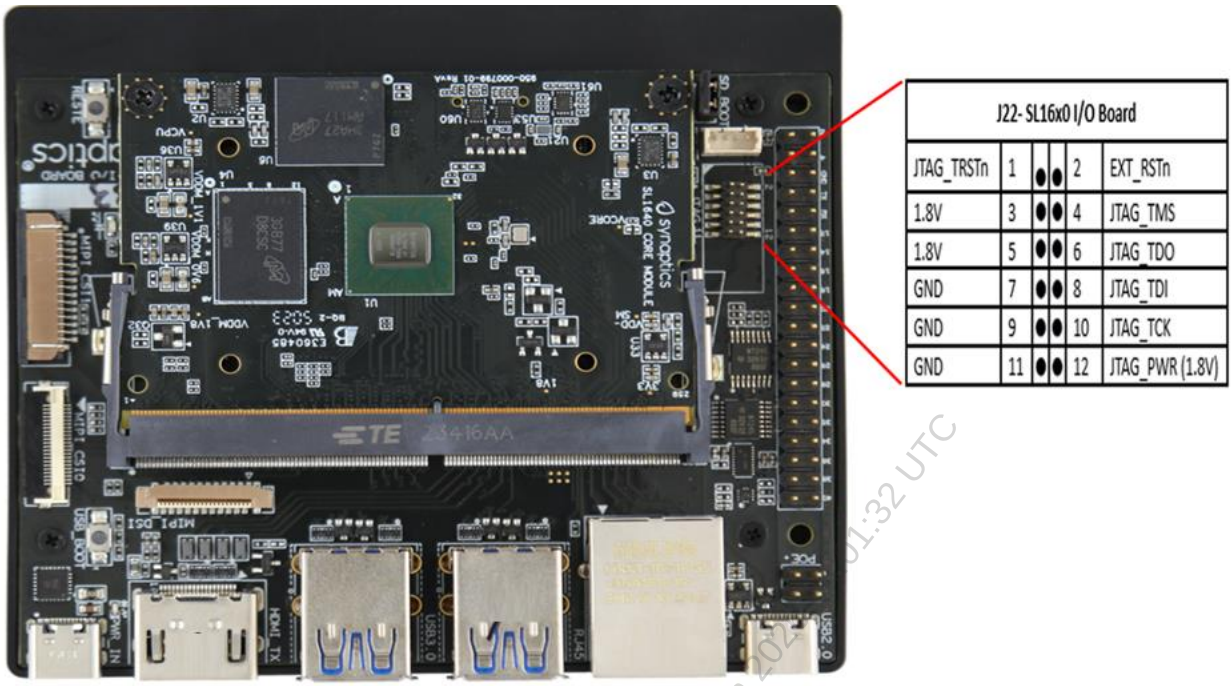


Figure 3. JTAG Header – J22 (1.27mm spacing) Digi-Key P/N: 952-3091-2-ND

Table 2. JTAG signals on SL2610 and I/O board to 2x6 Pin Header

SL2610 Pin #	SL2610 Pin Name	Mode	Direction	Default Function	J22 2x6 Pin Header
W26	SM_TRSTn	-	IN	JTAG_TRSTn	Pin #1
-	-	-	-	EXT_RSTn	Pin #2
-	-	-	-	1.8V	Pin #3
V30	SM_TMS	Mode 0	IN	JTAG_TMS	Pin #4
-	-	-	-	1.8V	Pin #5
U30	SM_TDO	Mode 0	OUT	JTAG_TDO	Pin #6
-	-	-	-	GND	Pin #7
T30	SM_TDI	Mode 0	IN	JTAG_TDI	Pin #8
-	-	-	-	GND	Pin #9
W30	SM_TCK	-	IN	JTAG_TCK	Pin #10
-	-	-	-	GND	Pin #11
-	-	-	-	JTAG_PWR (1.8V)	Pin #12



J22- SL16x0 I/O Board				
JTAG_TRSTn	1		2	EXT_RSTn
1.8V	3		4	JTAG_TMS
1.8V	5		6	JTAG_TDO
GND	7		8	JTAG_TDI
GND	9		10	JTAG_TCK
GND	11		12	JTAG_PWR (1.8V)

Figure 4. Astra Machina I/O Evaluation board 2x6-pin header definition

1.3. Astra SL2600 Series JTAG and Boundary Scan Description Language

1.3.1. Astra SL2600 Series JTAG

The SL2600 device implements a standard IEEE 1149.1-compliant JTAG interface to support debugging of SOC_CPU (ARM) through In-Circuit Emulation (ICE). Additionally, this JTAG interface is also used to control boundary scan (BSCAN) TAP controller, using which Memory Built-In Self -Test (MBIST) and IJTAG paths are controlled.

Figure 5 shows SL2600 JTAG chain connections for both ICE debugger and BSCAN mode. Both the BSCAN DFT controller and the ICE debugger share the same JTAG interface. To support security control features, either CPU ICE debugger interface or boundary scan access is disabled during power up. JTAG access protection level is provided by the OTP.

Note: For production parts, the DFT JTAG is disabled for security purpose.

1.3.1.1. SL2600 JTAG Block Diagram

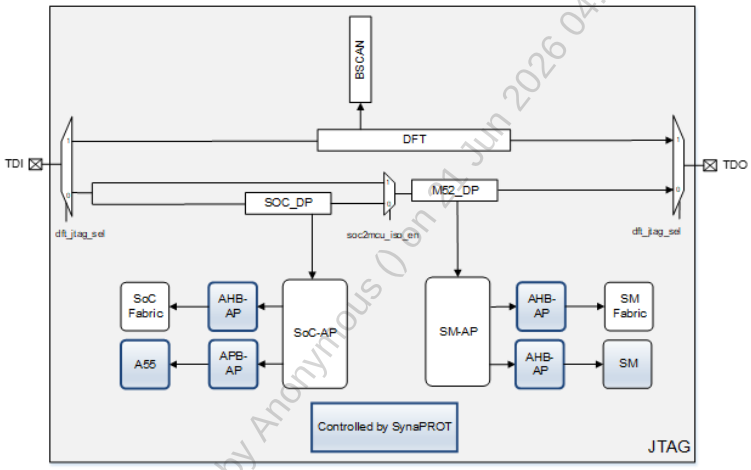


Figure 5. SL2600 JTAG Chain and Boundary Scan Diagram

Table 3. SL2600 Debug Port Configuration

dft_jtag_sel	SynaPROT (OTP)	soc2mcu_iso_en	BSCAN TAP	CPU TAP (CoreSight™)
x	Disable	x	No	No
1	Enable	x	Yes	No
0	Enable	1	No	SoC – No SM- Yes debug features controlled by SynaPROT
0	Enable	0	No	SoC – Yes SM- Yes debug features controlled by SynaPROT

1.3.2. SL2600 Boundary Scan Description Language

The SL2600 device supports the IEEE 1149.1-compliant boundary scan (BSCAN) interface. Table 4 lists the instructions supported.

Table 4. SL2600 Supported Instructions

Instruction	Code
BYPASS	4'b1111
EXTEST	4'b0001
INTEST	4'b0100
SAMPLE/PRELOAD	4'b0101
IDCODE	4'b1100
HIGHZ	4'b0110
CLAMP	4'b0000
Reserved	All others

2. References

- *SL2610 Production Line of Embedded Processors Datasheet* (PN: 505-001501-01)
- *Astra Machina SL2600 Series Single Board Computer (SBC) User Guide (eMMC DDR4)* (PN: 511-001454-01)

3. Revision History

Revision	Description
A	Initial release.

Contact Us

Visit our website at www.synaptics.com to locate the Synaptics office nearest you.

PN: 506-001641-01 Rev A