



Application Note

# Astra™ Machina SL2610 RDK PMIC Solution

Abstract: This application note describes the SL2610 RDK's PMIC solution and system requirement.

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# 1. Overview

The Astra™ Machina SL2610 SoC requires multiple power rails to support its core logic, memory interfaces, and peripheral subsystems. Proper sequencing and regulation of these supplies are essential to ensure reliable operation.

- **Core Supply (SOC\_VDD):**

Nominal operating voltage: 0.8 V

Supports dynamic voltage scaling for performance and power optimization. Over-drive up to 0.9 V or higher is supported for performance enhancement of the Cortex-A55 cores and Neural Processing Unit (NPU).

- **I/O Supplies (VDDQ, VDDQLP):**

Nominal operating voltage is depending on DDR interface standard. Consumption is workload dependent.

- **Peripheral and Analog Supplies:**

Dedicated rails power subsystems such as USB, PHYs, and analog circuits. Voltage levels and current requirements are interface-specific; refer to the SL2610 Datasheet for details.

Table 1. Recommended Operating Conditions

| Symbol       | Parameter                              | Condition  | Min   | Typ  | Max   | Units |
|--------------|----------------------------------------|------------|-------|------|-------|-------|
| AVDDIP8      | All analog supply voltage at 1.8V      | —          | 1.71  | 1.8  | 1.89  | V     |
| MO_AVDDIP8   | Memory 1.8V supply voltage             | —          | 1.71  | 1.8  | 1.89  |       |
| VDDIO1P8     | All IO supply voltage at 1.8V          | —          | 1.71  | 1.8  | 1.89  |       |
| AVDD3P3      | All USB AVDD3P3 at 3.3 supply voltage  | —          | 3.135 | 3.3  | 3.465 |       |
| SMM_VDD_CORE | SM Core supply voltage                 | —          | 0.72  | 0.8  | 0.88  |       |
| AVDD         | All analog supply voltage at           | Consumer   | TBD   | —    | TBD   |       |
|              |                                        | Industrial | TBD   | —    | TBD   |       |
| DVDD         | All USB DVDD 0.8V core supply voltage  | Consumer   | TBD   | —    | TBD   |       |
|              |                                        | Industrial | TBD   | —    | TBD   |       |
| VDD_CORE     | Core supply voltage 0.8V               | Consumer   | TBD   | 0.8  | TBD   |       |
|              |                                        | Industrial | TBD   | 0.8  | TBD   |       |
| VDDQ         | I/O supply voltage for DDR3L at 1.35V  | —          | 1.283 | 1.35 | 1.418 |       |
|              | I/O supply voltage for DDR4 at 1.2V    | —          | 1.14  | 1.2  | 1.26  |       |
|              | I/O supply voltage for LPDDR4 at 1.1V  | —          | 1.06  | 1.1  | 1.17  |       |
| VDDQLP       | I/O supply voltage for LPDDR4x at 0.6V | —          | 0.57  | 0.6  | 0.63  |       |

## 1.1. Worst-Case Consideration

Worst-Case design point assumes fast process corner and 105 °C operation (Commercial Grade), with all functional blocks active simultaneously.

Power rails should be sized to sustain maximum current demand under this condition.

Table 2. Worst Case Power Requirement

| SL2610 RDK Power Group | Voltage(V) | System Current Requirement(A) | SOC Current Requirement(A) |
|------------------------|------------|-------------------------------|----------------------------|
| SM_VDD                 | 0.8        | 0.2                           | 0.1                        |
| SOC_VDD                | 0.8        | 4                             | 4                          |
| SM_1P8                 | 1.8        | 1                             | 0.1                        |
| VPP                    | 2.5        | 0.5                           | 0                          |
| VDD                    | 1.2        | 0.5                           | 0.25                       |
| SOC_3P3                | 3.3        | 2                             | 0.4                        |
| SOC_1P8                | 1.8        | 1                             | 0.4                        |

## 1.2. Power Sequence and Ramp Rate

### 1.2.1. DDR4 Power-Up Sequence Requirements

- $VPP (2.5V) \geq VDD (1.2V) \geq VDDQ (1.2V)$ .
- VPP is required only for DDR4 DRAM, not connected to the SoC directly.
- VDD is the core voltage for DDR4.
- VDDQ is the I/O voltage and must not exceed VDD on power-up.

### 1.2.2. System-Level Power Rail Sequencing:

- SM\_VDD\_CORE > VDD\_CORE > SM\_1P8 > VDD (DDR4 Core)  $\geq$  VDDQ (DDR4 I/O) > SOC\_3P3 > SOC\_1P8

### 1.2.3. LPDDR4 / LPDDR4x Power-Up Sequence Requirements

- $VDD1 (1.8V) \geq VDD2 (1.1V) \geq VDDQ (0.6V)$ .
- VDD1 is the analog power (e.g., PLL).
- VDD2 is the core power.
- VDDQ is the I/O power and must never exceed VDD2.
- These three must ramp in order or simultaneously.

**Note:** VDDQ(0.6V) only needs to follow JEDEC LPDDR4 specification; it has no direct relation to SoC power sequence.

### 1.2.4. System-Level Power Rail Sequencing(LPDDR4x):

- SM\_VDD\_CORE > VDD\_CORE > SM\_1P8 ≥ VDD1(1.8V) ≥ VDD2(1.1V) > SOC\_3P3 > SOC\_1P8

Table 3. SL2610 Power Ramp Rate

| Power-up         | Power Rails        | Min | Typ | Max | Units |
|------------------|--------------------|-----|-----|-----|-------|
| Timing Parameter |                    |     |     |     |       |
| Ramp rate        | SM_VCORE, VDD_CORE | —   | —   | 18  | mV/uS |
|                  | All of DVDD        | —   | —   | 18  |       |
|                  | All of AVDD        | —   | —   | 18  |       |
|                  | All of VDDIO1P8    | —   | —   | 18  |       |
|                  | All of AVDD1P8     | —   | —   | 18  |       |
|                  | VDDQLP             | —   | —   | 18  |       |
|                  | VDDQ               |     |     |     |       |
|                  | MO_AVDD1P8         |     |     |     |       |
|                  | All of AVDD3P3     |     |     | 100 |       |

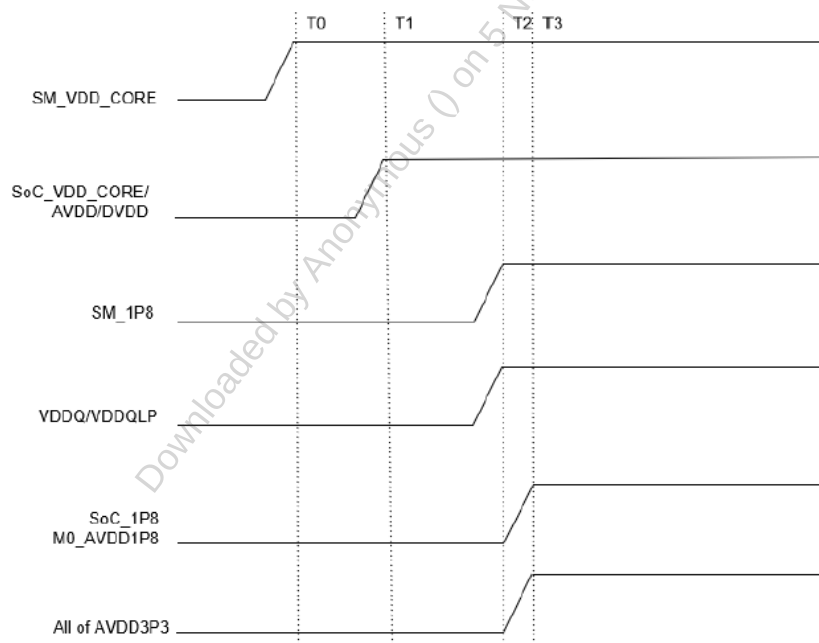


Figure 1. SL2610 Power Sequence

#### Notes:

1. Each power rail must reach its full operating voltage (100%) before the next dependent rail begins ramping up where it is applicable.
2. There are no ordering restrictions between the SoC 1.8V and SoC 3.3V supply domains during either power-up or power-down.

### 1.3. RDK\_DDR4 PMIC Solutions

To support multiple voltage rails for SL2610's CPU, memory, I/O, and system management domains. The power solution uses a combination of DC-DC converters and LDOs, primarily from Silergy, with 2nd source options for cost or sourcing flexibility.

Table 4. Recommended PMICs by Power Rail

| Power Rail  | Vendor           | PMIC                             |
|-------------|------------------|----------------------------------|
| VCORE       | Silergy          | SY8827N (6A, I2C control)        |
| 2nd Source  | MPS              | MP8867(8A) or MP8864(4A)         |
|             | TI               | TPS628660A(6A)/TPS628640AYCG(4A) |
| 3.3V/1.8V   | Silergy          | SY8832AIC(2A)                    |
| 2nd Source  | Fitipower        | FP6397S5(2A)/FP6396S5(1.2A)      |
| 2.5V        | ON Semiconductor | NCP114ASN250T1G(0.3A)            |
| 1.2V        | Silergy          | SY8088IAAC(1A)                   |
| 2nd Source  | Fitipower        | FP6396S5(1.2A)                   |
| 0.6V VTT    | TI               | TPS51206DSQR(2A)                 |
| 0.8V for SM | Silergy          | SY8088IAAC(1A, DC-DC)            |
| 2nd Source  | Fitipower        | FP6396S5(1.2A)                   |

## 2. References

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- *Astra Machina Foundation Series Quick Start Guide* (PN: 511-001404-01)
- *Astra Machina SL1620 Developer Kit User Guide* (PN: 511-001407-01)
- *Astra Machina SL1640 Developer Kit User Guide* (PN: 511-001405-01)
- *Astra Machina SL1680 Developer Kit User Guide* (PN: 511-001403-01)
- *Astra Machina SL2600 Series Developer Kit User Guide* (PN: 511-001453-01)

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### 3. Revision History

| Revision | Description      |
|----------|------------------|
| A        | Initial release. |

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