Application Note

SL2610 General PCB Design and DDR3L/DDR4 & LPDDR4(x) Interface Layout Guidelines

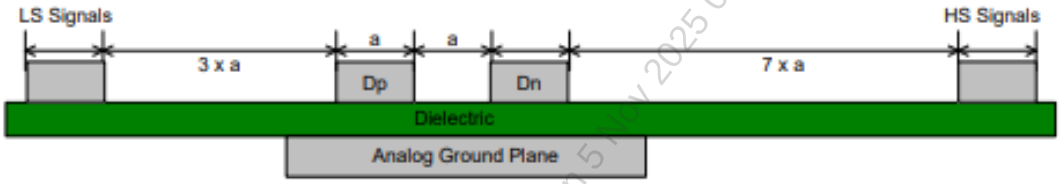
Abstract: This document provides PCB layout guidelines for integrating DDR3L, DDR4, and LPDDR4(x) memory with the SL2610 processor. It outlines key practices in routing, impedance control, and length matching to ensure signal integrity and reliable system performance.

  | PN: 506-001629-01 Rev A

Contents

1. PCB Layout Guidelines

- Trace impedance of 100 Ω differential (+/-10%) is required. For USB2.0, the trace impedance of 90 Ω differential (+/-10%) is required.
- Matching to < 0.5mm (about 0.02 inch) between two different signals. Trace lengths should match by 0.25mm (about 0.01 inch) or less for differential pairs (same pair) of high-speed signals.
- The skew between any data lane and clock lane should be matched within +/-10ps on both package and PCB.
- Do not route trace over plane void or anti-pads. Return path should be VSS and continuous.
- Ensure ground return vias adjacent to the differential pair core vias to minimize crosstalk between lanes.
- Void the planes above the BGA pads to minimize the capacitive discontinuity.
- To minimize crosstalk, take care of signal traces which are routed close to the data differential pairs. The minimum recommended spacing is 3xa for low-speed non-periodic signals and 7xa for high-speed periodic signals. A continuous ground plane below the differential lines is required.



- TX and RX pairs should not be routed side-by-side in the same signal layer.
- Crosstalk should be accumulated total with all aggressors and meet the -30dB requirement until Nyquist frequency.
- Differential trace insertion loss should be greater than -3 dB at the Nyquist frequency for standard high-speed interfaces. For PCIe 3.0, USB 3.0, and Ethernet, up to -6 dB is acceptable with receiver equalization. The loss profile must be monotonic, with no variations exceeding ±2 dB across the Nyquist band. Differential pairs should be short, impedance-controlled, length-matched within the specified intra-pair skew limits, and routed over continuous ground reference planes to minimize loss.
- Single-ended trace insertion loss should be less than -3 dB at the Nyquist frequency to maintain signal integrity. The loss profile should be monotonic with no abrupt variations, and deviations within the Nyquist band should not exceed ±1.5 dB. Traces should be as short as practical, impedance-controlled (typically 50 Ω ±10%), and routed over continuous reference planes to minimize reflection and loss.

2. Power Supply Guidelines

- Supply bypass capacitors are recommended to minimize power supply noise. Noise analysis of the power delivery network is required to determine the actual values. Depending on their size, each capacitor will have a different equivalent series resistance (ESR) and equivalent series inductance (ESL) that will determine the given capacitor's effectiveness over a frequency range. In general, several low-value capacitors (ceramic-type capacitors) should be placed as close as possible to the package pins. Larger-value capacitors (tantalum/electrolytic-type capacitors) can be placed farther away.
- The supply bypass capacitors should be connected as close as possible to the package pins to ensure a tight return path and maximize their effectiveness. When connecting from the package pin to the bypass capacitors, use as wide a plane / trace as possible to reduce inductive and resistive losses. Typical capacitor placement can be under the package (other side of the board) or on the same side but close. An example of bypass capacitors is shown below.

Component	Value[1]
Power Supply Bypass Capacitors	0.01 µF, 0.1 µF, 4.7 µF, 10.0 µF

1. Smaller-value capacitors must be placed between the ferrite bead and the package.

- Both power plane and ground plane should be maintained continuously and have solid return path (not in bits and pieces). Pay attention to the void areas caused by vias. If the planes are cut down by vias, we need to compensate for the loss of the plane shape to make sure the effective width of the plane.

3. 4L non-HDI PCB Design Rules

3.1. NSMD Pad

- Minimum pin pitch = 0.4 mm (15.75 mil)
- Footprint pad / Paste mask of pad = 10mil (bga10)
- Solder mask of pad = 10 mil

3.2. SMD Pad

- Minimum pin pitch = 0.381 mm (15 mil)
- Footprint pad / Paste mask of pad = 12 mil (bga12)
- Solder mask of pad = 8 mil

3.3. Via

- Minimum through hole pad / Drill size = 14 / 8 mil

3.4. Spacing

- Minimum trace-to-trace = 1 x trace width
- Minimum trace-to-via = 1 x trace width
- Minimum trace-to-pad = 1 x trace width

The example stack-up/trace width and spacing of 4L non-HDI PCB is shown below.

Stack-up		Thickness(mil)			DK	Df	Material
	SM_TOP (0.5_PT_1OZ)	0.5			3.4		
L1			1.654	0.333oz +Plating			
	PP (1080/RC=69%) / 0.076mm	2.99			4.14	0.019	S1000-2M
L2			1.26	1oz			
	Core+PP (1.3mm)	51.18			4.6	0.018	S1000-2M
L3			1.26	1oz			
	PP (1080/RC=69%) / 0.076mm	2.99			4.14	0.019	S1000-2M
L4			1.654	0.333oz +Plating			
	SM_BOT (0.5_PT_1OZ)	0.5			3.4		
Thickness(mil):	63.988	63.988					
FinishPCBThinckness(mm):	1.6 (+/-0.16) mm						
PressPCBThinkness(mm):	1.48 (+/-0.08) mm						

Number	Type	Control Layer	Referance Layer	Adjust Line Width (mil)	Adjust Spacing (mil)	Adjust Line To Copper (mil)	Design Impedance (ohm)
1	Single-End	L1/L4	L2/L3	3.6			55.01
2	Single-End	L1/L4	L2/L3	4			52.93
3	Single-End	L1/L4	L2/L3	4.5			50.15
4	Differential	L1/L4	L2/L3	3.5	3		84.62
5	Differential	L1/L4	L2/L3	3.6	4		90.11
6	Differential	L1/L4	L2/L3	3.4	5.8		99.3
7	Differential	L1/L4	L2/L3	4	4		88.41

4. PCB Routing Rules for SL2610 DDR3L/DDR4 & LPDDR4(x) Interface

Note:

- This guideline recommends optimal layout practices for the DRAM section and is not a set of strict limitations.
- Synaptics reference layouts follow the guidelines, ensuring good operating timing margins.
- It is strongly recommended to copy DDR routing from the reference design.

4.1. General Rules

The general rules of usage are:

- All signals must be routed with solid reference layer.
- Ground reference routing for all signals is preferred.
- No signal can be routed through discontinued reference.
- Impedance of single-ended signals should be targeted at a certain value within the small range of 50 Ω to 55 Ω ±10%
- All differential signals should have a differential impedance of 85 Ω ±10%.
- Via delay should be counted for length matching.
- No more than two vias on any signal between SoC and DRAMs is recommended. (Low speed DDR RSTn is not included in consideration).

4.2. Component Placement Guidelines for SL2610 and DRAM Power Integrity

- The DDR3L/DDR4/LPDDR4(x) signal pin assignments of SL2610 are designed to allow the DRAM chips to be placed next to SoC on top layer.
- Underneath SoC, the decoupling capacitors for VDDM is a combination of various capacitors that provide lower impedance from DC to 300MHz, it is highly recommended to follow the placement/values in Synaptics Reference Design Kits.
- RC components connecting to SL2610 M0_VREF should be placed as close to the pin as possible.
- A 1% 120 ohm (pulldown to GND) connecting to M0_CAL should be placed as close to the pin as possible.
- RC components connecting to SDRAM_CK0+/- should be placed as close to the SDRAM pins as possible.
- A pair of 1nF and 10nF capacitors should be placed at each individual power pin of SoC and all DRAMs as close as possible for decoupling purpose.
- A pair of 1nF and 10nF capacitors should be placed at the edge of power plane for reducing resonance purpose.
- All 1uF/10uF capacitors are suggested to be placed at the input of power rail for both SoC and DRAM, or at any bottleneck location of other power traces.

4.3. DDR3L/DDR4 Trace Length and Skew Guidelines

- Trace length difference of the DDR3L/DDR4 signals (within each own group) should be maintained in the following:
  - DDR3L:
    - DQ-to-DQ (including DQS) for each Byte group: keep shortest for each trace, trace length matching is not required (for DDR3 only)
    - Address / Command (ADCM) -to-ADCM (including CLK): keep shortest for each trace, trace length matching is not required (for DDR3 only).
  - DDR4:
    - DQ–DQS total length matching within ±70 ps
    - DQS+ to DQS- skew ≤ 4.5 ps
- Intra-pair of Differential signals (DQS+/-, CLK+/-): 15 mil
- The stub length from the via of each CK0+/- trace to the resistor pad should be kept within 50 mil.

4.4. DDR3L/DDR4/LPDDR4(x) Package Trace Length Compensation

- Trace lengths between the chip die and package pins were not well matched due to package geometry, causing varying propagation delays and impacting timing margins. To compensate for this mismatch, proper PCB routing is essential. Refer to the table below for the electrical length of individual traces.
- Note that compensation should be made in addition to any special trace matching or tuning requirements mentioned in the sections that follow.
- The detailed constraint information can be found in the Synaptics reference layout files.

Table 1. Propagation Delay of Byte Lane 0 Group

Byte Lane 0 Group							
Pin	**Signal Net**	**DDR4 Signal**	**LPDDR4 Signal**	**DDR3L Signal**	**Package Substrate Trace Length (um)**	**Package Propagation Delay (ps)**	**Equivalent PCB Trace Length Based on Propagation delay Entered (mil)**
G2	M0_DQSn[0]	M0_DDR4_DQS0n	M0_LPDDR4_DQS1n	M0_DDR3L_DQS0n	5178.341	31.23	191.60
G1	M0_DQSp[0]	M0_DDR4_DQS0p	M0_LPDDR4_DQS1p	M0_DDR3L_DQS0p	5493.159	33.13	203.25
J6	M0_DM[0]	M0_DDR4_DM0	M0_LPDDR4_DM1	M0_DDR3L_DM0	2741.372	16.53	101.43
H2	M0_DQ[0]	M0_DDR4_DQ0	M0_LPDDR4_DQ8	M0_DDR3L_DQ0	5086.269	30.68	188.20
J1	M0_DQ[1]	M0_DDR4_DQ1	M0_LPDDR4_DQ15	M0_DDR3L_DQ3	5183.7	31.26	191.80
J3	M0_DQ[2]	M0_DDR4_DQ2	M0_LPDDR4_DQ14	M0_DDR3L_DQ2	4455.265	26.87	164.85
J5	M0_DQ[3]	M0_DDR4_DQ3	M0_LPDDR4_DQ11	M0_DDR3L_DQ1	3698.43	22.31	136.84
K2	M0_DQ[4]	M0_DDR4_DQ4	M0_LPDDR4_DQ10	M0_DDR3L_DQ5	4285.386	25.85	158.56
J2	M0_DQ[5]	M0_DDR4_DQ5	M0_LPDDR4_DQ9	M0_DDR3L_DQ4	4529.759	27.32	167.60
L2	M0_DQ[6]	M0_DDR4_DQ6	M0_LPDDR4_DQ12	M0_DDR3L_DQ7	4639.5	27.98	171.66
L6	M0_DQ[7]	M0_DDR4_DQ7	M0_LPDDR4_DQ13	M0_DDR3L_DQ6	2532.89	15.28	93.72

Table 2. Propagation Delay of Byte Lane 1 Group

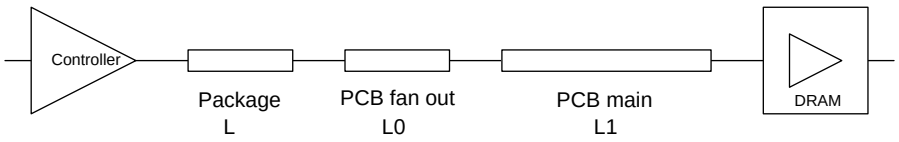
Byte Lane 1 Group							
Pin	**Signal Net**	**DDR4 Signal**	**LPDDR4 Signal**	**DDR3L Signal**	**Package Substrate Trace Length (um)**	**Package Propagation Delay (ps)**	**Equivalent PCB Trace Length Based on Propagation delay Entered (mil)**
D1	M0_DQSn[1]	M0_DDR4_DQS1n	M0_LPDDR4_DQS0n	M0_DDR3L_DQS1n	5777.886	34.85	213.79
D2	M0_DQSp[1]	M0_DDR4_DQS1p	M0_LPDDR4_DQS0p	M0_DDR3L_DQS1p	5630.78	33.96	208.34
D4	M0_DM[1]	M0_DDR4_DM1	M0_LPDDR4_DM0	M0_DDR3L_DM1	4547.985	27.43	168.28
C2	M0_DQ[8]	M0_DDR4_DQ8	M0_LPDDR4_DQ0	M0_DDR3L_DQ15	5521.61	33.30	204.30
E2	M0_DQ[9]	M0_DDR4_DQ9	M0_LPDDR4_DQ1	M0_DDR3L_DQ12	5007.082	30.20	185.27
F2	M0_DQ[10]	M0_DDR4_DQ10	M0_LPDDR4_DQ7	M0_DDR3L_DQ14	5198.877	31.35	192.36
F4	M0_DQ[11]	M0_DDR4_DQ11	M0_LPDDR4_DQ5	M0_DDR3L_DQ10	4167.23	25.13	154.19
G6	M0_DQ[12]	M0_DDR4_DQ12	M0_LPDDR4_DQ3	M0_DDR3L_DQ13	3360.915	20.27	124.36
F1	M0_DQ[13]	M0_DDR4_DQ13	M0_LPDDR4_DQ6	M0_DDR3L_DQ8	5598.213	33.76	207.14
F3	M0_DQ[14]	M0_DDR4_DQ14	M0_LPDDR4_DQ2	M0_DDR3L_DQ9	4345.803	26.21	160.80
G4	M0_DQ[15]	M0_DDR4_DQ15	M0_LPDDR4_DQ4	M0_DDR3L_DQ11	3794.001	22.88	140.38

Table 3. Propagation Delay of Address / Command / Control Group

ADDRESS / COMMAND / CONTROL Group							
Pin	Signal Net	DDR4 Signal	LPDDR4 Signal	DDR3L Signal	Package Substrate Trace Length (um)	Package Propagation Delay (ps)	Equivalent PCB Trace Length Based on Propagation delay Entered (mil)
M3	M0_CKn	M0_DDR4_CKn	M0_LPDDR4_CKn	M0_DDR3L_CKn	4234.202	25.54	156.67
N3	M0_CKp	M0_DDR4_CKp	M0_LPDDR4_CKp	M0_DDR3L_CKp	4224.001	25.48	156.29
W3	M0_A[0]	M0_DDR4_A0	LPDDR4_NC	M0_DDR3L_A5	3961.842	23.89	146.59
W7	M0_A[1]	M0_DDR4_A1	LPDDR4_NC	M0_DDR3L_BA0	3134.222	18.90	115.97
AA3	M0_A[2]	M0_DDR4_A2	M0_LPDDR4_A0	M0_DDR3L_A13	4204.208	25.36	155.56
W6	M0_A[3]	M0_DDR4_A3	LPDDR4_NC	M0_DDR3L_BA2	3028	18.26	112.04
V2	M0_A[4]	M0_DDR4_A4	M0_LPDDR4_A5	M0_DDR3L_A3	4601.548	27.75	170.26
R3	M0_A[5]	M0_DDR4_A5	LPDDR4_NC	M0_DDR3L_A8	4073.575	24.57	150.72
Y1	M0_A[6]	M0_DDR4_A6	M0_LPDDR4_A2	M0_DDR3L_A9	5493.142	33.13	203.25
U3	M0_A[7]	M0_DDR4_A7	LPDDR4_NC	M0_DDR3L_A14	3878.462	23.39	143.51
AA2	M0_A[8]	M0_DDR4_A8	M0_LPDDR4_A1	M0_DDR3L_A11	5136.405	30.98	190.05
Y2	M0_A[9]	M0_DDR4_A9	LPDDR4_NC	M0_DDR3L_A1	4455.35	26.87	164.85
U2	M0_A[10]	M0_DDR4_A10	M0_LPDDR4_A3	M0_DDR3L_A12	4327.679	26.10	160.13
AB3	M0_A[11]	M0_DDR4_A11	LPDDR4_NC	M0_DDR3L_A7	4446.522	26.82	164.52
R4	M0_A[12]	M0_DDR4_A12	LPDDR4_NC	M0_DDR3L_WEn	3610.94	21.78	133.61
U1	M0_A[13]	M0_DDR4_A13	M0_LPDDR4_A4	M0_DDR3L_A0	4901.54	29.56	181.36
U6	M0_ACTn	M0_DDR4_ACTn	LPDDR4_NC	M0_DDR3L_CASn	2632.241	15.88	97.39
V3	M0_BA[0]	M0_DDR4_BA0	LPDDR4_NC	M0_DDR3L_A2	4381.633	26.43	162.12
R2	M0_BA[1]	M0_DDR4_BA1	LPDDR4_NC	M0_DDR3L_A6	4399.352	26.53	162.78
U7	M0_BG[0]	M0_DDR4_BG0	LPDDR4_NC	M0_DDR3L_A15	2223.067	13.41	82.25
P1	M0_BG[1]	M0_DDR4_BG1	LPDDR4_NC	M0_DDR3L_BA1	4876.509	29.41	180.43
P2	M0_CASn	M0_DDR4_CASn	LPDDR4_NC	M0_DDR3L_A4	4415.193	26.63	163.36
N6	M0_CKE	M0_DDR4_CKE	M0_LPDDR4_CKE	M0_DDR3L_CKE	2584.036	15.58	95.61
M1	M0_CSn	M0_DDR4_CSn	M0_LPDDR4_CSn	M0_DDR3L_CSn	5207.708	31.41	192.69

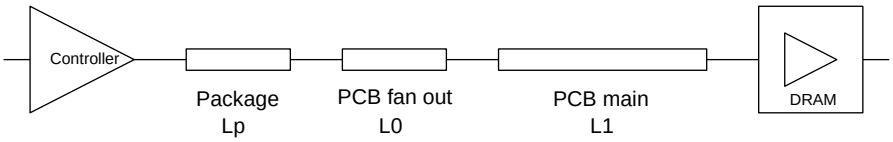
ADDRESS / COMMAND / CONTROL Group							
Pin	Signal Net	DDR4 Signal	LPDDR4 Signal	DDR3L Signal	Package Substrate Trace Length (um)	Package Propagation Delay (ps)	Equivalent PCB Trace Length Based on Propagation delay Entered (mil)
L5	M0_ODT	M0_DDR4_ODT	M0_LPDDR4_ODT	M0_DDR3L_ODT	3255.064	19.63	120.44
M2	M0_RASn	M0_DDR4_RASn	LPDDR4_NC	M0_DDR3L_A10	4570.127	27.56	169.10
N5	M0_WEn	M0_DDR4_WEn	LPDDR4_NC	M0_DDR3L_RASn	3358.069	20.25	124.25
AA4	M0_RSTn	DDR4_RSTn	M0_LPDDR4_RSTn	DDR3L_RSTn	4135.611	24.94	153.02
N8	M0_CAL	M0_CAL	M0_CAL	M0_CAL	1481.695	8.94	54.82

4.5. LPDDR4(x) Data (DQ/DM/DQS) Bus



- All signals use point-to-point routing topology.
- Place the DRAM chip as close to the SoC chip as possible to minimize the trace length from SoC to DRAM.
- The impedance of single-ended signals should be 50 Ω +/- 10%. In the BGA break-out area, it may be 55 Ω +/- 10%.
- The impedance of differential pairs should be 85 Ω +/- 10%.
- DQS must be routed in pairs on the same layer to match propagation delay and should use VSS instead of PWR as the reference plane for optimal current return.
- For each byte lane, the length matching for DQ(DM) to DQ(DM) (Lp + L0 + L1) should be within +/-40 ps.
- For each byte lane, the length matching for DQS to DQ(DM) (Lp + L0 + L1) should be within +/-40 ps.
- For each byte lane, the length matching for DQSp to DQSn (Lp + L0 + L1) should be within +/- 0.5 ps.
- The spacing (air gap between traces' edge) between single-ended signals should be:
  - more than 1x the trace width in the PCB fan-out section (L0).
  - more than 2x the trace width in the PCB main section (L1).
- The spacing (air gap between traces' edge) between DQSp / DQSn to other signals should be:
  - more than 1x the maximum intra-pair air gap or trace width in the PCB fan out section (L0).
  - more than 3x the maximum intra-pair air gap or trace width in the PCB main section (L1).

4.6. LPDDR4(x) CA Bus



- All signals use point-to-point routing topology.
- CLK must be routed in pairs on the same layer to match propagation delay and should use VSS instead of PWR as the reference plane for optimal current return.
- For each CA channel, the length matching for CA(CS) to CA(CS) (Lp + L0 + L1) should be +/- 65ps.
- For each CA channel, the length matching for CLK to CA(CS) (Lp + L0 + L1) should be +/- 65ps.
- For each CA channel, the length matching for CLKp to CLKn (Lp + L0 + L1) should be +/- 0.5ps.
- For each CA channel, the length matching for CLK to DQS (Lp + L0 + L1) should be +/-90ps.
- The spacing (air gap between traces' edge) between single-ended signals should be:
  - more than 1x the trace width in the PCB fan out section (L0).
  - more than 2x the trace width in the PCB main section (L1).
- The spacing (air gap between traces' edge) between CLKp / CLKn to other signals should be:
  - more than 1x the maximum intra-pair air gap or trace width in the PCB fan out section (L0).
  - more than 3x the maximum intra-pair air gap or trace width in the PCB main section (L1).

4.7. 4-Layer PCB Routing Example

4.7.1. Footprint

Please follow the dimension drawings specified in the Synaptics datasheet, with particular attention to pad and solder mask opening sizes:

- Pad size: 10 mil
- Solder mask opening: 10 mil

4.7.2. Layout Design Rule

- PCB board thickness: 1.6mm
- 4-layers PCB
- Single-ended trace width: 4 mil
- Single-ended trace impedance: 55 Ω ±10%
- Differential-pair trace width/spacing: 4.5/4 mil
- Differential-pair trace impedance: 85 Ω ±10%
- Minimum via (mechanical drilling) size: 8mil
- Maximal annulus of via: 16mil
- Minimum spacing (not including BGA area):
  - Pad to pad: 4mil
  - Pad to trace: 4mil
  - Pad to via: 4mil
  - Trace to trace: 4mil
  - Trace to via: 4mil
  - Via to via: 4mil

4.7.3. Board Stack-up

- The Synaptics EVK (Evaluation Kit) board uses the common 1.6mm PCB stack-up shown below.
- It is suggested that H34 (thickness between L3 and L4) be more than 5x the thickness of H12 (thickness between L1 and L2) to avoid cross talk between signals on L2 and L3.
- High-speed data signals that run on the top layer should reference L2 (VSS).
- Low-speed CA signals that run on the bottom layer should reference L3 (PWR).
- The placement and routing of the Synaptics reference design were derived through comprehensive signal integrity (SI) simulations, including model extraction and transient analysis, to ensure reliable timing closure. This is particularly critical for 4-layer PCB implementations due to the inherent non-homogeneity of microstrip transmission lines. As such, it is not feasible to define a single set of detailed routing rules applicable to all designs. Therefore, it is strongly recommended to follow the PCB layout of the Synaptics reference design. For custom PCB implementations, achieving timing closure through proper SI simulation is essential to ensure functional integrity and robust system performance.

Layer Name	Thickness	Dk @ 1GHz
Top SM	1.18 mil	3.8
Cu1	0.333oz + Planting	
Dielectric	3.2 mil	4.5
Cu2	1 oz	
Core	48.38	4.5
Cu3	1 oz	
Dielectric	3.2 mil	4.5
Cu4	0.333oz + Planting	
Bottom SM	1.18 mil	3.8

4.8. DDR3L/DDR4/LPDDR4(x) Routing Compliance Summary

Table 4. DDR3L/DDR4/LPDDR4(x) Routing Compliance Summary

Summary	DDR3L	DDR4	LPDDR4(x)
DQ–DQS skew (total length)	Not required (minimize only)	≤ 70 ps	≤ 40 ps
DQS+ to DQS- skew	≤ 15 mil	≤ 4.5 ps	≤ 0.5 ps
CLKp/n - skew	≤ 15 mil	≤ 4.5 ps	≤ 0.5 ps
Diff impedance	85 Ω ±10%	85 Ω ±10%	85 Ω ±10%
SE impedance	50–55 Ω ±10%	50–55 Ω ±10%	50 Ω (55 Ω in BGA) ±10%
Max vias per net	2 (excluding RSTn)	2 (excluding RSTn)	2 (excluding RSTn)

5. Revision History

Revision	Description
A	Initial release.

PN: 506-001629-01 Rev A