Application Note

Astra Machina Micro Evaluation Platform Kit General Design Layout Guidelines

Abstract: This application note provides PCB layout guidelines for the Astra™ Machina Micro Evaluation Platform Kit, with a focus on 6-layer HDI board design, high-speed signal integrity, and power supply decoupling. It covers best practices for differential pair routing, trace impedance control, length matching, via placement, and fanout strategies for FCCSP and WLCSP packages. These guidelines help ensure stable performance and design robustness across the platform.

  | PN: 506-001622-01 Rev A

Contents

1. PCB Layout Guidelines

- Use 100Ω ±10% differential trace impedance for CSI. For USB2.0, 90 Ω ±10% differential trace impedance is required. Other single-ended signals should maintain a characteristic trace impedance of 50 Ω ±10%.
- Match signal lengths within the same interface to less than 0.5mm (≈0.02 in). For high-speed differential pairs, maintain length matching within 0.25 mm (≈0.01 in) or less.
- Match the skew between any data lane and clock lane within ±10 ps on both the package and PCB.
- Ensure a continuous solid ground plane beneath signal traces to provide a consistent return path. Avoid routing traces across different reference planes or over anti-pads.
- Minimize vias on differential traces. To keep symmetry within a differential pair, must place the same number of vias on each trace. Place ground vias close to the cluster of signal vias to ensure the shortest possible return path..
- To reduce crosstalk, take care of signal traces which are routed close to the data differential pairs. The minimum recommended spacing is 3x trace width for low-speed non-periodic signals, and 7x trace width for high-speed periodic signals. A continuous ground plane below the differential traces is required.

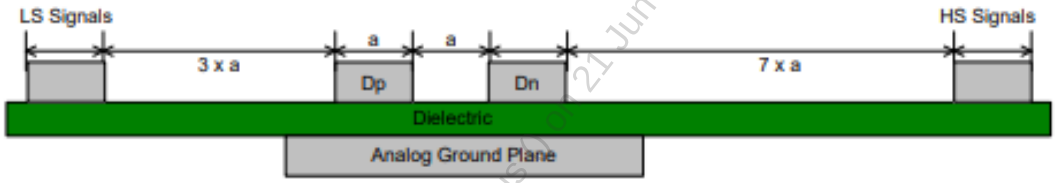

Figure 1. Recommended Spacing for Differential Pairs to Minimize Crosstalk from Adjacent Signals

- Avoid routing TX and RX pairs side-by-side on the same signal layer to reduce crosstalk.
- Total crosstalk from all aggressors must be accounted for and should remain below the -3 dB threshold up to the Nyquist frequency.

2. Power Supply Guidelines

- Allocating decoupling capacitors underneath main MCU is recommended to reduce ground bounce. Noise analysis of the power delivery network is required to determine the actual values. Depending on their size, each capacitor will have a different equivalent series resistance (ESR) and equivalent series inductance (ESL) that will determine the given capacitor's effectiveness over a frequency range. In general, several small-value capacitors (ceramic-type capacitors) should be placed as close as possible to the package pins. Larger-value capacitors (tantalum/electrolytic-type capacitors) can be placed farther away.
- The supply bypass capacitors should be connected as close as possible to the package pins to shorten return path and maximize their effectiveness. When connecting from the package pin to the bypass capacitors, use as wide as possible plane / trace to reduce inductive and resistive losses. Typical capacitor placement can be under the package (opposite side of the board) or on the same side but closed. An example of bypass capacitors is shown below.

Component	Value[1]
Power Supply Bypass Capacitors	0.01 µF, 0.1 µF, 4.7 µF, 10.0 µF

1. Smaller-value capacitors must be placed between the ferrite bead and the package.

- Both power and ground planes should be continuous and provide a solid return path—not fragmented or broken into isolated sections. Special attention should be given to voids caused by vias. If vias disrupt the plane continuity, the layout must be adjusted to compensate for the loss of copper area and ensure sufficient effective plane width is maintained.

3. 6L HDI PCB Design Rules

3.1. SMD Pad - FCCSP

- Minimum pin pitch = 0.386 mm (15.2 mil)
- Footprint pad / Paste mask of pad = 12 mil / 9 mil (CSP)
- Solder mask of pad = 8 mil

3.2. SMD Pad – WLCSP

- Minimum pin pitch = 0.41 mm (16.1875 mil)
- Footprint pad / Paste mask of pad = 8 mil / 8 mil (CSP)
- Solder mask of pad = 7 mil

3.3. Via

- Minimum through hole pad / Drill size = 16 / 8 mil
- Minimum blind via pad / Drill size = 10 / 4 mil (1-2 Layer, 5-6 Layer)
- Minimum buried via pad / Drill size = 12 / 6 mil (2-5 Layer)

3.4. Spacing

- Minimum trace-to-trace = 3 mil
- Minimum trace-to-via = 3 mil
- Minimum trace-to-pad = 2.5 mil

The example stack-up/trace width and spacing of 6L HDI PCB is shown in Figure 2 and Table 1.

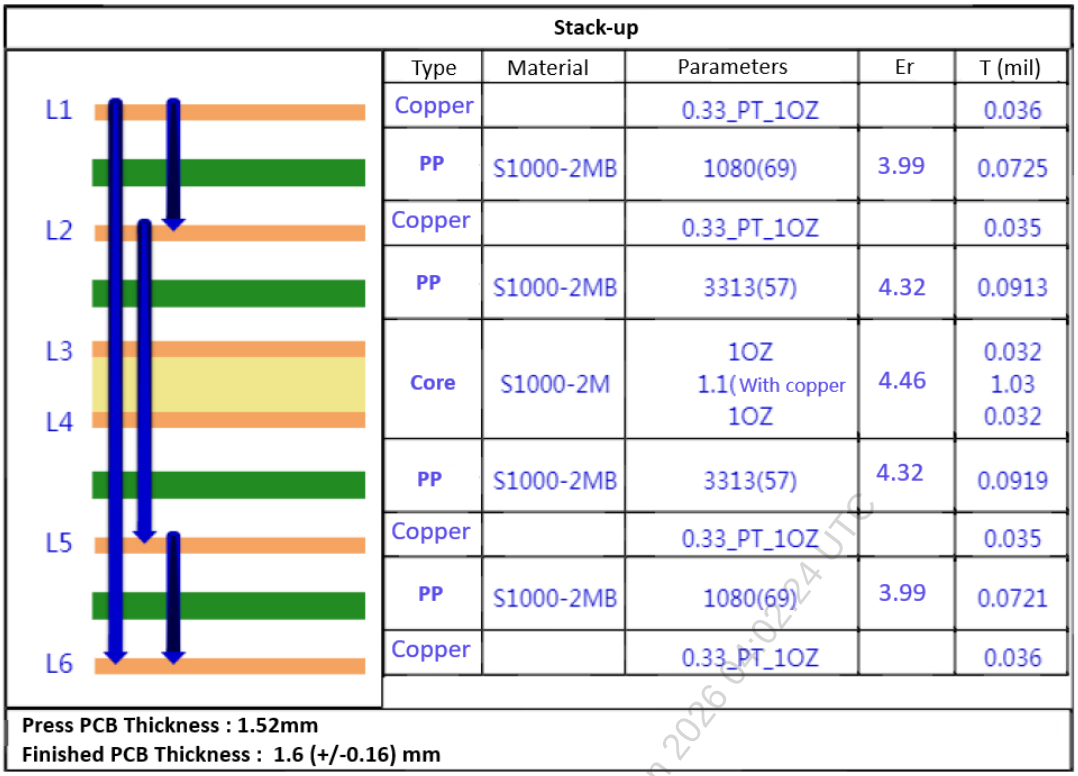

Figure 2. Example Stack-up/trace width

Table 1. Stack-up/trace width and spacing of 6L HDI PCB

Number	Type	Control layer	Reference layer	Adjust Line Width (mil)	Adjust Spacing (mil)	Design Impedance (ohm)
1	Single-End	L1	L2	3.6	—	55
2	Single-End	L6	L5	3.6	—	55
3	Single-End	L3	L2/L5	3.4	—	55
4	Single-End	L4	L2/L5	3.4	—	55
5	Differential	L1	L2	3.2	3	90
6	Differential	L6	L5	3.2	3	90
7	Differential	L1	L2	3	4.2	100
8	Differential	L6	L5	3	4.2	100

4. Chip Fanout

- Both SR1xx FCCSP and WLCSP packages support full function fanout using a 6-layer HDI PCB design. A 4-layer non-HDI PCB design may also be used with the FCCSP-122 package, though with limited functionality.

Note: These guidelines provide recommended practices for optimal fanout layout and are not a set of strict requirements.

4.1. FCCSP-122pin Fanout

SR1xx MCU platforms using the FCCSP package can be implemented on a non-HDI PCB if interfaces from inner balls are not required. The impact interfaces are SDIO1, SWIRE, and part of xSPI for pSRAM. The example in Figure 3 demonstrates a fanout layout for this configuration.

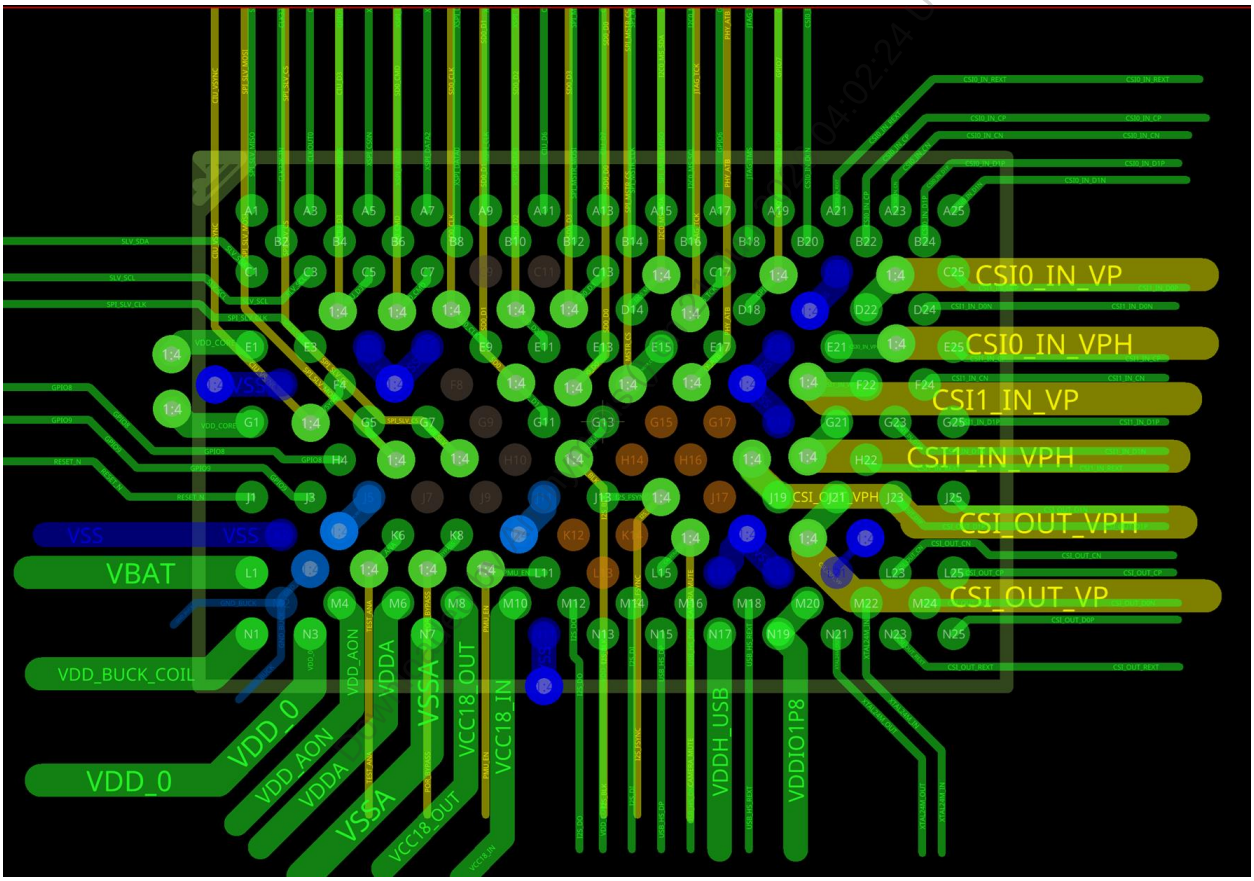

Figure 3. Impact interfaces: SDIO1, SWIRE, and part of xSPI for pSRAM

5. Revision History

Revision	Description
A	Initial Release

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