Application Note

Astra Machina Foundation Series I2S PDM Interfaces

Abstract: This document details the I2S and PDM Interfaces of the Astra™ Machina SoC.

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Overview

The Astra Machina Foundation Series offers evaluation-ready kits that facilitate quick and straightforward prototyping with the Synaptics SL-Series of embedded Linux® and Android™ processors. Featuring a modular design, these kits include interchangeable core compute modules, a standard I/O board and variety of daughter cards for connectivity, debugging, and various I/O configurations.

1.1. Scope

This document offers overview connection interface diagrams, audio clock schemes, sampling rates, and bit clocks specifically for core modules containing the Astra Machina SoC.

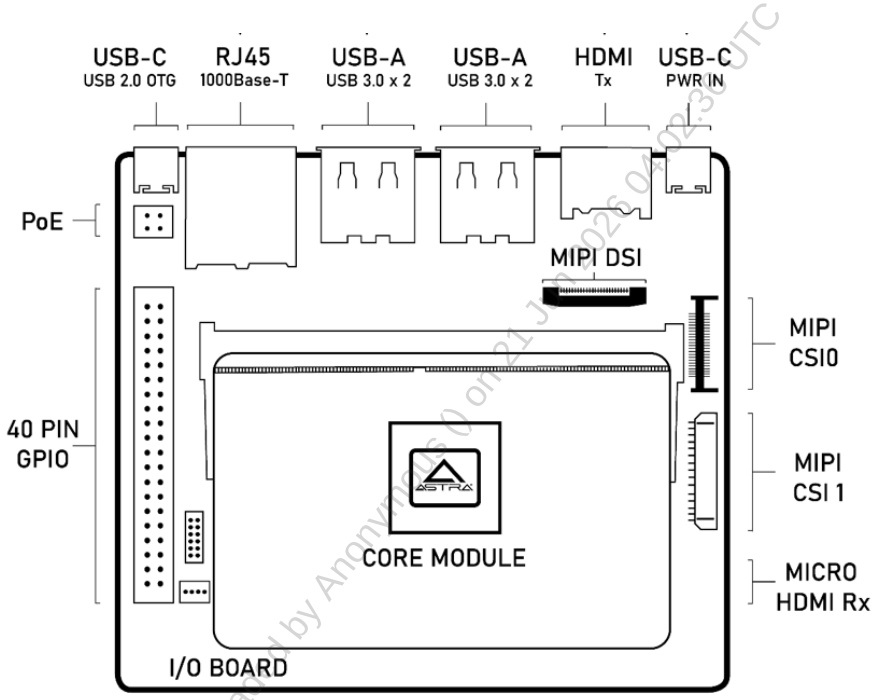

Figure 1. Overview of Astra Machina Foundation Series

1.1.1. 40-Pin header on I/O board interfaces

Table 1. I2S, PDM signals on SL1640 I/O board to 40-pin Header

SL1640 SoC GPIO/GPO	Availability	Direction	Default Function	40-pin Header
SOC_GPO[7]	MODE_2	OUT	IO:PDMB_CLKIO	Pin #27
SOC_GPIO[8]	MODE_2	IN	I:PDMA_DI[0]	Pin #29
SOC_GPIO[9]	MODE_2	IN	I:PDMA_DI[1]	Pin #28
SOC_GPIO[11]	MODE_1	IN	I:I2S2_DI[0]	Pin #15
SOC_GPIO[12]	MODE_1	IN/OUT	IO:I2S2_BCLKIO	Pin #11
SOC_GPIO[13]	MODE_1	IN/OUT	IO:I2S2_LRCKIO	Pin #13
SOC_GPIO[18]	MODE_1	OUT	IO:I2S1_MCLK	Pin #37
SOC_GPO[19]	MODE_1	OUT	O:I2S1_DO[0]	Pin #40
SOC_GPIO[20]	MODE_1	IN/OUT	IO:I2S1_BCLKIO	Pin #38
SOC_GPIO[21]	MODE_1	IN/OUT	IO:I2S1_LRCKIO	Pin #35

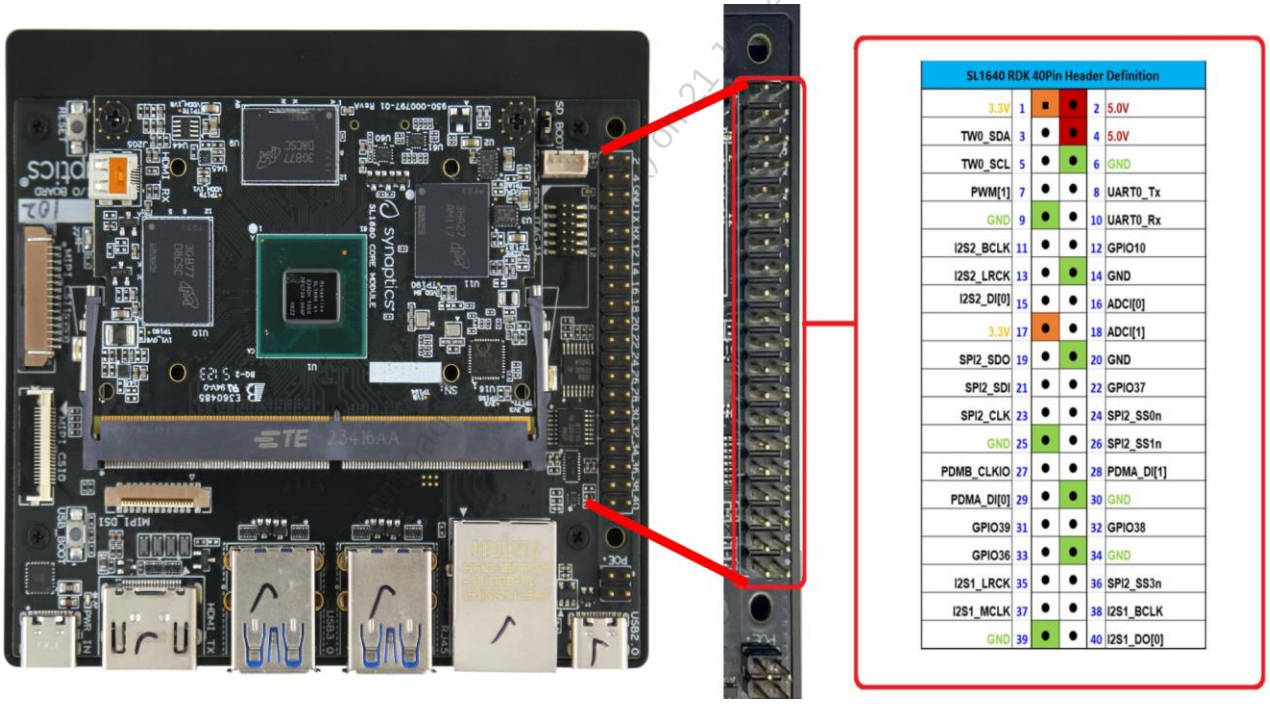

Figure 2. Astra Machina SL1640 Evaluation board 40-pin connector pin definition

Table 2. I2S, PDM signals on SL1620 I/O board to 40-pin Header

SL1620 SoC GPIO/GPO	Availability	Direction	Default Function	40-pin Header
GPIO[14]	MODE_1	OUT	IO:I2S1_LRCK	Pin #35
GPIO[15]	MODE_1	OUT	IO:I2S1_BCLK	Pin #38
GPO[16]	MODE_1	OUT	O:I2S1_DO	Pin #40
GPIO[17]	MODE_1	OUT	IO:I2S1_MCLK	Pin #37
GPIO[18]	MODE_1	IN	I:I2S1_DI	Pin #15
GPIO[23]	MODE_1	IN	I:PDM_DI[1]	Pin #28
GPIO[25]	MODE_1	OUT	IO:PDM_CLKIO	Pin #27

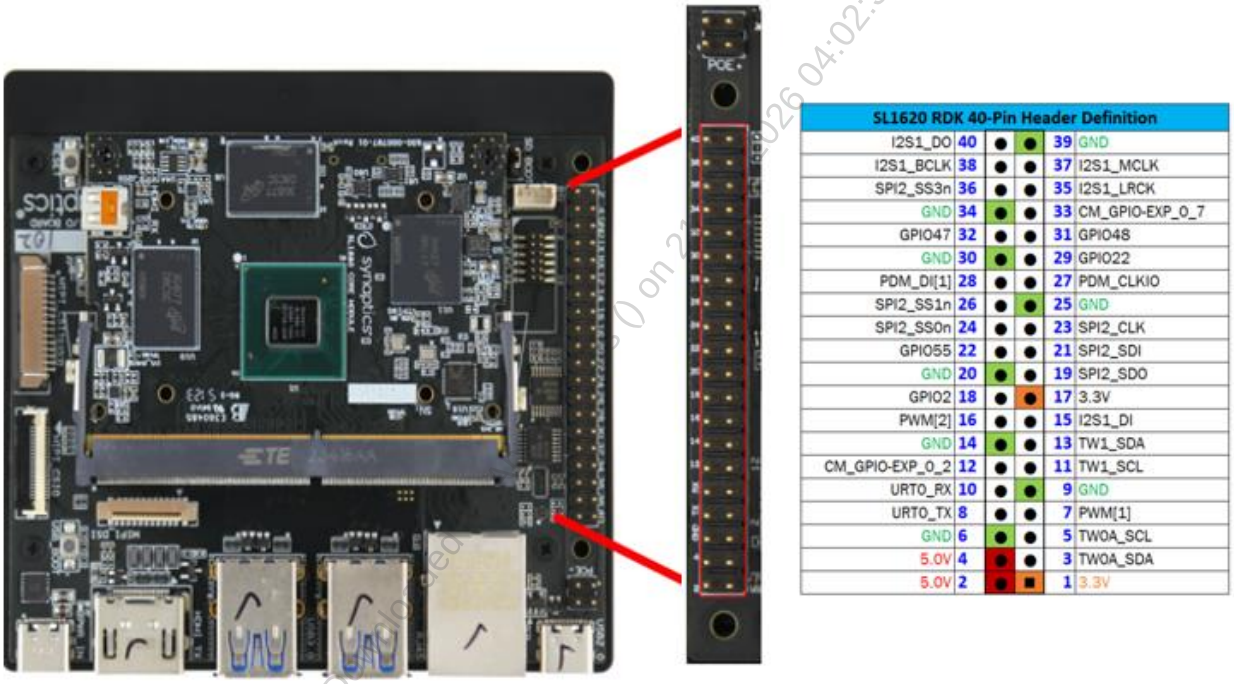

Figure 3. Astra Machina SL1620 Evaluation board 40-pin connector pin definition

Table 3. I2S, PDM signals on SL680 I/O board to 40-pin Header

SL1680 SoC GPIO/GPO	Availability	Direction	Default Function	GPIO Signaling
SOC_GPO[7]	MODE_2	OUT	IO:PDMB_CLKIO	Pin #27
SOC_GPIO[8]	MODE_2	IN	I:PDMA_DI[0]	Pin #29
SOC_GPIO[9]	MODE_2	IN	I:PDMA_DI[1]	Pin #28
SOC_GPIO[11]	MODE_1	IN	I:I2S2_DI[0]	Pin #15
SOC_GPIO[12]	MODE_1	IN/OUT	IO:I2S2_BCLKIO	Pin #11
SOC_GPIO[13]	MODE_1	IN/OUT	IO:I2S2_LRCKIO	Pin #13
SOC_GPIO[18]	MODE_1	OUT	IO:I2S1_MCLK	Pin #37
SOC_GPO[19]	MODE_1	OUT	O:I2S1_DO[0]	Pin #40
SOC_GPIO[20]	MODE_1	IN/OUT	IO:I2S1_BCLKIO	Pin #38
SOC_GPIO[21]	MODE_1	IN/OUT	IO:I2S1_LRCKIO	Pin #35

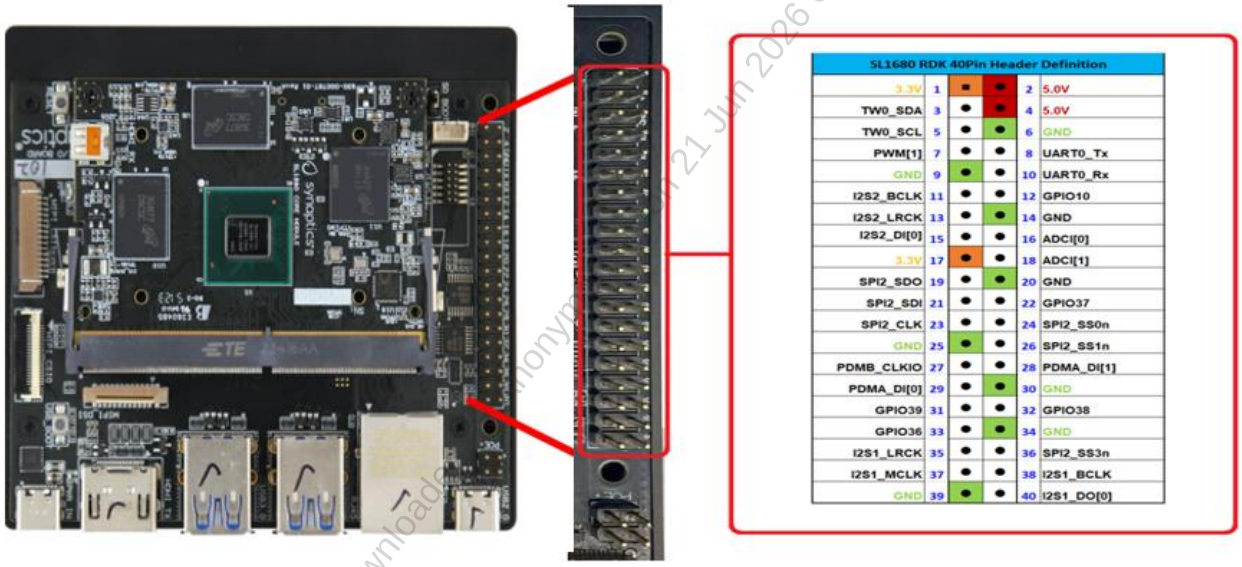

Figure 4. Astra Machina SL1680 Evaluation board 40-pin connector pin definition

Table 4. I2S, PDM signals on SL2610 I/O board to 40-pin Header

SL2610 SoC GPIO/GPO	Availability	Direction	Default Function	GPIO Signaling
SM_GPIO[2]	MODE_3	OUT	IO: I2S2_MCLK	Pin #37
SOC_GPIO[5]	MODE_1	IN/OUT	IO: I2S2_LRCKIO	Pin #35
SOC_GPIO[6]	MODE_1	IN/OUT	IO: I2S2_BCLKIO	Pin #38
SOC_GPIO[7]	MODE_1	OUT	I: I2S2_DO	Pin #40
SOC_GPIO[8]	MODE_1	IN	IO: I2S2_DI	Pin #15
SOC_GPIO[9]	MODE_4	IN	IO: PDM_DI1	Pin #28
SOC_GPIO[11]	MODE_4	OUT	IO: PDM_CLKIO	Pin #27

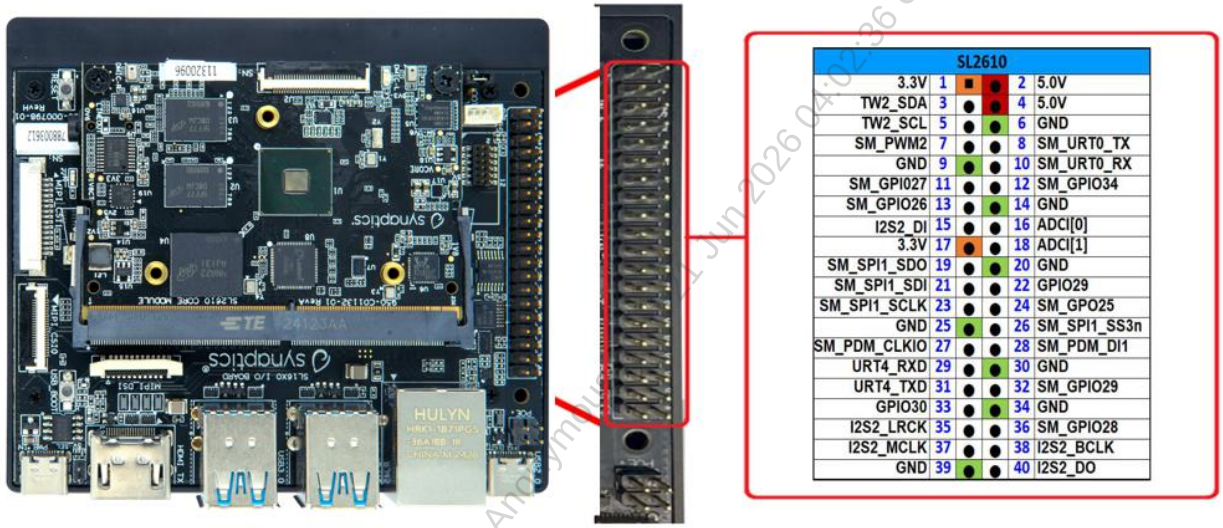

Figure 5. Astra Machina SL2610 Evaluation board 40-pin connector pin definition

1.2. Astra Machina Audio Clock Scheme

Each I2S (TX+RX pair) or PDM of AIO has its own MCLK (host clock). Two independent clocks from APLL are used to generate these MCLKs. There are independent dividers for each MCLK to fine adjust their required frequencies. BCLKs are derived from MCLKs using another set of dividers.

1.3. Astra SL1640 SoC Functional Block Diagram

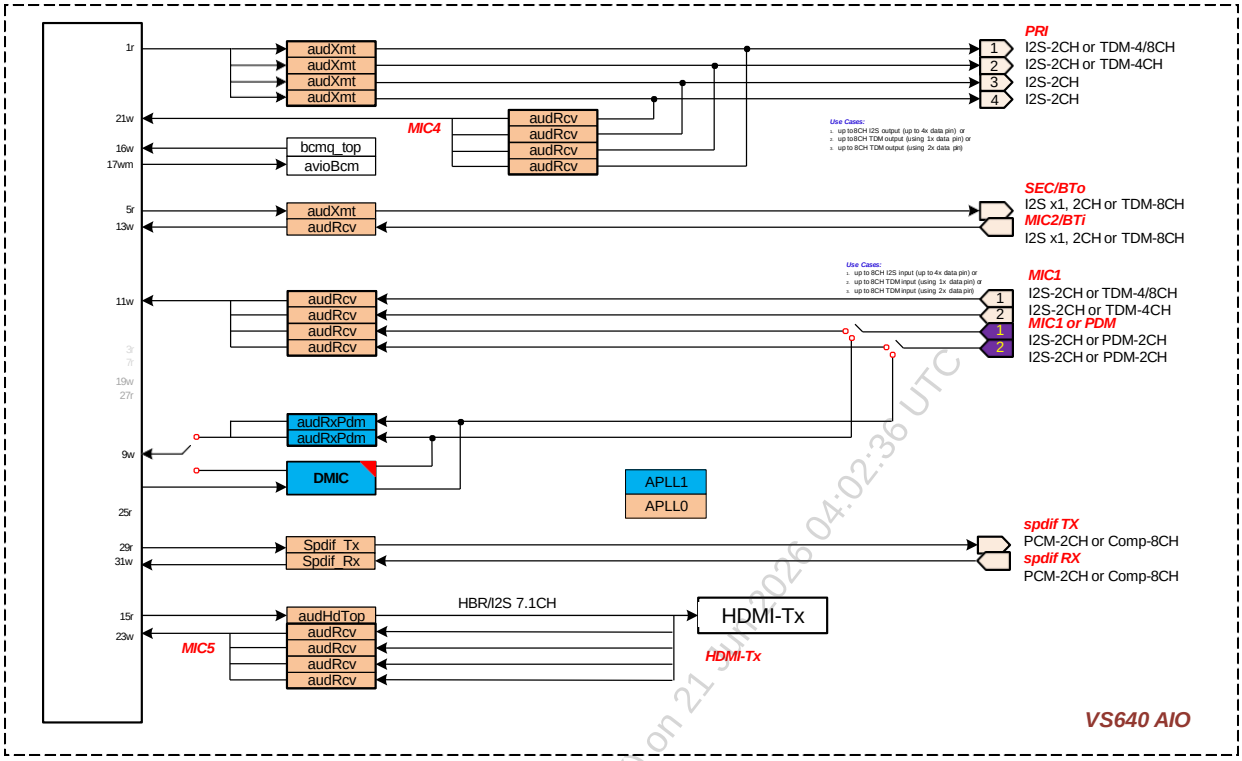

Figure 6. Astra SL1640 SoC functional block diagram

For each input/output ports, there are audio FIFOs between the DMA channel and the Transmitter/Receiver block. In unexpected or error cases when underflow or overflow happens, an interrupt will be generated. All the FIFOs can be flushed by firmware.

The SL1640 AIO module also has audio clock logic to generate the various sampling clocks (Bit-Clocks or BCLK) required for each port by dividing from Host Clock (MCLK). The source of MCLK is driven by the APLLs.

The audio clock module generates the data BCLK for AIO module by dividing the input Host Clock (MCLK) by 1/ 2/4/8/16/32/64/128/256/512/1024. The desired BCLK clock frequency and polarity can be selected by programming the AIO registers.

1.3.1. Astra SL1640 SoC Sampling Rate and Bit Clock

The bit clock toggles once for each discrete bit of data on the data lines. The bit clock frequency is derived by the number of bits per channel, the number of channels, and the sampling rate. For example, stereo audio (2 channels) with a sample frequency of 192 kHz and 16-bits per sample will have a bit clock frequency of 6.144 MHz (192 x 2 x 16). The Word Strobe clock (LRCK) indicates whether Left Channel or Right Channel data is currently being sent to the device. Transitions on the LRCK also serve as a start-of-word indicator. The LRCK frequency is always the same as the audio sampling rate. The sampling size and sampling rate must be same within the same channel pair and the same port.

Table 5 shows the required BCLK frequency for supported audio sampling rates at 32FS/48FS/64FS.

Table 5. SL1640 Sampling Rate and Bit Clock Relationship (I2S/LJ/RJ)

Sampling Rate (FS)	Bit- clock frequency (MHz)		
	32*FS (2-Ch)	48*FS (2-Ch)	64*FS (2-Ch)
32 kHz	1.02	1.536	2.048
44.1 kHz	1.4112	2.1168	2.8224
48 kHz	1.536	2.304	3.072
96 kHz	3.072	4.608	6.144
192 kHz	6.144	9.216	12.288

Table 6. SL1640 Sampling Rate and Bit Clock Relationship (TDM)

Sampling Rate (FS)	Bit- clock frequency (MHz)		
	128*FS (4-Ch)	192*FS (6-Ch)	256*FS (8-Ch)
32 kHz	4.096	6.144	8.192
44.1 kHz	5.6448	8.4672	11.2896
48 kHz	6.144	9.216	12.288
96 kHz	12.288	18.432	24.576
192 kHz	24.576	N/A	N/A

To generate desired frequencies for audio clocks, APLL must be first configured to generate required MCLKs. AIO clock dividers must be programmed to generate correct BCLKs and LRCKs from MCLKs.

1.4. Astra SL1620 SoC Functional Block Diagram

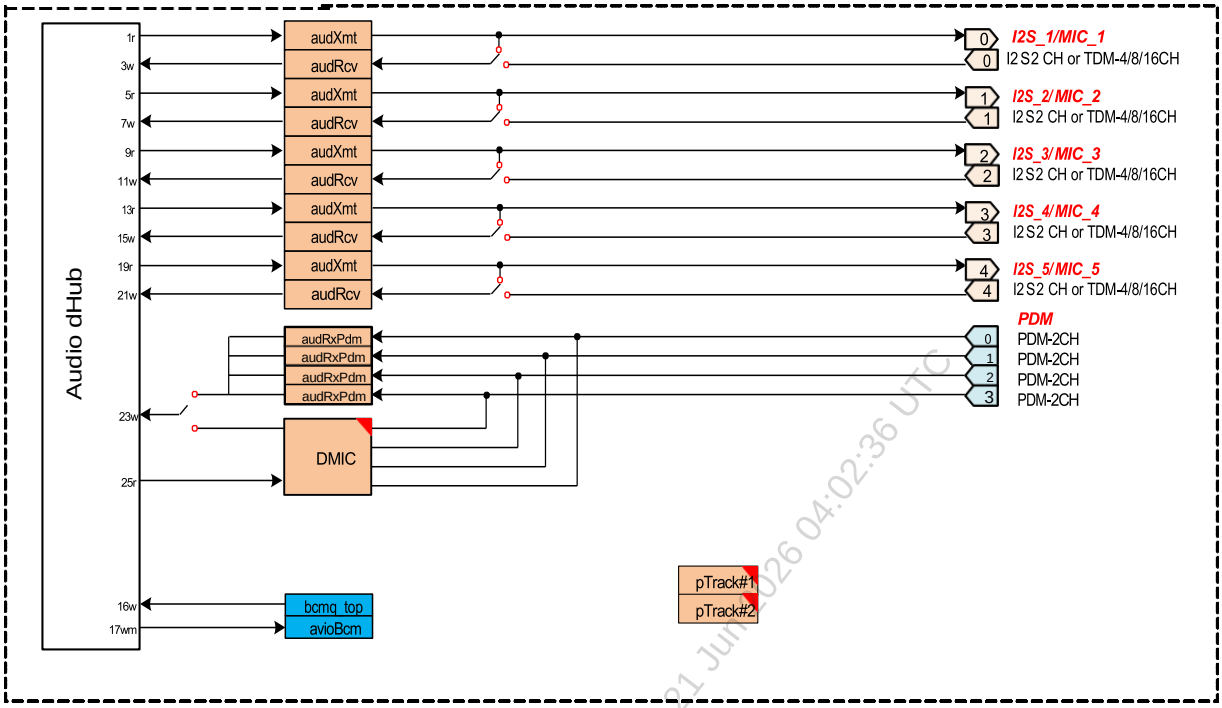

Figure 7. Astra SL1620 SoC functional block diagram

For each input/output ports, there are audio FIFOs between the DMA channel and the Transmitter/Receiver block. In unexpected or error cases when underflow or overflow happens, an interrupt will be generated. All the FIFOs can be flushed by firmware.

The SL1620 AIO module also has audio clock logic to generate the various sampling clocks (Bit-Clocks or BCLK) required for each port by dividing from Host Clock (MCLK). The source of MCLK is driven by the APLLs.

The audio clock module generates the data BCLK for AIO module by dividing the input Host Clock (MCLK) by 1/ 2/4/8/16/32/64/128/256/512/1024. The desired BCLK clock frequency and polarity can be selected by programming the AIO registers.

1.4.1. Astra SL1620 SoC Sampling Rate and Bit Clock

The bit clock toggles once for each discrete bit of data on the data lines. The bit clock frequency is derived by the number of bits per channel, the number of channels, and the sampling rate. For example, stereo audio (2 channels) with a sample frequency of 192 kHz and 16-bits per sample will have a bit clock frequency of 6.144 MHz (192 x 2 x 16). The Word Strobe clock (LRCK) indicates whether Left Channel or Right Channel data is currently being sent to the device. Transitions on the LRCK also serve as a start-of-word indicator. The LRCK frequency is always the same as the audio sampling rate. The sampling size and sampling rate must be same within the same channel pair and the same port.

Table 7 shows the required BCLK frequency for supported audio sampling rates at 32FS/48FS/64FS.

Table 7. SL1620 Sampling Rate and Bit Clock Relationship (I2S)

Sampling Rate (FS)	Bit- clock frequency (MHz)		
	32*FS (2-Ch)	48*FS (2-Ch)	64*FS (2-Ch)
32 kHz	1.02	1.536	2.048
44.1 kHz	1.4112	2.1168	2.8224
48 kHz	1.536	2.304	3.072
96 kHz	3.072	4.608	6.144
192 kHz	6.144	9.216	12.288

Table 8. SL1620 Sampling Rate and Bit Clock Relationship (TDM)

Sampling Rate (FS)	Bit- clock frequency (MHz)			
	128*FS (4-Ch)	192*FS (6-Ch)	256*FS (8-Ch)	512*FS (16-Ch
32 kHz	4.096	6.144	8.192	16.384
44.1 kHz	5.6448	8.4672	11.2896	22.579
48 kHz	6.144	9.216	12.288	24.576
96 kHz	12.288	18.432	24.576	49.152
192 kHz	24.576	36.864	49.152	Not supported

To generate desired frequencies for audio clocks, APLL must be first configured to generate required MCLKs. AIO clock dividers must be programmed to generate correct BCLKs and LRCKs from MCLKs.

1.5. Astra SL1680 SoC Functional Block Diagram

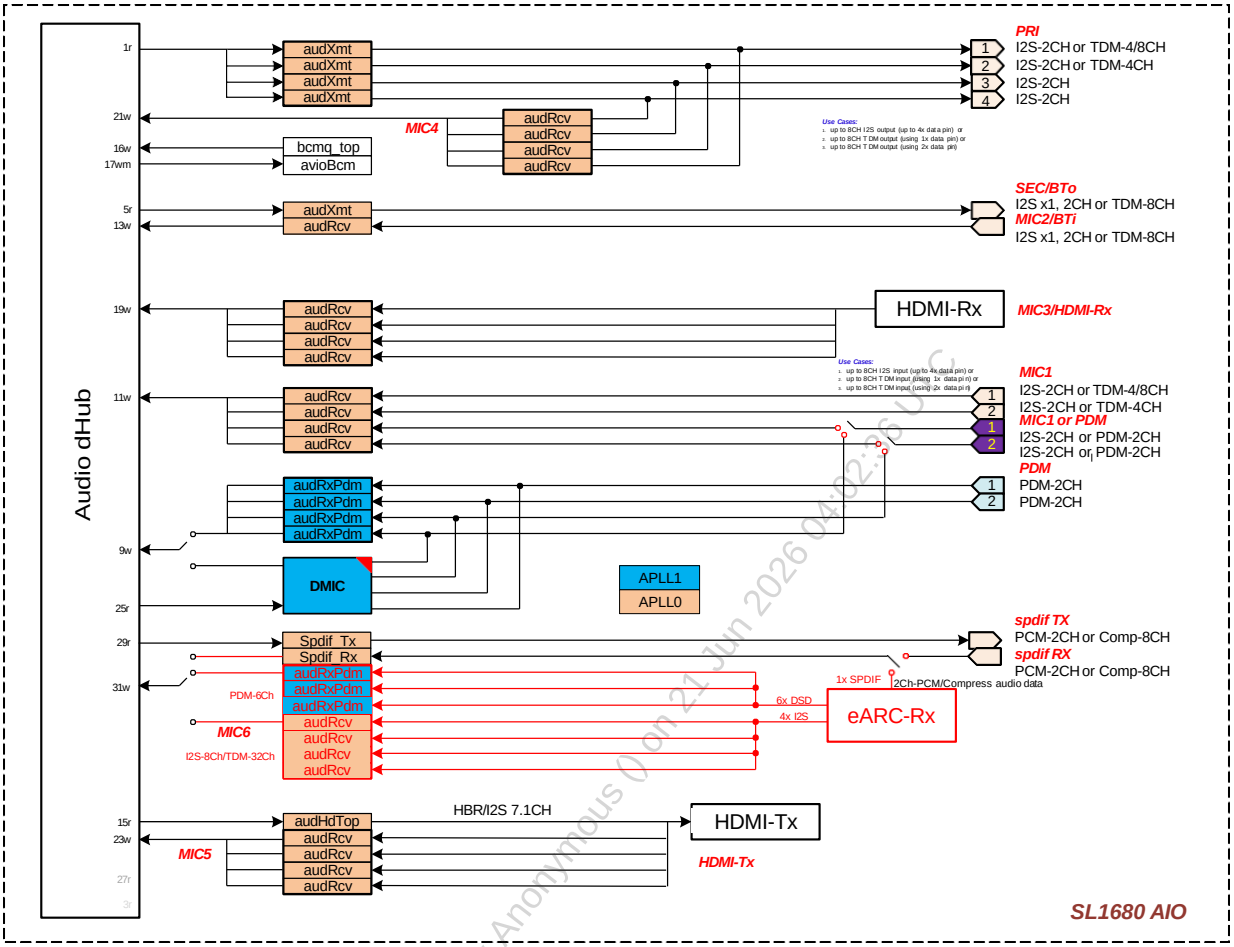

Figure 8. Astra SL1680 SoC functional block diagram

For each input/output ports, there are audio FIFOs between the DMA channel and the Transmitter/Receiver block. In unexpected or error cases when underflow or overflow happens, an interrupt will be generated. All the FIFOs can be flushed by firmware.

The SL1680 AIO module also has audio clock logic to generate the various sampling clocks (Bit-Clocks or BCLK) required for each port by dividing from Host Clock (MCLK). The source of MCLK is driven by the APLLs.

The audio clock module generates the data BCLK for AIO module by dividing the input Host Clock (MCLK) by 1/ 2/4/8/16/32/64/128. The desired BCLK clock frequency and polarity can be selected by programming the AIO registers.

1.5.1. Astra SL1680 SoC I2S Sampling Rate and Bit Clock

The bit clock toggles once for each discrete bit of data on the data lines. The bit clock frequency is derived by the number of bits per channel, the number of channels, and the sampling rate. For example, stereo audio (2 channels) with a sample frequency of 192 kHz and 16-bits per sample will have a bit clock frequency of 6.144 MHz (192 x 2 x 16). The Word Strobe clock (LRCK) indicates whether Left Channel or Right Channel data is currently being sent to the device. Transitions on the LRCK also serve as a start-of-word indicator. The LRCK frequency is always the same as the audio sampling rate. The sampling size and sampling rate must be same within the same channel pair and the same port.

Table 9 shows the required BCLK frequency for supported audio sampling rates at 32FS/48FS/64FS.

Table 9. SL1680 Sampling Rate and Bit Clock Relationship (I2S/LJ/RJ)

Sampling Rate (FS)	Bit- clock frequency (MHz)		
	32*FS (2-Ch)	48*FS (2-Ch)	64*FS (2-Ch)
32 kHz	1.02	1.536	2.048
44.1 kHz	1.4112	2.1168	2.8224
48 kHz	1.536	2.304	3.072
96 kHz	3.072	4.608	6.144
192 kHz	6.144	9.216	12.288

Table 10. SL1680 Sampling Rate and Bit Clock Relationship (TDM)

Sampling Rate (FS)	Bit- clock frequency (MHz)		
	128*FS (4-Ch)	192*FS (6-Ch)	256*FS (8-Ch)
32 kHz	4.096	6.144	8.192
44.1 kHz	5.6448	8.4672	11.2896
48 kHz	6.144	9.216	12.288
96 kHz	12.288	18.432	24.576
192 kHz	24.576	36.864	49.152

To generate desired frequencies for audio clocks, APLL must be first configured to generate required MCLKs. AIO clock dividers must be programmed to generate correct BCLKs and LRCKs from MCLKs.

1.6. Astra SL2610 SoC Functional Block Diagram

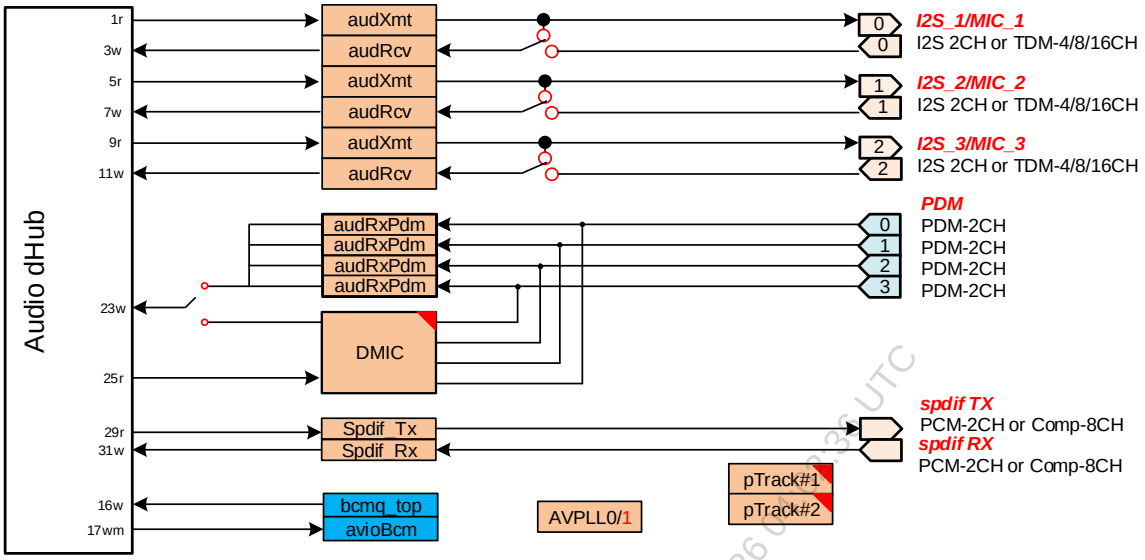

Figure 9. Astra SL2610 SoC functional block diagram

For each input/output ports, there are audio FIFOs between the DMA channel and the Transmitter/Receiver block. In unexpected or error cases when underflow or overflow happens, an interrupt will be generated. All the FIFOs can be flushed by firmware.

The SL2610 AIO module also has audio clock logic to generate the various sampling clocks (Bit-Clocks or BCLK) required for each port by dividing from Host Clock (MCLK). The source of MCLK is driven by the APLLs.

The audio clock module generates the data BCLK for AIO module by dividing the input Host Clock (MCLK) by 1/ 2/4/8/16/32/64/128/256/512/1024. The desired BCLK clock frequency and polarity can be selected by programming the AIO registers.

1.6.1. Astra SL2610 SoC Sampling Rate and Bit Clock

The bit clock toggles once for each discrete bit of data on the data lines. The bit clock frequency is derived by the number of bits per channel, the number of channels, and the sampling rate. For example, stereo audio (2 channels) with a sample frequency of 192 kHz and 16-bits per sample will have a bit clock frequency of 6.144 MHz (192 x 2 x 16). The Word Strobe clock (LRCK) indicates whether Left Channel or Right Channel data is currently being sent to the device. Transitions on the LRCK also serve as a start-of-word indicator. The LRCK frequency is always the same as the audio sampling rate. The sampling size and sampling rate must be same within the same channel pair and the same port.

Table 11 shows the required BCLK frequency for supported audio sampling rates at 32FS/48FS/64FS.

Table 11. SL2610 Sampling Rate and Bit Clock Relationship (I2S)

Sampling Rate (FS)	Bit- clock frequency (MHz)		
	32*FS (2-Ch)	48*FS (2-Ch)	64*FS (2-Ch)
32 kHz	1.02	1.536	2.048
44.1 kHz	1.4112	2.1168	2.8224
48 kHz	1.536	2.304	3.072
96 kHz	3.072	4.608	6.144
192 kHz	6.144	9.216	12.288
352,8 kHz	11.283	16.934	22.579
384 kHz	12.288	18.432	24.536

Table 12. SL2610 Sampling Rate and Bit Clock Relationship (TDM)

Sampling Rate (FS)	Bit- clock frequency (MHz)			
	128*FS (4-Ch)	192*FS (6-Ch)	256*FS (8-Ch)	512*FS (16-Ch
32 kHz	4.096	6.144	8.192	16.384
44.1 kHz	5.6448	8.4672	11.2896	22.579
48 kHz	6.144	9.216	12.288	24.576
96 kHz	12.288	18.432	24.576	49.152
192 kHz	24.576	36.864	49.152	Not supported

To generate desired frequencies for audio clocks, APLL must be first configured to generate required MCLKs. AIO clock dividers must be programmed to generate correct BCLKs and LRCKs from MCLKs.

1.7. Astra Machina Audio Data Format

The Astra Machina I2S Transmitters and Receivers supports I2S mode, Left-Justified mode, Right-Justified mode, TDM Mode, PCM Mono and PDM mode.

The following sections provide brief description about each of the supported data formats.

1.7.1. Astra Machina I2S Mode

In I2S mode, data is sent out "one" BCLK after the LRCK transition. In this mode left channel data are transmitted during the low period of LRCK and right channel data are transmitted during the high period of LRCK. Figure 10 shows the I2S mode.

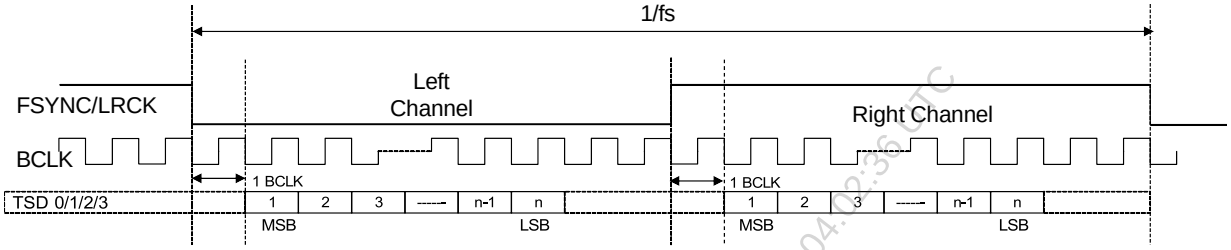

Figure 10. Astra Machina I2S Mode

1.7.2. Astra Machina I2S, Left-Justified Mode

In Left-Justified mode, there is no BCLK delay between the first data transmission and the LRCK transition and data is aligned with the leading transitions on LRCK. In this mode left channel data are transmitted during the high period of LRCK and right channel data are transmitted during the low period of LRCK. Figure 11 shows the Left-Justified mode.

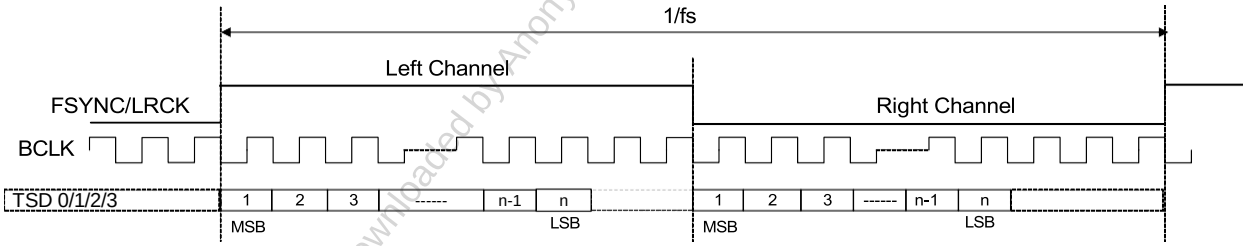

Figure 11. Astra Machina I2S, Left-Justified Mode

1.7.3. Astra Machina I2S, Right-Justified Mode

In Figure 12, the Right-Justified format is very similar to the Left-Justified format, except for the placement of channel data within the LRCK. In this mode, the data lines up with the right edge of LRCK transition and last bit of the data are transmitted one BCLK before the LRCK transition.

As with the Left-Justified mode, left channel data is transmitted during the high period of LRCK and right channel data are transmitted during the low period of LRCK. Figure below shows the Right-Justified mode.

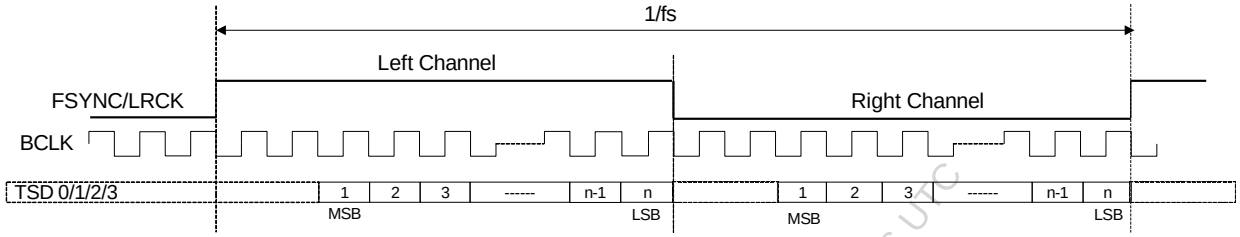

Figure 12. Astra Machina I2S, Right-Justified Mode

1.7.4. Astra Machina Time Division Multiplexed (TDM) Mode

The TDM format is typically used when communicating between integrated circuit devices on the same printed circuit board or on another printed circuit board within the same piece of equipment. For example, the TDM format is used to transfer data between the DSP and one or more analog-to-digital converter (ADC), digital-to- analog converter (DAC).

The TDM format consists of three components in a basic synchronous serial transfer: the clock (BCLK), the data (DIN / DOUT) and the frame sync (LRCK).

1. The BCLK for Transmit / Receive needed for 32bit resolution per channel:
    - SL1680 and SL1640:
        - 256 Clocks: 8-Channel
        - 192 Clocks: 6-Channel
        - 128 Clocks: 4-Channel
    - SL1620 and SL2610:
        - 512 Clocks: 16-Channel
        - 256 Clocks: 8-Channel
        - 192 Clocks: 6-Channel
        - 128 Clocks: 4-Channel

    Each 64 BCLK 2-Channel data is transmitted / received.
2. In I2S-TX, the LRCLK can be generated for:
    - **SL1680/SL1640**: 1-254 BCLK in an audio frame whereas in I2S-RX the module detects the low to high edge to start decoding the data.
    - **SL1620/SL2610**: 1-510 BCLK in an audio frame whereas in I2S-RX the module detects the low to high edge to start decoding the data.

3. The audio frame in TDM mode:
    - **SL1680/SL1640:** carries 2/4/6/8-Channels of data.
    - **SL1620/SL2610**: carries 2/4/6/8/16-Channels of data.
4. The data is always in I2S / Justified Mode.
    - In I2S mode, data is sent out *one* BCLK after the LRCK transition.
    - In Left-Justified mode, there is no BCLK delay between the first data transmission and the LRCK transition and data is aligned with the leading transitions on LRCK.
    - It is relatively apparent that the Right-Justified format is very similar to the Left-Justified format, with the exception that the placement of channel data within the LRCK. In this mode the data lines up with the right edge of LRCK transition and last bit of the data is transmitted one BCLK before the LRCK transition.

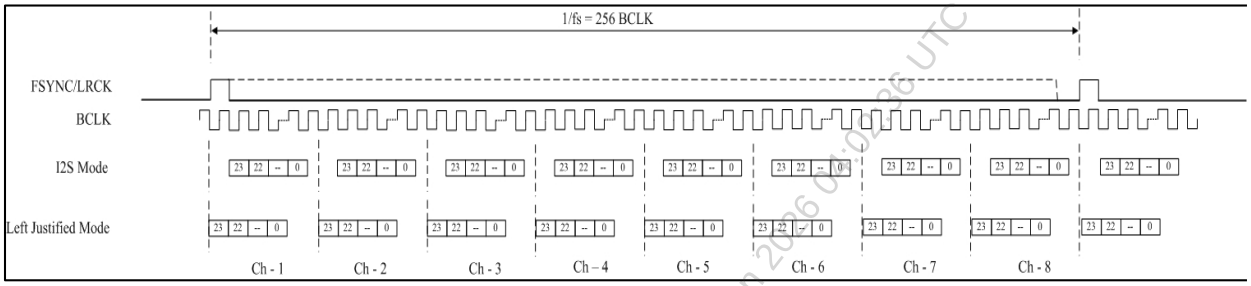

Figure 13. Astra Machina 8-Channel TDM Mode Data

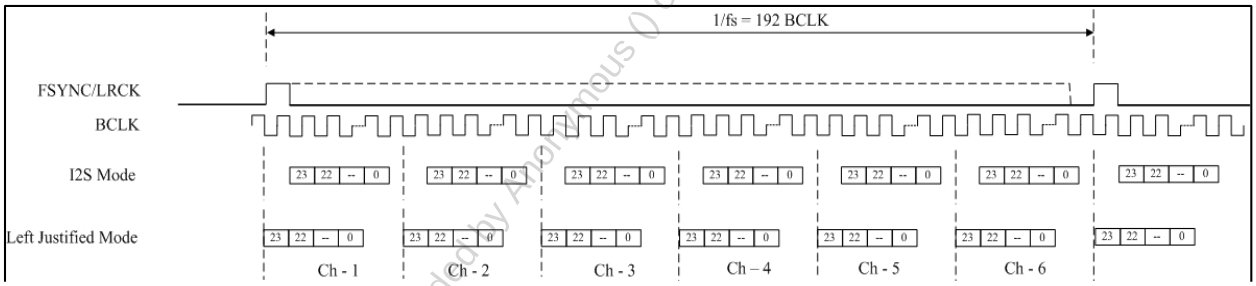

Figure 14. Astra Machina 6-Channel TDM Mode Data

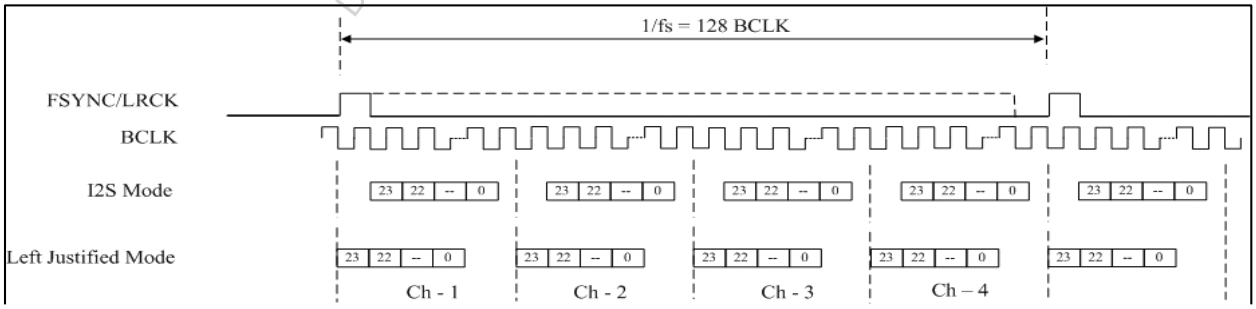

Figure 15. Astra Machina 4-Channel TDM Mode Data

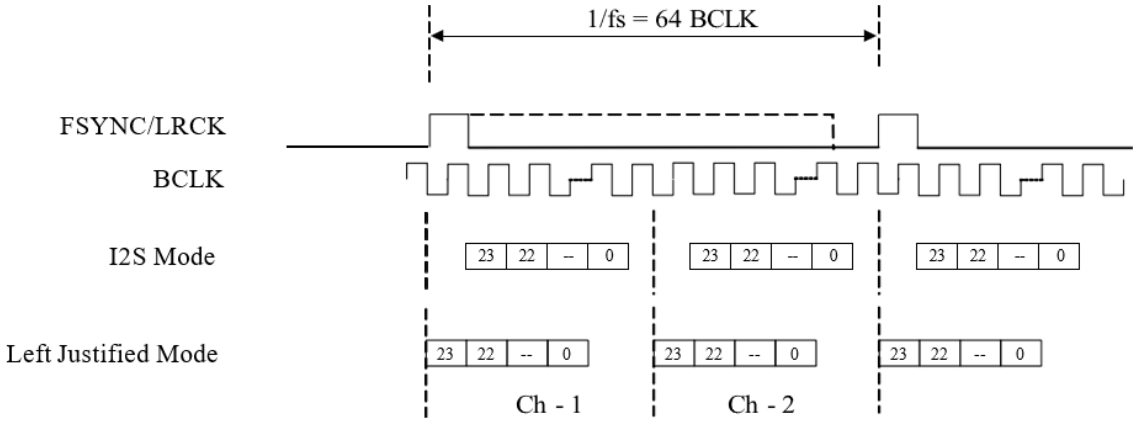

Figure 16. Astra Machina 2-Channel TDM Mode Data

1.7.5. Astra Machina PCM Mode

PCM mono channel data is used specifically for transfer of chunk data indicatively by a single pulse to start the data.

After the rising edge of the PCM_FR the data will be captured. The number of bits (Data resolution) which needs to be captured will be configurable between 8/16/24/32 Bits. Data is captured or sent on the falling edge.

When transmitter is operating in Host Mode the frame width, that is, the occurrence of PCM_FR pulses can also be configured between 8 to 256. While transmitter is operating in Target mode the frame width is defined by the Host Mode generating the PCM_FR, to take care of this there is a programming guideline to be followed.

The audio frame in TDM mode:

- **SL1680/SL1640:** carries 2/4/6/8-Channels of data.
- **SL1620/SL2610**: carries 2/4/6/8/16-Channels of data.

Figure 17 represents the data being sent by the transmitter.

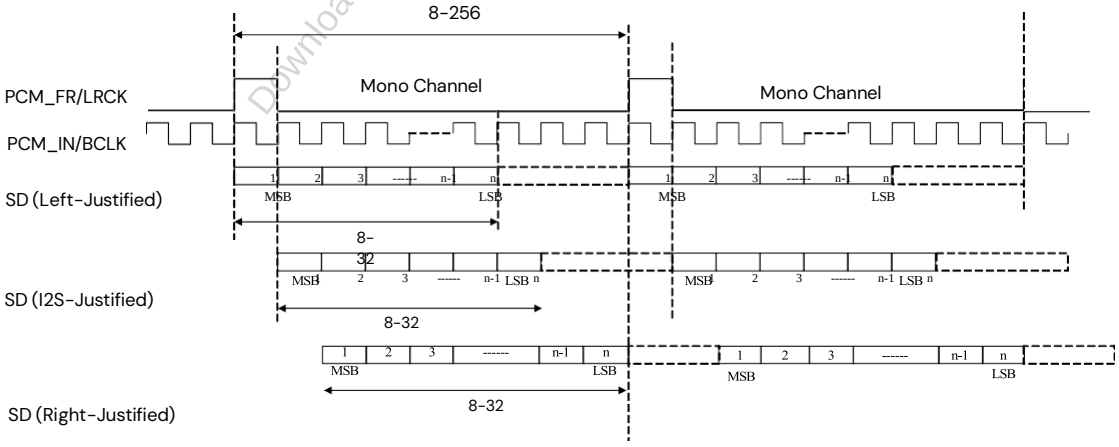

Figure 17. Astra Machina PCM Mono Mode Data

1.7.6. Astra Machina Pulse Density Modulation (PDM) Mode

AIO module in Astra Machina has a dedicated receiver to receive PDM digital input. In PDM mode, register configurable PDM clock is sent out from Astra SOC to the PDM device to clock the data bits. The data bits are presented by the PDM device at the clock rate, either on the rising edge/falling edge or both. Astra SOC samples the PDM data and stores in the DRAM.

Astra SOC supports both the PDM data transfer modes namely Classic PDM and Half Cycle PDM. In Classic PDM, the PDM device will present data on every rising (or falling) clock edge. In Half cycle PDM, the PDM device will present valid data on both the clock edges. Astra SoC samples the PDM data either using the internal PDM clock edges or a programmable counter running on internal high-speed clock, also number of bits to store per frame is configurable using the register settings.

Table 13. Astra Machina PDM clocks

Parameter	Condition	Min	Typ		Max	Units
PDM Clock Frequency	—	—	—		$F_{AIOSYSCLK}/4$[1]	MHz
Clock Duty Cycle	—	—	50		—	%

1. Where default of $F_{AIOSYSCLK}$ = 400 MHz for SL1680, 200 MHz for SL1640 and 300 MHz SL1620/SL2610.

Table 14. SL16xx FAIOSYSCLK clocks

Parameter	Condition	SL1680	SL1640	SL1620/SL2610	Units
$F_{AIOSYSCLK}$	Default	400	200	300	MHz

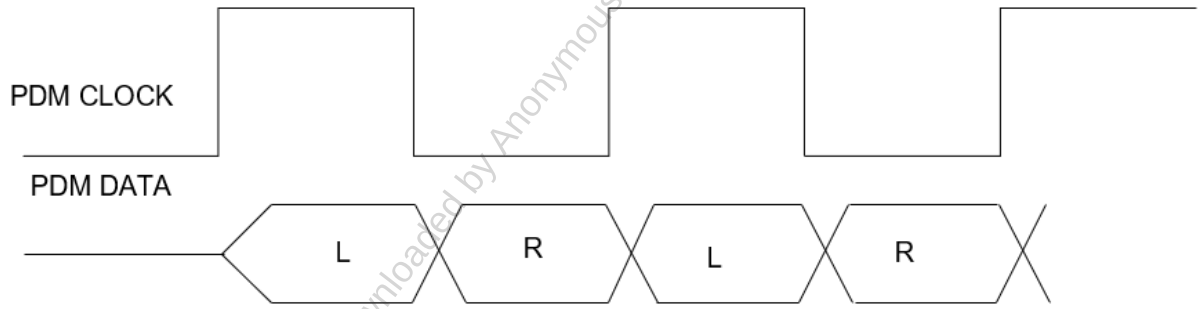

Figure 18. Astra Machina Half-Cycle PDM

2. References

- *Astra Machina Foundation Series Quick Start Guide* (PN: 511-001404-01)
- *Astra Machina SL1620 Developer Kit User Guide* (PN: 511-001407-01)
- *Astra Machina SL1640 Developer Kit User Guide* (PN: 511-001405-01)
- *Astra Machina SL1680 Developer Kit User Guide* (PN: 511-001403-01)
- *Astra Machina SL2610 Developer Kit User Guide* (PN: 505-001501-01)

3. Revision History

Revision	Description
A	Initial release.
B	Minor update to trademarked items.
C	Added SL2610 I2S, PDM information.
D	Updated Table 6. SL1640 Sampling Rate and Bit Clock Relationship (TDM)

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