Application Note

Astra™ Machina Foundation Series - Pulse Width Modulation

Abstract: This application note introduces the Pulse Width Modulation (PWM) functionality in the Astra™ Machina Foundation Series. It provides a basic overview of signal generation, control, and configuration for use with the SL1680, SL1640, and SL1620 embedded processors.

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1. Overview

The Astra™ Machina Foundation Series offers evaluation-ready kits that facilitate quick and straightforward prototyping with the Synaptics SL-Series of embedded Linux® and Android™ processors. Featuring a modular design, these kits include interchangeable core compute modules, a standard I/O board, and daughter cards for connectivity, debugging, and various I/O configurations. Additionally, the Astra Machina Foundation Series features PWM(x) technology.

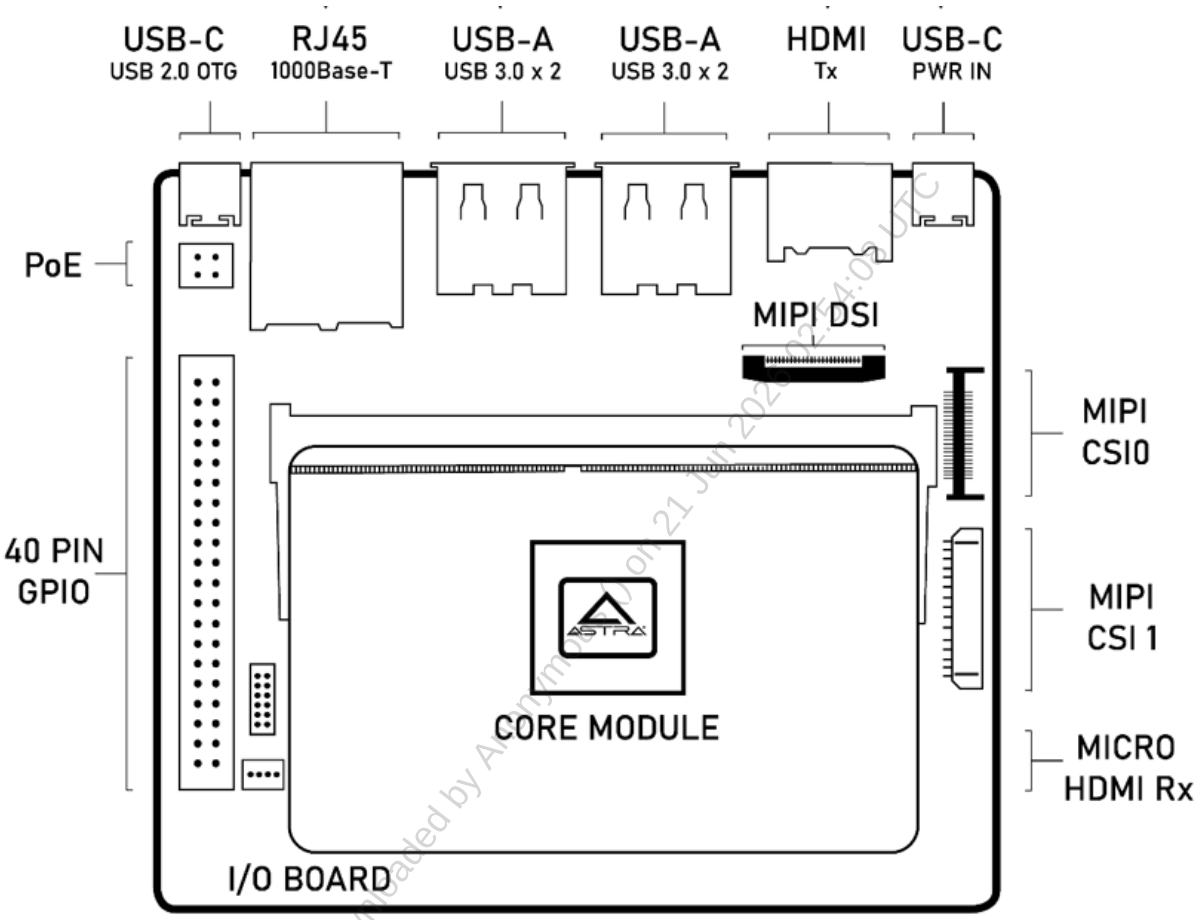


Figure 1. Astra Machina Foundation Series overview

2. PWM Introduction

The Pulse Width Modulator (PWM) allows for the generation of a high-resolution, periodic digital signal with customizable duty cycles to manage external devices. It includes four distinct channels, each of which can be configured independently, as demonstrated in Figure 2.

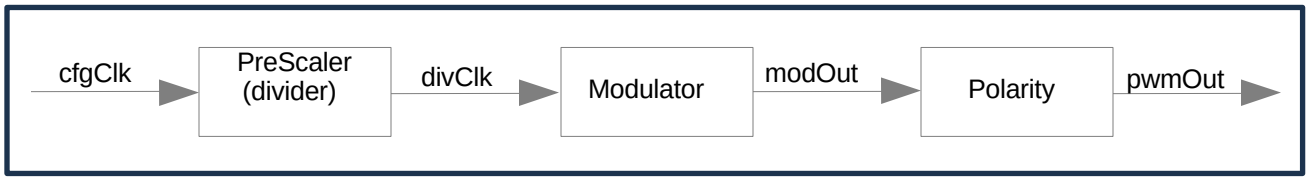
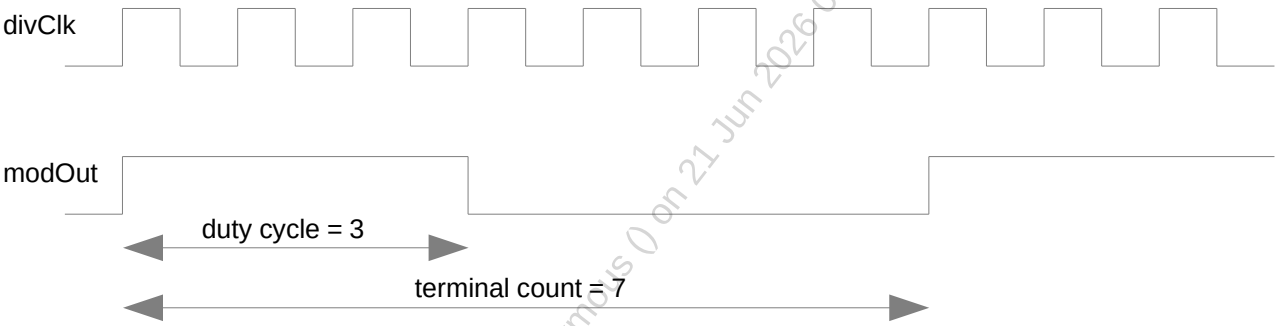


Figure 2. PWM block diagram

2.1. PWM Timing Diagram - Duty Cycle and Terminal Count Visualization



2.2. Functional Overview of PWM Signal Generative and Control

- cfgClk runs @100 MHz.
- The PreScaler module pre-divides the input clock if a longer periodic signal is needed.
- The counters reside within the Modulator block, meaning that they are clocked by divClk, not the original input cfgClk.
- Duty cycle is programmed via the pwmCh*Duty registers.
- Terminal count is programmed via the pwmCh*TCnt registers where TCOUNT = cfgClk/PWMfreq , PWMfreq. out.
- % Dutty cycle increment step = (PWMfreg / cfgClk)*100 where cfgClk = 100MHz
- If duty cycle is 0, modOut will always be low.
- If duty cycle is >= terminal count, modOut will always be high.
- modOut can be inverted by setting the polarity inversion register, pwmCh*Pol.
- Four distinct channels, each of which can be configured independently.

2.3. PWM(x) Base Address Register Information

Table 1. SL16xx Peripheral Base Address Register Memory Map

Base Address	Functional Name	Device SL16xx
0xF7F2_0000	PWM	SL1680
0xF7F2_0000	PWM	SL1640
0xF7F2_0000	PWM	SL1620

2.4. SL16(xx) PWM(x) Offset Address Register Information

Table 2. PWM Register Summary for all SL16(xx)

Offset	Name	Description
0x0000	PWM_pwmCh0En	PWM pwmCh0En
0x0004	PWM_pwmCh0Ctrl	PWM pwmCh0Ctrl
0x0008	PWM_pwmCh0Duty	PWM pwmCh0Duty
0x000C	PWM_pwmCh0TCnt	PWM pwmCh0TCnt
0x0010	PWM_pwmCh1En	PWM pwmCh1En
0x0014	PWM_pwmCh1Ctrl	PWM pwmCh1Ctrl
0x0018	PWM_pwmCh1Duty	PWM pwmCh1Duty
0x001C	PWM_pwmCh1TCnt	PWM pwmCh1TCnt
0x0020	PWM_pwmCh2En	PWM pwmCh2En
0x0024	PWM_pwmCh2Ctrl	PWM pwmCh2Ctrl
0x0028	PWM_pwmCh2Duty	PWM pwmCh2Duty
0x002C	PWM_pwmCh2TCnt	PWM pwmCh2TCnt
0x0030	PWM_pwmCh3En	PWM pwmCh3En
0x0034	PWM_pwmCh3Ctrl	PWM pwmCh3Ctrl
0x0038	PWM_pwmCh3Duty	PWM pwmCh3Duty
0x003C	PWM_pwmCh3TCnt	PWM pwmCh3TCnt
0x0040	PWM_pwmCh01Ctr	PWM pwmCh01Ctr
0x0044	PWM_pwmCh23Ctr	PWM pwmCh23Ctr

2.5. SL16(xx) PWM(x) Register Details

2.5.1. PWM pwmCh0En (PWM_pwmCh0En)

PWM Channel 0 Enable Register

Instance Name **Offset**

PWM_pwmCh0En 0x0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																																pwmCh0En
Default																																0

Bits	Name	Type	Reset	Description
0	pwmCh0En	R/W	0x0	1'b1: Enables PWM Channel 0 1'b0: Disables PWM Channel 0

2.5.2. PWM pwmCh0Ctrl (PWM_pwmCh0Ctrl)

PWM Channel 0 Control Register

Instance Name **Offset**

PWM_pwmCh0Ctrl 0x0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																													pwmCh0Pol	pwmCh0PreScale		
Default																													0	1	1	1

Bits	Name	Type	Reset	Description
2:0	pwmCh0PreScale	R/W	0x7	3'b000: Divide by 1 3'b001: Divide by 4 3'b010: Divide by 8 3'b011: Divide by 16 3'b100: Divide by 64 3'b101: Divide by 256 3'b110: Divide by 1024 3'b111: Divide by 4096 Default: 3'b111 to reduce power consumption when idle
3	pwmCh0Pol	R/W	0x0	1'b0: Non-inverted PWM output (Active High) 1'b1: Inverted PWM output (Active Low)

2.5.3. PWM pwmCh0Duty (PWM_pwmCh0Duty)

PWM Channel 0 Duty Cycle Register

Instance Name **Offset**

PWM_pwmCh0Duty 0x0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																	pwmCh0Duty															
Default																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Type	Reset	Description
15:0	pwmCh0Duty	R/W	0x2	Resets to 50% duty cycle based on Terminal Count of 4 Valid range = 0 to 65535 Boundary cases: 0 = pwmOut always inactive dutyCycle > tCnt = pwmOut always active

2.5.4. PWM pwmCh0TCnt (PWM_pwmCh0TCnt)

PWM Channel 0 Terminal Count Register

Instance Name **Offset**

PWM_pwmCh0TCnt 0x000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																	pwmCh0TCnt															
Default																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Type	Reset	Description
15:0	pwmCh0TCnt	R/W	0x4	Resets to 4 Valid range = 2 to 65535

2.5.5. PWM pwmCh1En (PWM_pwmCh1En)

PWM Channel 1 Enable Register

Instance Name **Offset**

PWM_pwmCh1En 0x0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																																pwmCh1En
Default																																0

Bits	Name	Type	Reset	Description
0	pwmCh1En	R/W	0x0	—

2.5.6. PWM pwmCh1Ctrl (PWM_pwmCh1Ctrl)

PWM Channel 1 Control Register

Instance Name **Offset**

PWM_pwmCh1Ctrl 0x0014

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																													pwmCh1Pol	pwmCh1PreScale		
Default																													0	1	1	1

Bits	Name	Type	Reset	Description
2:0	pwmCh1PreScale	R/W	0x7	—
3	pwmCh1Pol	R/W	0x0	—

2.5.7. PWM pwmCh1Duty (PWM_pwmCh1Duty)

PWM Channel 1 Duty Cycle Register

Instance Name **Offset**

PWM_pwmCh1Duty 0x0018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																	pwmCh1Duty															
Default																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Type	Reset	Description
15:0	pwmCh1Duty	R/W	0x2	—

2.5.8. PWM pwmCh1TCnt (PWM_pwmCh1TCnt)

PWM Channel 1 Terminal Count Register

Instance Name **Offset**

PWM_pwmCh1TCnt 0x001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																	pwmCh1TCnt															
Default																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Type	Reset	Description
15:0	pwmCh1TCnt	R/W	0x4	—

2.5.9. PWM pwmCh2En (PWM_pwmCh2En)

PWM Channel 2 Enable Register

Instance Name **Offset**

PWM_pwmCh2En 0x0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																																pwmCh2En
Default																																0

Bits	Name	Type	Reset	Description
0	pwmCh2En	R/W	0x0	—

2.5.10. PWM pwmCh2Ctrl (PWM_pwmCh2Ctrl)

PWM Channel 2 Control Register

Instance Name **Offset**

PWM_pwmCh2Ctrl 0x0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																													pwmCh2Pol	pwmCh2PreScale		
Default																													0	1	1	1

Bits	Name	Type	Reset	Description
2:0	pwmCh2PreScale	R/W	0x7	—
3	pwmCh2Pol	R/W	0x0	—

2.5.11. PWM pwmCh2Duty (PWM_pwmCh2Duty)

PWM Channel 2 Duty Cycle Register

Instance Name **Offset**

PWM_pwmCh2Duty 0x0028

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																	pwmCh2Duty															
Default																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Type	Reset	Description
15:0	pwmCh2Duty	R/W	0x2	—

2.5.12. PWM pwmCh2TCnt (PWM_pwmCh2TCnt)

PWM Channel 2 Terminal Count Register

Instance Name **Offset**

PWM_pwmCh2TCnt 0x002C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																	pwmCh2TCnt															
Default																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Type	Reset	Description
15:0	pwmCh2TCnt	R/W	0x4	—

2.5.13. PW—M pwmCh3En (PWM_pwmCh3En)

PWM Channel 3 Enable Register

Instance Name **Offset**

PWM_pwmCh3En 0x0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																																pwmCh3En
Default																																0

Bits	Name	Type	Reset	Description
0	pwmCh3En	R/W	0x0	—

2.5.14. PWM pwmCh3Ctrl (PWM_pwmCh3Ctrl)

PWM Channel 3 Control Register

Instance Name **Offset**

PWM_pwmCh3Ctrl 0x0034

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																													pwmCh3Pol	pwmCh3PreScale		
Default																													0	1	1	1

Bits	Name	Type	Reset	Description
2:0	pwmCh3PreScale	R/W	0x7	—
3	pwmCh3Pol	R/W	0x0	—

2.5.15. PWM pwmCh3Duty (PWM_pwmCh3Duty)

PWM Channel 3 Duty Cycle Register

Instance Name **Offset**

PWM_pwmCh3Duty 0x0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																	pwmCh3Duty															
Default																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Type	Reset	Description
15:0	pwmCh3Duty	R/W	0x2	—

2.5.16. PWM pwmCh3TCnt (PWM_pwmCh3TCnt)

PWM Channel 3 Terminal Count Register

Instance Name **Offset**

PWM_pwmCh3TCnt 0x003C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field																	pwmCh3TCnt															
Default																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Type	Reset	Description
15:0	pwmCh3TCnt	R/W	0x4	—

2.5.17. PWM pwmCh01Ctr (PWM_pwmCh01Ctr)

PWM Channel 0 and 1 Read-only Current Counter Value

Instance Name **Offset**

PWM_pwmCh01Ctr 0x0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	pwmCh1Ctr																pwmCh0Ctr															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Type	Reset	Description
15:0	pwmCh0Ctr	R	0x	—
31:16	pwmCh1Ctr	R	0x	—

2.5.18. PWM pwmCh23Ctr (PWM_pwmCh23Ctr)

PWM Channel 2 and 3 Read-only Current Counter Value

Instance Name **Offset**

PWM_pwmCh23Ctr 0x0044

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	pwmCh3Ctr																pwmCh2Ctr															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Type	Reset	Description
15:0	pwmCh2Ctr	R	0x	—
31:16	pwmCh3Ctr	R	0x	—

3. SL16(xx) PWM Pinmux

3.1. SL1680 – PWM Pinmux

Table 3. SL1680 Pinmux

Ball #	Mode 2	Mode 3	Mode 4
AG59	—	PWM[2]	—
AB60	—	PWM[3]	—
AP59	PWM[0]	—	—
AP60	PWM[1]	—	—
AR51	PWM[2]	—	—
AR53	PWM[3]	—	—
AT59	—	PWM[0]	—
AY59	—	PWM[1]	—
F59	—	—	PWM[1]
K60	—	—	PWM[0]
R57	PWM[0]	—	—
R55	PWM[1]	—	—
P59	PWM[2]	—	—
P60	PWM[3]	—	—
BH61	PWM[2]	—	—
BF59	PWM[3]	—	—
BG55	PWM[0]	—	—
BH60	PWM[1]	—	—

3.2. SL1640 – PWM Pinmux

Table 4. SL1640 Pinmux

Ball #	Mode 2	Mode 3	Mode 4
AC32	—	PWM[2]	—
AD31	—	PWM[3]	—
AH32	PWM[0]	—	—
AC26	PWM[1]	—	—
AH31	PWM[2]	—	—
AJ31	PWM[3]	—	—
AK32	—	PWM[0]	—
AL30	—	PWM[1]	—
A10	—	—	PWM[1]
B13	—	—	PWM[0]
B8	PWM[0]	—	—
A8	PWM[1]	—	—
C10	PWM[2]	—	—
C11	PWM[3]	—	—
AL11	PWM[2]	—	—
AK13	PWM[3]	—	—
AK11	PWM[0]	—	—
AM10	PWM[1]	—	—

3.3. SL1620 – PWM Pinmux

Table 5. SL1620 Pinmux

Ball #	Mode 1	Mode 2
A23	PWM[0]	—
B23	PWM[1]	—
B24	PWM[2]	—
A25	PWM[3]	—
F23	—	PWM[1]
D25	—	PWM[2]

4. Example SL1620 PWM[0]

This section provides an example of generating PWM0 at 1MHz with 50% duty cycle.

4.1. General Information – Calculation

Calculate or use the given values:

- cfgClk runs @100 MHz.
- Duty cycle is programmed via the pwmCh*Duty registers.
- Terminal count is programmed via the pwmCh*TCnt registers where TCOUNT = cfgClk/PWMfreq , and PWMfreq. Output = 1MHz
  TCOUNT = 100MHz / 1MHz = 100 Decimal (0x64 Hex)
- % Duty cycle increment step = (PWMfreg / cfgClk)*100 where cfgClk = 100MHz
  (1MHz / 100MHz) * 100 = 1% Duty cycle increment step.
  PWM 1MHz @ 50% Duty Cycle = TCOUNT * 50% = 100 * 50% = 50 Dec (0x32 Hex)
- If duty cycle is 0, modOut will always be low.
- If duty cycle is >= terminal count, modOut will always be high.
- modOut can be inverted by setting the polarity inversion register, pwmCh*Pol.

4.2. Program Steps for PWM[0] = 1MHz @50% Duty Cycle

a. Set GPIO 46 pin output value to 0 (Optional to initial the output to low signal output @pin A23)
   Reg: 0xF7E80C00
   Bit: 14
   Write Value: 0x0

b. Set GPIO 46 pin direction, Input: 0, Output: 1 (Optional step)
   Reg: 0xF7E80C04
   Bit: 14
   Write Value: 0x1

c. PWM0 enable/dis-enable. Make sure that PWM[0] is disable.
   Reg: 0xF7F20000
   Bit: 0
   Write Value: 0x0

d. Set PWM0 pin pinmux
   Reg: 0xF7EA8008
   Bit: [23:21]
   Write Value: 0x1

e. Set PWM0 Prescal & Polarity
   Reg: 0xF7F20004
   Bit: [2:0]
   Write Value: 0x0 (divided by 1)
   Bit; [3] Polarity
   Write Value: 0x0 (None invert)

f. Set PWM[0] @50% Duty Cycle Value
   Reg: 0xF7F20008
   Bit: [15:0]
   Write Value: 0x32

g. Set PWM[0] TCOUNT
   Reg: 0xF7F2000C
   Bit: [15:0]
   Write Value: 0x64

h. PWM0 is enable
   Reg: 0xF7F20000
   Bit: 0
   Write Value: 0x1

5. References

- *Astra Machina Foundation Series Quick Start Guide* (PN: 511-001404-01)
- *Astra Machina SL1640 Developer Kit User Guide* (PN: 511-001405-01)
- *Astra Machina SL1620 Developer Kit User Guide* (PN: 511-001407-01)
- *Astra Machina SL1680 Developer Kit User Guide* (PN: 511-001403-01)

6. Revision History

Revision	Description
A	Initial release.
B	Added sections 3 SL16(xx) PWM Pinmux and 4 Example SL1620 PWM[0].
C	Minor update to latest template and fixed trademark typo.

PN: 506-001526-01 Rev C