SR100 Series Family Datasheet

High-Performance Context-Aware AI MCUs

Description

The Synaptics Astra™ SR100 Series of AI MCUs is designed to deliver high-performance, AI-Native, multimodal compute to consumer, enterprise, and industrial Internet of Things (IoT) workloads. Based on Arm® Cortex®-M55 cores with Helium™ technology and Arm Ethos™-U55 neural network processors (NPU), the MCUs feature multiple tiers of operation—performance, efficiency, low-power (LP) sensing, and always-on (AON)—that algorithmically deliver intelligence at every power level, to enable a new class of context-aware IoT devices. The AI-Native SR100 Series supports a rich set of peripherals and accelerators, including dual MIPI camera interfaces, image processing with encode and pre-roll, motion and voice activity detection engines, and industry-standard security. These features make it well-suited for streaming vision and audio processing applications at the IoT device edge.

The SR100 Series is a high-performance, ultra-low power, and small footprint Audio and Vision AI processor family.

The main applications of the SR100 Series are:

- Battery-operated security cameras
- Industrial control systems
- AI-enhanced smart home appliances
- Wearables, fitness monitors, privacy sensors

The SR100 Series processing power is based on a combination of two processors and two NN hardware accelerators and equipped with the relevant interfaces to communicate with other devices in the system, such as the application processor (AP), camera sensors, digital microphones, and other sensors.

The SR100 Series offers a combination of:

- Ultra-low power (ULP) architecture that includes multiple power modes by implementing both clock gating and power switching
- Rich set of peripherals
- Small form factor that can fit into thin laptop camera modules, small IoT cameras and mobile devices.
- Self-contained operation as IoT processor or simple interface to strong AP
- Multiple camera interfaces
- Two PDM interfaces that can handle up to four digital microphones
- Two processors
- Two neural network (NN) accelerators
- Low power image processing and motion detection hardware accelerator

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1. Block Diagram

Figure 1 depicts the high-level diagram of the SR100 Series.

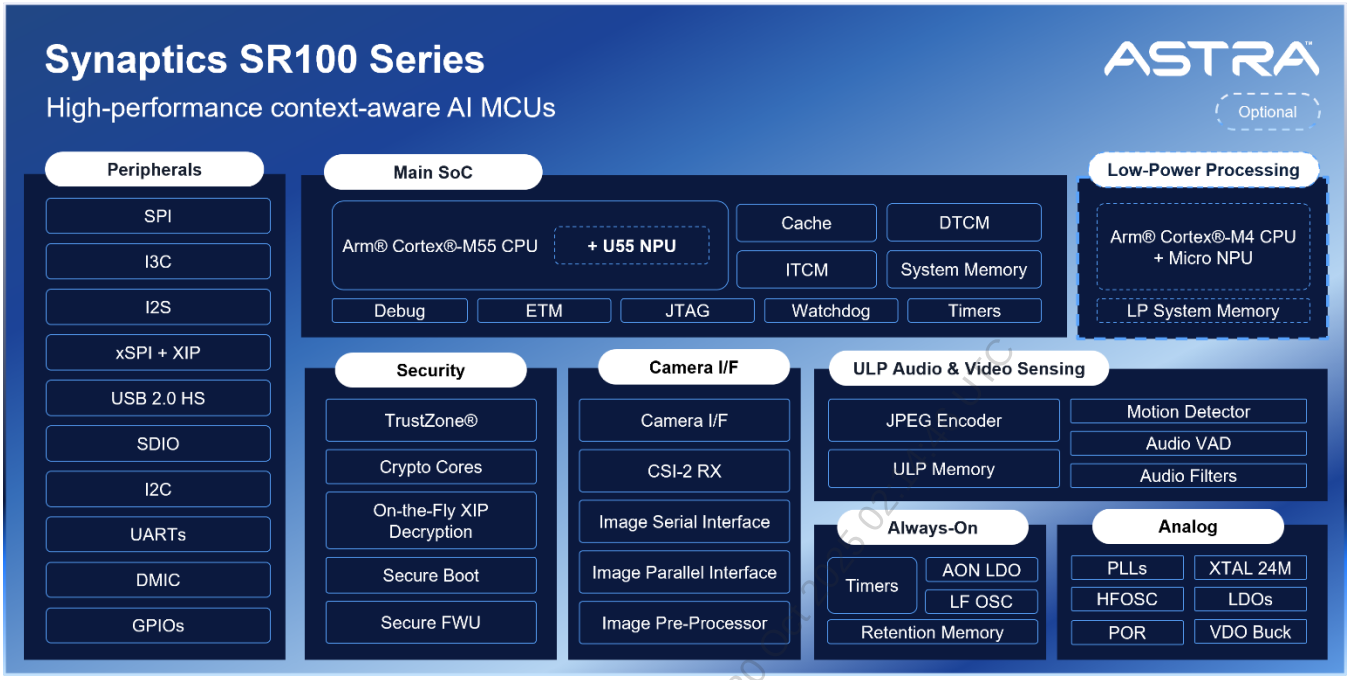


Figure 1. SR100 Series block diagram

There are three groups of connections:

- **Communication**
  - xSPI Host interface for booting from QSPI serial Flash
  - I3C/I2C Target for two wire Host connectivity
  - USB 2.0 HS for:
    - meta data and audio stream to external Host processor
    - bridge control for signal aggregation
    - FW upgrade
  - SPI Target for boot and control
  - UART for debug and boot
  - SDIO connection
- **Sensing interfaces**
  - Camera Inputs:
    - 2x MIPI CSI-2 receivers
    - SPI DVI serial input low resolution video stream
    - DVP (Digital Video Parallel) input for low resolution video stream
  - **Camera output**:
    - MIPI CSI-2 transmitter. Images can be bypassed from CSI input to CSI output, or aggregation of two CSI-2 inputs to the CSI-2 output.

  - **Audio sense:**
    - Two PDM interfaces connected to 1-4 digital microphones
    - I2S for external Codec or Class-D amplifier output
    - Audio input from up to four digital microphones for VT events, Key-word detection or for general purpose voice input
  - **Audio Mute and Camera Mute:**
    - Dedicated HW pins to block either audio and/or camera out to Host
- **Power**
  - 3V3 and 1V8 power inputs, or alternatively single battery input for 2.97V-3.63V
  - High efficiency buck regulators to generate VDD from VBAT and feed the digital logic
  - LDOs to generate 1V8 and 0V8
  - PMU_EN pin to turn-on the PMU

1.1. Features

1.1.1. Processing Power

- Main processor: Arm® Cortex®-M55 CPU
  - Clock frequency: Up to 400 MHz
  - 32 kB of instruction cache
  - 32 kB of data cache
  - 128 kB of ITCM memory and 128 kB of DTCM memory
  - Arm CoreSight™ debugging interface
  - TrustZone®
  - Support standard tool chains
- LP processor: Arm® Cortex®-M4 CPU
  - Clock frequency: Up to 100 MHz
  - 4 kB of cache
- Main NN processor: Arm Ethos™-U55 micro NPU core
  - Clock frequency: Up to 400 MHz
  - 128 MACs/cycle
  - 24 kB of memory
- LP NN processor: Synaptics propriety NPU
  - Clock frequency: Up to 100 MHz
  - Automatic cache pre-fetch with zero miss-penalty

1.1.2. Memory

- Up to 3008 kB of system memory, including 1448 kB of LP system memory
- 630 kB of ULP audio and video sense memory
- All memories can be completely turned off, LP system memory and ULP memory can be retained
- Ultra-low power 16 kB AON memory

1.1.3. Sensing Interfaces

- MIPI CSI-2 camera input and output
  - 2 x Two lanes MIPI CSI-2® RX interfaces with max bandwidth of 1.5 Gb/Sec
  - One MIPI CSI-2 TX interface with max BW of 1.5 Gb/Sec
  - Support up to resolution of 3840x2160(4K)
  - MIPI Aggregation mode joining two camera input streams to single output stream
- Digital camera input support
  - Serial video interface with max bandwidth of 73 Mb/Sec input
  - Parallel video interface input with max bandwidth of 147 Mb/Sec
  - Support input resolution of up to VGA@60fps (QFHD@30fps)
- Audio Interfaces
  - I2S interface
  - 2 x 2-channel PDM
  - PDM output bypass interface to the external HOST
  - MIPI SoundWire® Target interface
- Audio and Video LP sense processing
  - Format conversion
  - Motion detection
  - De-mosaic and White Balancing
  - Image crop and resize
  - JPEG encoder
  - Automatic HWVAD with history buffer
  - Frames buffer
  - Frame statistics calculation (Virtual ALS)

1.1.4. Security

- Arm TrustZone
- Secure boot
- TRNG
- Secure OTP AES-256
- RSA-4096
- SHA-512

1.1.5. Rich Peripherals Set

- Three I2C interfaces
  - I2C Target interface
  - Two I2C Host interfaces
- I3C Host interface
- I3C Target interface
- Two UARTs
- SPI Host interface
- Two SPI Target interfaces (one used for boot)
- Two SDIO interfaces
- 4/8 bits 133 MHz 'xSPI' Host interface (support boot from serial memory and XIP)
- Watchdog

- Eight timers
- Up to 43 general-purpose 1.8V input/outputs (GPIOs)
- USB 2.0 HS (480 Mb/s) with USB audio class support.
- LP Processor Peripherals
  - Dedicated UART
  - Dedicated GPIOs

1.1.6. Boot Interfaces

- Protected Boot from QSPI flash or via Host interfaces: I2C, SPI, UART and I3C

1.1.7. Clock and Reset

- 24 MHz XTAL
- 32 kHz LP clock input
- Digital input reset
- Two Internal RC oscillators
  - 24 MHz trimmed RC oscillator
  - Ultra-low power 32 kHz oscillator for AON
- Three high speed PLLs for the USB, CSI-2, and System

1.1.8. Power Management

- Can be powered from 3.3V & 1.8V external sources or from single 2.97V-3.63V battery supply.
- On chip Buck regulator and LDO supplies.
- Low-power modes: active (sub-100 mW), low-power (sub-10 mW), ULP AON (sub-100 uW) and power-down mode.
- Power-enabled pin powers up the device from complete power down and can be controlled from an external GPIO or button.
- Battery voltage monitor.
- AON power island that stays on during low-power mode, while all other SR100 Series logic and memories are off. The AON can wakeup SR100 Series from external GPIO interrupts and timer events; During low-power mode, recovery information is stored in the ULP AON memory.

1.1.9. Packaging

- 84-balls WLCSP, 0.4 mm pitch, 5.2 mm x 2.7 mm
- 122-balls FCCSP, 0.386 mm pitch, 7 mm x 4.5 mm

Table 1. SR100 Series Chipset Feature Summary

Feature	SR100 Series WLCSP	SR100 Series FCCSP
Package	84-balls WLCSP, 0.4 mm pitch, 5.2 mm x 2.7 mm	122-balls FCCSP, 0.386 mm pitch, 7 mm x 4.5 mm
Application Processor	Arm® Cortex®-M55 with Helium™ at up to 400 MHz	
Coprocessors	Arm Cortex-M4 Low-power processor at up to 100 MHz	
NN Processor	Ethos-U55 micro NPU core at up to 400 MHz	
NN Co-processors	Synaptics ULP NN proprietary processor at up to 100 MHz	
Camera sensing interfaces	Single MIPI CSI-2 RX with max BW of 1.5 GHz	Two MIPI CSI-2 RX with max BW of 1.5 GHz
	Parallel camera interface 1 bit	Parallel camera interface 1, 4, 8 bit
	Serial Camera interface	
Camera output interface	Single MIPI CSI-2 TX with max BM of 1.5 GHz	
Security Hardware Accelerators	✓	
xSPI	4-bits	8-bits
USB	High-Speed USB 2.0 MAC+PHY Device controller	
SDIO 2.0	x	Two 1/4-bits SDIO interfaces
TDM/I2S	1	
SoundWire Target interface	1	
Digital microphones	Two PDM interfaces with support of up to four digital microphones	
SPI Host	1	
UART	3	
I2C Host	2	
I2C Target	1	
I3C Host	1	
I3C Target	1	
Clock inputs	24 MHz XTAL	24 MHz XTAL, 32K digital input
GPIOs	27	43

2. Ball Description

2.1. SR100 Series WLCSP Ball-out

Note: All figures in this section refer to the top-view.

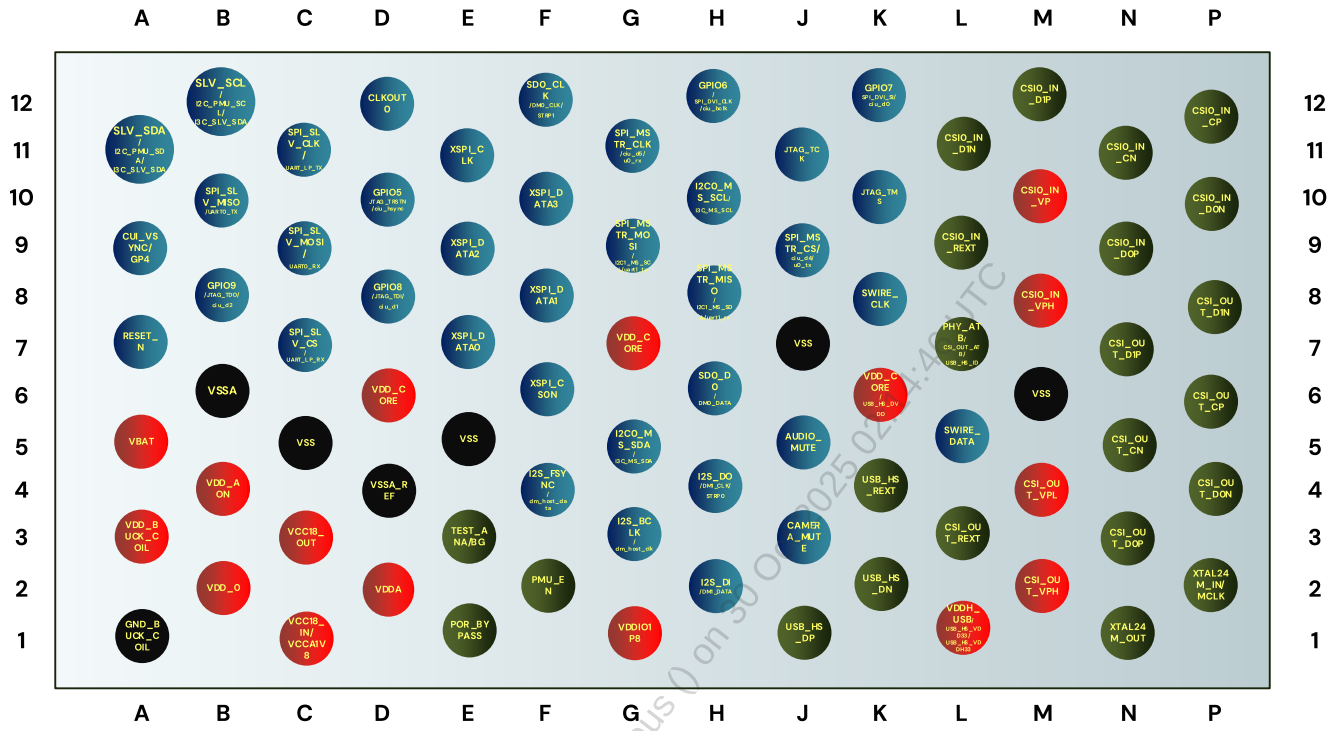


Figure 2. SR100 Series WLCSP top view

2.2. SR100 Series FCCSP Ball-out

Note: All figures in this section refer to the top-view.

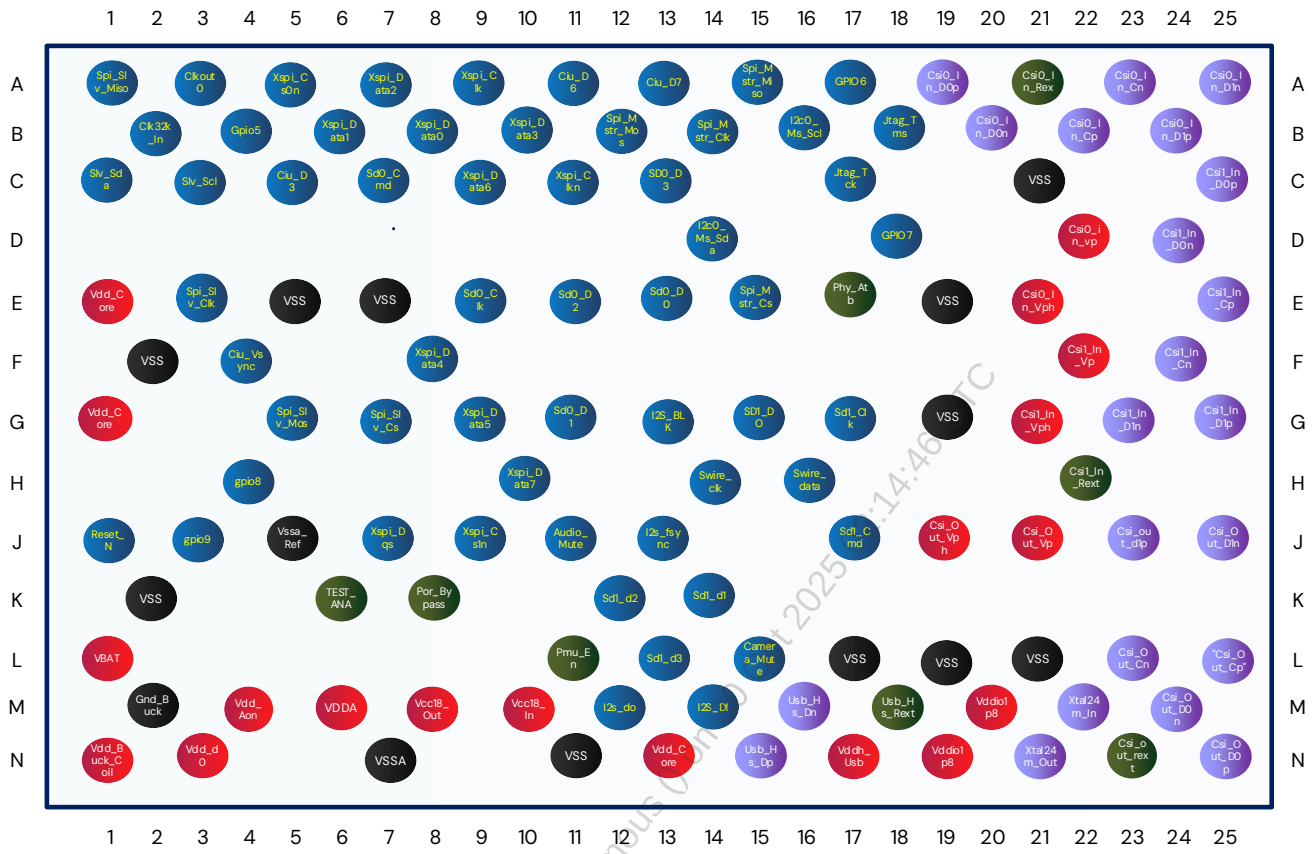


Figure 3. SR100 Series FCCSP top view

2.3. Signal List

Table 3 presents the functionality of all operational balls. Most of the digital I/O balls can be configured for more than one function. The list does not include testing functions (enabled when TEST is high).

Table 2. Pin Type Abbreviations

Pin Type	Definitions
Direction Column	
I	Input only
O	Output only
I/O	Input and output
P	Power / Ground
PI	Power Input
PO	Power Output
Type Column	
A	Analog
D	Digital
Diff	Differential
Pwr	Power

Table 3. Signal Descriptions

Signal Name	Count	Direction	Type	Description
MIPI CSI-2 RX				
CSI0_IN_CN	1	I	Diff	MIPI RX0 clock negative input.
CSI0_IN_CP	1	I	Diff	MIPI RX0 clock positive input
CSI0_IN_D0N	1	I	Diff	MIPI RX0 data lane 0 negative input.
CSI0_IN_D0P	1	I	Diff	MIPI RX0 data lane 0 positive input.
CSI0_IN_D1N	1	I	Diff	MIPI RX0 data lane 1 negative input.
CSI0_IN_D1P	1	I	Diff	MIPI RX0 data lane 1 positive input.
CSI0_IN_REXT	1	I	Diff	CSI RX 200Ω ±1% reference resistor
CSI1_IN_CN	1	I	Diff	MIPI RX1 clock negative input.
CSI1_IN_CP	1	I	Diff	MIPI RX1 clock positive input
CSI1_IN_D0N	1	I	Diff	MIPI RX1 data lane 0 negative input.
CSI1_IN_D0P	1	I	Diff	MIPI RX1 data lane 0 positive input.
CSI1_IN_D1N	1	I	Diff	MIPI RX1 data lane 1 negative input.
CSI1_IN_D1P	1	I	Diff	MIPI RX1 data lane 1 positive input.
CSI1_IN_REXT	1	I	Diff	CSI RX 200Ω ±1% reference resistor

Signal Name	Count	Direction	Type	Description
MIPI CSI-2 TX				
CSI_OUT_CN	1	O	Diff	MIPI TX clock negative output.
CSI_OUT_CP	1	O	Diff	MIPI TX clock positive output
CSI_OUT_D0N	1	O	Diff	MIPI TX data lane 0 negative output.
CSI_OUT_D0P	1	O	Diff	MIPI TX data lane 0 positive output.
CSI_OUT_D1N	1	O	Diff	MIPI TX data lane 1 negative output.
CSI_OUT_D1P	1	O	Diff	MIPI TX data lane 1 positive output.
CSI_OUT_REXT	1	I	A	CSI TX 200Ω ±1% reference resistor
USB 2.0 HS				
USB_HS_DN	1	I/O	Diff	USB Data Negative Signal
USB_HS_DP	1	I/O	Diff	USB Data Positive Signal
USB_HS_REXT	1	I	A	USB 200Ω ±1% reference resistor
Mute Signals				
CAMERA_MUTE	1	I	D	Camera mute control signal
AUDIO_MUTE	1	I	D	Microphone mute control signal
SDIO Controller 0				
SD0_D[3:0]	4	I/O	D	SDMMC Data
SD0_CLK	1	O	D	SDMMC Clock
SD0_CMD	1	I/O	D	SDMMC Command
SD0_WR_PROT	1	I	D	SDMMC Write Protect
SD0_DETECT	1	I	D	SDMMC Detect
SDIO Controller 1				
SD1_D[3:0]	4	I/O	D	SDMMC Data
SD1_CLK	1	O	D	SDMMC Clock
SD1_CMD	1	I/O	D	SDMMC Command
UART0				
UART0_TX	1	O	D	UART0 Serial Data Output
UART0_RX	1	I	D	UART0 Serial Data Input
UART0_RTS	1	O	D	UART0 Ready To Send
UART0_CTS	1	I	D	UART0 Clear To Send
UART1				
UART1_TX	1	O	D	UART1 Serial Data Output
UART1_RX	1	I	D	UART1 Serial Data Input
UARTLP				
UART_LP_TX	1	O	D	LP PROC UART Serial Data Output
UART_LP_RX	1	I	D	LP PROC UART Serial Data Input
I2S/TDM				
I2S_BCLK	1	I/O	D	TDM/I2S SCLK
I2S_FSYNC	1	I/O	D	TDM/I2S Frame Sync

Signal Name	Count	Direction	Type	Description
I2S_DO	1	O	D	TDM/I2S TX Data
I2S_DI	1	I	D	TDM/I2S RX Data
Digital Microphones				
DM0_CLK	1	I/O	D	Digital microphone 0 clock signal
DM0_DATA	1	I	D	Digital microphone 0 data
DM1_CLK	1	I/O	D	Digital microphone 1 clock signal
DM1_DATA	1	I	D	Digital microphone 1 data
DM_HOST_CLK	1	I	D	Digital microphone Host clock input
DM_HOST_DATA	1	O	D	Digital microphone Host data output
I2C Target				
I2C_SLV_SCL	1	Open Drain	D	I2C Target Clock
I2C_SLV_SDA	1	Open Drain	D	I2C Target Data
I2C Host				
I2C0_MS_SCL	1	Open Drain	D	I2C0 Host Clock
I2C0_MS_SDA	1	Open Drain	D	I2C0 Host Data
I2C1_MS_SCL	1	Open Drain	D	I2C1 Host Clock
I2C1_MS_SDA	1	Open Drain	D	I2C1 Host Data
I3C Target				
I3C_SLV_SCL	1	I	D	I3C Target Clock
I3C_SLV_SDA	1	I/O	D	I3C Target Data
I3C Host				
I3C_MS_SCL	1	O	D	I3C Host Clock
I3C_MS_SDA	1	I/O	D	I3C Host Data
SPI Target				
SPI_SLV_MISO	1	O	D	SPI Target Serial Data Out
SPI_SLV_MOSI	1	I	D	SPI Target Serial Data In
SPI_SLV_CS	2	O	D	SPI Target Chip Selects
SPI_SLV_CLK	1	O	D	SPI Target Clock
SPI Host				
SPI_MSTR_MOSI	1	O	D	SPI Host Serial Data Out
SPI_MSTR_MISO	1	I	D	SPI Host Serial Data In
SPI_MSTR_CS	1	I	D	SPI Host Chip Select
SPI_MSTR_CLK	1	O	D	SPI Host Clock
GPIO				
GPIO[10:0],[32:13],[47:34]	30	I/O	D	General Purpose I/O Port A
Camera Digital Interfaces				
CIU_D[7:0]	8	I	D	Camera Interface Unit data input signals
CIU_VSYNC	1	I	D	Camera Interface Unit data vertical sync signal
CIU_HSYNC	1	I	D	Camera Interface Unit data horizontal sync signal

Signal Name	Count	Direction	Type	Description
CIU_BCLK	1	I	D	Camera Interface Unit bit clock signal
SPI_DVI_CLK	1	I	D	SPI Camera Interface clock signal
SPI_DVI_SI	1	O	D	SPI Camera Interface data signal
xSPI Host				
XSPI_DATA[7:0]	8	I/O	D	xSPI data signals
XSPI_CS[1:0]	2	O	D	xSPI Chip Selects signals
XSPI_CLK	1	O	D/Diff	xSPI Clock positive signal
XSPI_CLKN	1	O	Diff	xSPI Clock negative signal
XSPI_DQS	1	I	D	xSPI data strobe signal
SoundWire				
SWIRE_CLK	1	I	D	SoundWire Clock Input to Microphone
SWIRE_DATA	1	I/O	D	SoundWire Bi-directional Data Signal
Clocks and Crystals				
CLK32K_IN	1	I	D	Optional 32K digital clock input to the AON
CLKOUT[1:0]	2	O	D	Digital Clock Output
XTAL24M_IN	1	I	A	24 MHz Crystal Input or External Clock Input
XTAL24M_OUT	1	O	A	24 MHz Crystal Feedback
JTAG and TEST				
TDO	1	O	D	CPU JTAG Data Out
TMS	1	I	D	CPU JTAG Mode Select
TDI	1	I	D	CPU JTAG Data In
TCK	1	I	D	CPU JTAG Clock
TRST	1	I	D	CPU JTAG Reset
SWCLK	1	I	D	CPU 2-pins JTAG Clock input signal
SWD	1	I/O	D	CPU 2-pins JTAG bidirectional Data signal
TRACE_DATA[3:0]	4	O	D	ARM Trace bus data signals
TRACE_CLK	1	O	D	ARM Trace bus clock signal
TEST_ANA/BG	1	I/O	A	Analog test mux output and BG output
PHY_ATB	1	O	A	CSI and USB analog test mux output
POR_BYPASS	1	I	A	POR circuit bypass
Digital Power Supplies				
VBAT	1	PI	Pwr	Battery or 3V3 power input
VDD_BUCK_COIL	1	PI	Pwr	VDD Buck regulator output
GND_BUCK	1	PI	Pwr	Buck regulator Ground
VSS	4	PI	Pwr	Digital Ground
VSSA	1	PI	Pwr	Analog Ground
VSSA_REF	1	PI	Pwr	Bandgap analog ground
VDD_0	1	PI	Pwr	0.8V buck regulator FB pin
VDD_CORE	3	PI	Pwr	0.8 V Core input

Signal Name	Count	Direction	Type	Description
VDDIO1V8	1	PI	Pwr	1V8 Supply to the I/Os
VDD_AON	1	PI/O	Pwr	AON LDO Output
CSI[1:0]_IN_VP	2	PI	Pwr	CSI Receive Digital 0.8V input
CSI[1:0]_IN_VPH	1	PI	Pwr	CSI Receive Analog 1.8V input
CSI_OUT_VP	1	PI	Pwr	CSI Transmit Digital 0.8V output
CSI_OUT_VPH	1	PI	Pwr	CSI Transmit Analog 1.8V output
VCCA	1	PI	Pwr	1V8 Analog input
VDDA	1	PI/O	Pwr	0V8 Analog LDO output/input
VDDH_USB	1	PI	Pwr	USB2 3V3 Analog Supply
VCC18_OUT	1	PO	Pwr	1V8 Analog LDO output
VCC18_IN	1	PI	Pwr	1V8 input
Straps				
TEST	1	I	D	Test strap pin
STRAP[1:0]	2	I	D	BOOT Select straps

3. Pin Multiplexing

3.1. Pin Multiplexing Modes

This section describes the various modes related to the multiplexed pins. The primary pin name reflects the pinout name, while the Mode 0, Mode 1, ..., Mode 4 and Strap multiplex names are located in the respective columns.

Figure 4 shows the multiplexed pin naming scheme that is used for the Multiplexed pins.

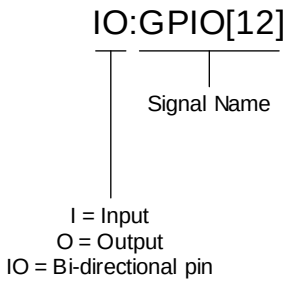


Figure 4. Example of the Multiplexed Pin Naming Scheme

3.2. Pin Multiplexing Signal Descriptions

Table 4. Ball Assignment

Ball Name	SR100 Series FCCSP Ball No.	SR100 Series WLCSP Ball No.	ALT 0 (Default)	ALT 1	ALT 2	ALT 3	ALT4	ALT5	Strap	PUboot/ PDboot[2]	AON
AUDIO_MUTE	J11	J5	I:AUDIO_MUTE	—	—	—	—	—	—	PD	—
CAMERA_MUTE	L15	J3	I:CAMERA_MUTE	—	—	—	—	—	—	PD	—
CIU_D3	C5	N/A	IO:GPIO10	I:CIU_D3	O:CLKOUT1	IO:DMO_CLK_D	—	O:AON_CLKOUT1	—	—	AON
CIU_D6	A11	N/A	IO:GPIO13	I:CIU_D6	IO:DMO_CLK_B	O:UART1_TX_B	—	—	—	—	—
CIU_D7	A13	N/A	IO:GPIO14	I:CIU_D7	I:DMO_DATA_B	I:UART1_RX_B	—	—	—	—	—
CIU_VSYNC	F4	A9	IO:GPIO4	I:CIU_VSYNC	—	I:UART0_CTS	—	I:AON_GPI3	—	—	AON
CLK32K_IN	B2	N/A	IO:GPIO40	I:CLK32K_IN	—	—	—	—	—	—	—
CLKOUT0	A3	D12	IO:GPIO41	O:CLKOUT0	—	—	—	O:AON_CAMERA_CLK	—	—	AON
CSI_OUT_CN	L23	N5	—	—	—	—	—	—	—	—	—
CSI_OUT_CP	L25	P6	—	—	—	—	—	—	—	—	—
CSI_OUT_D0N	M24	P4	—	—	—	—	—	—	—	—	—
CSI_OUT_D0P	N25	N3	—	—	—	—	—	—	—	—	—
CSI_OUT_D1N	J25	P8	—	—	—	—	—	—	—	—	—
CSI_OUT_D1P	J23	N7	—	—	—	—	—	—	—	—	—
CSI_OUT_REXT	N23	L3	—	—	—	—	—	—	—	—	—
CSI_OUT_VP	J21	M4	—	—	—	—	—	—	—	—	—
CSI_OUT_VPH	J19	M2	—	—	—	—	—	—	—	—	—
CSI0_IN_CN	A23	N11	—	—	—	—	—	—	—	—	—
CSI0_IN_CP	B22	P12	—	—	—	—	—	—	—	—	—
CSI0_IN_D0N	B20	P10	—	—	—	—	—	—	—	—	—
CSI0_IN_D0P	A19	N9	—	—	—	—	—	—	—	—	—
CSI0_IN_D1N	A25	L11	—	—	—	—	—	—	—	—	—
CSI0_IN_D1P	B24	M12	—	—	—	—	—	—	—	—	—
CSI0_IN_REXT	A21	L9	—	—	—	—	—	—	—	—	—

Ball Name	SR100 Series FCCSP Ball No.	SR100 Series WLCSP Ball No.	ALT 0 (Default)	ALT 1	ALT 2	ALT 3	ALT4	ALT5	Strap	PUboot/ PDboot[2]	AON
CSI0_IN_VP	D22	M10	—	—	—	—	—	—	—	—	—
CSI0_IN_VPH	E21	M8	—	—	—	—	—	—	—	—	—
CSI1_IN_CN	F24	N/A	—	—	—	—	—	—	—	—	—
CSI1_IN_CP	E25	N/A	—	—	—	—	—	—	—	—	—
CSI1_IN_D0N	D24	N/A	—	—	—	—	—	—	—	—	—
CSI1_IN_D0P	C25	N/A	—	—	—	—	—	—	—	—	—
CSI1_IN_D1N	G23	N/A	—	—	—	—	—	—	—	—	—
CSI1_IN_D1P	G25	N/A	—	—	—	—	—	—	—	—	—
CSI1_IN_REXT	H22	N/A	—	—	—	—	—	—	—	—	—
CSI1_IN_VP	F22	N/A	—	—	—	—	—	—	—	—	—
CSI1_IN_VPH	G21	N/A	—	—	—	—	—	—	—	—	—
GPIO5	B4	D10	I:JTAG_TRSTN_A	I:CIU_HSYNC	IO:GPIO5	O:UART0_RTS	—	I:AON_GPI2	—	—	AON
GPIO6	A17	H12	IO:GPIO6	I:CIU_BCLK	I:SPI_DVI_CLK	I:SPI_SLV_CLK_B	—	—	—	—	—
GPIO7	D18	K12	IO:GPIO7	I:CIU_D0	I:SPI_DVI_SI	I:SPI_SLV_MOSI_B	—	—	—	—	—
GPIO8	H4	D8	I:JTAG_TDI_A	I:CIU_D1	IO:GPIO8	I:SPI_SLV_CS_B	—	O:AON_GPO2	—	—	AON[1]
GPIO9	J3	B8	IO:JTAG_TDO_A	I:CIU_D2	IO:GPIO9	IO:SPI_SLV_MISO_B	—	O:AON_CAMERA_TRIGGER	—	—	AON[1]
SLV_SCL	C3	B12	IO:I2C_PMU_SCL[3]	—	—	—	—	—	—	PU	AON
			IO:GPIO45[3]	IO:I2C_SLV_SCL	I:UART0_RX_C	—	—	—	—	PU	—
			IO:GPIO47[3]	IO:I3C_SLV_SCL	—	—	—	—	—	PU	—
SLV_SDA	C1	A11	IO:I2C_PMU_SDA[3]	—	—	—	—	—	—	PU	AON
			IO:GPIO44[3]	IO:I2C_SLV_SDA	O:UART0_TX_C	—	—	—	—	PU	—
			IO:GPIO46[3]	IO:I3C_SLV_SDA	—	—	—	—	—	PU	—
I2S_BLK	G13	G3	IO:GPIO17	IO:I2S_BCLK	O:TRACE_DATA3	I:DM_HOST_CLK	—	—	—	—	—
I2S_DI	M14	H2	IO:GPIO20	IO:I2S_DI	O:TRACE_DATA0	I:DM1_DATA_B	—	—	—	—	—
I2S_DO	M12	H4	IO:GPIO19	IO:I2S_DO	O:TRACE_DATA1	IO:DM1_CLK_B	—	—	STRAP0	PD	—
I2S_FSYNC	J13	F4	IO:GPIO18	IO:I2S_FSYNC	O:TRACE_DATA2	O:DM_HOST_DATA	—	—	—	—	—
I2C0_MS_SCL	B16	H10	IO:GPIO15	IO:I2C0_MS_SCL	IO:I3C_MS_SCL	IO:DM0_CLK_C	—	—	—	PU	—
I2C0_MS_SDA	D14	G5	IO:GPIO16	IO:I2C0_MS_SDA	IO:I3C_MS_SDA	I:DM0_DATA_C	—	—	—	PU	—

Ball Name	SR100 Series FCCSP Ball No.	SR100 Series WLCSP Ball No.	ALT 0 (Default)	ALT 1	ALT 2	ALT 3	ALT4	ALT5	Strap	PUboot/ PDboot[2]	AON
JTAG_TCK	C17	J11	I:JTAG_TCK	IO:GPIO31	—	—	—	—	—	PU	—
JTAG_TMS	B18	K10	IO:JTAG_TMS	IO:GPIO32	—	—	—	—	—	PU	—
PMU_EN	L11	F2	—	—	—	—	—	—	—	—	—
RESET_N	J1	A7	I:RESET_N	—	—	—	—	—	—	PU	—
SDO_CLK	E9	F12	IO:GPIO26	O:SDO_CLK	IO:DM0_CLK_A	O:TRACE_CLK	—	O:UART_LP_TX_B	STRAP1	PD	—
SDO_CMD	C7	N/A	IO:GPIO25	IO:SDO_CMD	—	—	—	—	—	PU	—
SDO_D0	E13	H6	IO:GPIO27	IO:SDO_D0	I:DM0_DATA_A	—	—	I:UART_LP_RX_B	—	—	—
SDO_D1	G11	N/A	IO:GPIO28	IO:SDO_D1	—	—	—	—	—	—	—
SDO_D2	E11	N/A	IO:GPIO29	IO:SDO_D2	IO:DM1_CLK_A	—	—	—	—	—	—
SDO_D3	C13	N/A	IO:GPIO30	IO:SDO_D3	I:DM1_DATA_A	—	—	—	—	—	—
SD1_CLK	G17	N/A	IO:GPIO35	O:SD1_CLK	—	—	—	—	—	PU	—
SD1_CMD	J17	N/A	IO:GPIO34	IO:SD1_CMD	I:JTAG_TRSTN_B	—	—	—	—	PU	—
SD1_D0	G15	N/A	IO:GPIO36	IO:SD1_D0	I:JTAG_TDI_B	—	—	—	—	PU	—
SD1_D1	K14	N/A	IO:GPIO37	IO:SD1_D1	IO:JTAG_TDO_B	—	—	—	—	PU	—
SD1_D2	K12	N/A	IO:GPIO38	IO:SD1_D2	—	—	—	—	—	PU	—
SD1_D3	L13	N/A	IO:GPIO39	IO:SD1_D3	—	—	—	—	—	PU	—
SPI_MSTR_CLK	B14	G11	IO:GPIO22	IO:SPI_MSTR_CLK	I:UART0_RX_B	I:CIU_D5	—	—	—	—	—
SPI_MSTR_CS	E15	J9	IO:GPIO21	O:SPI_MSTR_CS	O:UART0_TX_B	I:CIU_D4	—	—	—	—	—
SPI_MSTR_MISO	A15	H8	IO:GPIO24	I:SPI_MSTR_MISO	I:UART1_RX_A	IO:I2C1_MS_SDA	—	—	—	PU	—
SPI_MSTR_MOSI	B12	G9	IO:GPIO23	O:SPI_MSTR_MOSI	O:UART1_TX_A	IO:I2C1_MS_SCL	—	—	—	PU	—
SPI_SLV_CLK	E3	C11	IO:GPIO2	I:SPI_SLV_CLK_A	O:UART_LP_TX_A	I:SD0_CDn	IO:LP_GPIO2	O:AON_GPO1	—	PU	AON
SPI_SLV_CS	G7	C7	IO:GPIO3	I:SPI_SLV_CS_A	I:UART_LP_RX_A	I:SD0_WP	IO:LP_GPIO3	I:AON_GPI1	—	PU	AON
SPI_SLV_MISO	A1	B10	IO:GPIO0	O:UART0_TX_A	IO:SPI_SLV_MISO_A	IO:LP_GPIO0	—	O:AON_GPO0	TEST_N	PU	AON
SPI_SLV_MOSI	G5	C9	IO:GPIO1	I:UART0_RX_A	I:SPI_SLV_MOSI_A	IO:LP_GPIO1	—	I:AON_GPI0	—	—	AON
SWIRE_CLK	H14	K8	IO:GPIO42	—	—	IO:I2C1_MS_SCL_B	—	—	—	—	—
SWIRE_DATA	H16	L5	IO:GPIO43	—	—	IO:I2C1_MS_SDA_B	—	—	—	—	—
POR_BYPASS	K8	E1	—	—	—	—	—	—	—	—	—
TEST_ANA	K6	E3	—	—	—	—	—	—	—	—	—

Ball Name	SR100 Series FCCSP Ball No.	SR100 Series WLCSP Ball No.	ALT 0 (Default)	ALT 1	ALT 2	ALT 3	ALT4	ALT5	Strap	PUboot/ PDboot[2]	AON
PHY_ATB	E17	L7	—	—	—	—	—	—	—	—	—
USB_HS_DN	M16	K2	—	—	—	—	—	—	—	—	—
USB_HS_DP	N15	J1	—	—	—	—	—	—	—	—	—
USB_HS_REXT	M18	K4	—	—	—	—	—	—	—	—	—
VBAT	L1	A5	—	—	—	—	—	—	—	—	—
VDD_BUCK_COIL	N1	A3	—	—	—	—	—	—	—	—	—
VCC18_OUT	M8	C3	—	—	—	—	—	—	—	—	—
VDD_AON	M4	B4	—	—	—	—	—	—	—	—	—
VDD_0	N3	B2	—	—	—	—	—	—	—	—	—
VDD_CORE	E1, G1, N13	D6, K6, G7	—	—	—	—	—	—	—	—	—
VDDIO1P8	M20, N19	G1	—	—	—	—	—	—	—	—	—
VCC18_IN	M10	C1	—	—	—	—	—	—	—	—	—
VSSA	N7	B6	—	—	—	—	—	—	—	—	—
VDDH_USB	N17	L1	—	—	—	—	—	—	—	—	—
VSSA_REF	J5	D4	—	—	—	—	—	—	—	—	—
VDDA	M6	D2	—	—	—	—	—	—	—	—	—
VSS	C21, E5, E7, E19, F2, G19, K2, L21, L19, L17, N11	C5, E5, J7, M6	—	—	—	—	—	—	—	—	—
GND_BUCK_COIL	M2	A1	—	—	—	—	—	—	—	—	—
XSPI_CLK	A9	E11	—	—	—	—	—	—	—	—	—
XSPI_CLKN	C11	N/A	—	—	—	—	—	—	—	—	—
XSPI_CSON	A5	F6	—	—	—	—	—	—	—	PU	—
XSPI_CS1N	J9	N/A	—	—	—	—	—	—	—	PU	—
XSPI_DATA0	B8	E7	—	—	—	—	—	—	—	—	—
XSPI_DATA1	B6	F8	—	—	—	—	—	—	—	—	—
XSPI_DATA2	A7	E9	—	—	—	—	—	—	—	—	—
XSPI_DATA3	B10	F10	—	—	—	—	—	—	—	—	—

Ball Name	SR100 Series FCCSP Ball No.	SR100 Series WLCSP	ALT 0 (Default)	ALT 1	ALT 2	ALT 3	ALT4	ALT5	Strap	PUboot/ PDboot[2]	AON
XSPI_DATA4	F8	N/A	—	—	—	—	—	—	—	—	—
XSPI_DATA5	G9	N/A	—	—	—	—	—	—	—	—	—
XSPI_DATA6	C9	N/A	—	—	—	—	—	—	—	—	—
XSPI_DATA7	H10	N/A	—	—	—	—	—	—	—	—	—
XSPI_DQS	J7	N/A	—	—	—	—	—	—	—	—	—
XTAL24M_IN	M22	P2	—	—	—	—	—	—	—	—	—
XTAL24M_OUT	N21	N1	—	—	—	—	—	—	—	—	—

1.Could be used to hold PU/PD state during AON.

2. **PUboot/PDboot:** Always pulled after reset, but software can disable them afterward.
3. Default Tri-state and OR together.

3.3. Functional Description

3.3.1. Processing

- Main processor: Arm® Cortex®-M55 CPU
  - Clock frequency: Up to 400 MHz
  - 32 kB of instruction cache
  - 32 kB of data cache
  - 128 kB of ITCM memory and 128 kB of DTCM memory
  - Arm CoreSight™ debugging interface
  - TrustZone®
  - Support standard tool chains
- Low power processor: Arm® Cortex®-M4 CPU
  - Clock frequency: Up to 100 MHz
  - 4 kB of cache
- Main NN processor: Arm Ethos™-U55 micro NPU core
  - Clock frequency: Up to 400 MHz
  - 128 MACs/cycle
  - 24 kB of memory
- ULP NN processor: Synaptics propriety NN processor
  - Clock frequency: Up to 100 MHz
  - Automatic cache pre-fetch with zero miss-penalty

3.3.2. Memory

- Up to 3008 kB of system memory, including 1448 kB of LP system memory
- 630 kB of ULP audio and video sense memory
- All memories can be completely turned off, LP system memory and ULP memory can be retained
- Ultra-low power 16 kB AON memory

3.3.3. Inter-IC (I2C) Interface

3.3.3.1. Fast-Mode+ Target I2C Interface

SR100 Series has one I2C Target interface.

The Target I2C interface features:

- Up to 1 MHz support
- Configurable device ID
- 64 entry Rx and Tx FIFOs

3.3.3.2. Host I2C Interface

SR100 Series has two I2C Host interfaces.

Each Host I2C interface features:

- Up to 1 MHz support
- 32 entry Rx and Tx FIFOs

3.3.4. Universal Asynchronous Receiver Transmitter (UART) Interface

There are two enhanced serial UART interfaces, compatible with the industry-standard 16450/16550 UART. They can be used for communication, testing and logging data as well as boot option.

The UART features:

- UART0 support SW or CTS/RTS flow control
- UART1 support SW flow control
- Programmable baud rates for rates up to 6 Mbps
- 7, 8 or 9 data bits
- 1 or 2 stop bits
- Optional parity bit
- Software flow control
- 64 entry Rx and Tx FIFOs

3.3.5. Serial Peripheral Interface (SPI)

3.3.5.1. SPI Target

Features include:

- SPI_CLK frequencies: up to 25 MHz
- Choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol, or National Semiconductor Microwire
- Programmable data item size of 4-32 bits
- Programmable serial clock and phase polarity
    - SPI modes 0 through 3
- Single frame and block transfers
- 32 entry Rx and Tx FIFOs

3.3.5.2. SPI Host

The SPI Host features include:

- SPI_CLK frequencies: up to 25 MHz
- Choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol, or National Semiconductor Microwire
- Programmable data item size of 4-32 bits
- Programmable serial clock and phase polarity
    - SPI modes 0 through 3
- Single frame and block transfers
- 8 entry Rx and Tx FIFOs

3.3.6. General-Purpose I/O (GPIO)

This unit features:

- Up to 43 multiplexed GPIOs (1.8V domain), that can be configured as external interrupts
- 27 GPIOs in the WLCSP
- All I/Os can be configured as pull-up, pull-down, open-drain, and bus keeper
- Configurable drive-strength and slew-rate
- Schmitt trigger support
- Input-triggered interrupt, configurable as Edge or Level
- Fail-Safe, I/O pad sustain voltage without current flowing from bus to the chip when both IO and VDD are off

3.3.7. System Timers

There are up to eight 32-bit timers. The timers have the following features:

- Configurable timer width: 8 to 32 bits
- Support for two operation modes: free-running and user-defined count
- Support for independent clocking of timers.

3.3.8. Watchdog Timer

The Watchdog timer has the following features:

- Configurable watchdog counter width of 16 to 32 bits

- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout

3.3.9. I2S

Serial digital audio interfaces provide streaming audio connectivity to external Codecs or AP audio bus.

The I2S interface block supports the following modes and configurations on the I2S/PCM bus:

- Word lengths of 8, 16, 24 bits
- Supports Philips (I2S)/left justified/right justified/PCM/TDM modes
- Supports Host and Target mode
- Supports sharing of the WS signal between transmitter and receiver
- Programmable length of WS signal in Host mode
- Data may be driven on falling or rising edge of SCLK
- Programmable channel order - 'left then right' or 'right then left'
- Up to 12.288 MHz SCLK
- I2S supports four channels in and four channels out

3.3.10. Digital Microphone (DM) Interface

The DM interface enables direct connection to a digital acoustic microphone.

The features include:

- Two interfaces with up to four digital microphones over a 1-bit PDM oversample bit stream
- Configurable output clock
- Support for sampling rates of 8, 16, 22.05, 32, 44.1, 48 kHz
- Configurable sample sizes: 16-bit or 24-bit

3.3.11. AUDIO_MUTE pin

HW pin that can block audio received from the digital microphones or from the I2S to be transmitted toward the Host.

The mute function is configurable to block either the audio input to the SR100 Series device, the audio output from SR100 Series device or both.

3.3.12. I3C

I3C is a low power, high speed, backwards compatible improvement to the I2C interface. Like I2C, it is a multi-drop bus that uses two wires for the bi-directional transfer of data and commands. However, I3C is designed to provide additional capabilities and improved efficiency compared to I2C. Some key features are:

- Two wire serial interface up to 12.5 MHz using push-pull
- Legacy I²C device co-existence on the same bus (with some limitations)
- Dynamic addressing while supporting static addressing for legacy I²C devices
- Legacy I²C messaging
- I²C-like single data rate (SDR) messaging
- Multi-Host capability
- In-band interrupt support
- Hot-join support
- 1.8V operation

The SR100 Series device has single I3C Target, the Target interface is used for fast boot and control of external AP.

The SR100 Series device has single I3C Host, the Host interface is used to connect I3C and I2C sensors and future AON cameras.

- Each I3C has 32 Rx and Tx FIFOs

3.3.13. SoundWire Target Interface

MIPI SoundWire®, consolidates many of the key attributes in mobile and PC audio interfaces, providing a common, comprehensive interface and scalable architecture that can be used to enable audio features and functions in multiple types of devices and across market segments. It supports the use of advanced amplifiers and microphones.

The SoundWire interface provides the following key capabilities:

- Transport of payload data and command over the same two-pins interface
- High-quality, low-latency audio transfer from the digital microphones connected to SR100 Series device to the main CPU
- Flexibility and versatility. SoundWire can be easily integrated into different hardware configurations, making it suitable for various devices such as laptops, tablets, and smartphones
- Support wakeup of the CPU Host during always on operation

The SoundWire interface in the SR100 Series is a Target interface, and it is used to control and transfer data from one to four microphones to the main-CPU using the SoundWire bus.

3.3.14. USB 2.0

The USB in the SR100 Series features:

- USB 2.0 Hi-Speed 480 Mbps
- Compliant with USB audio device class definition 1.0 and above
- Supports USB HID consumer controls for USB to GPIO bridge control and button press
- Supports audio transfers of 8 kHz -48 kHz sampling rates
- Optimized for low power support

When working with USB, 24 MHz clock must be present at the XTAL_IN input, generation of this clock is done with Crystal or supplied as digital clock.

3.3.15. SDIO

The SR100 Series support two 4-bits SDIO interfaces, one is used for SDCARD and the other for WIFI control.

The SDCARD interfaces are 1.8V only, so when using external SDCARD, the SDCARD should carry the “LV” logo that guarantees 1.8V Voltage work, else the SDCARD should be connected to the SR100 Series device via 1.8<->3.3V Level shifter.

The SDIO primary features are as follows:

- Supports SD memory and SD Input/Output (SDIO) digital interface protocol, and compliant with SD HCI Specification1-4 bits interface
- Supports 4-bit interface
- Supports UHS-I mode
- Supports default speed, high speed, SDR12, SDR25, SDR50 speed modes
- Supports SDIO read wait
- Supports SDIO card interrupts in both 1-bit and 4-bit modes

- Wake up on card interrupt

3.3.16. xSPI

xSPI (Expanded Serial Peripheral Interface) is the serial synchronous communication protocol developed by JEDEC eXpanded Serial Peripheral Interface (xSPI)for Non-Volatile Memory Devices which provides high data throughput, low signal count, and limited backward compatibility with legacy Serial Peripheral

Interface (SPI) devices.

The xSPI electrical interface can deliver up to 266 MBytes per second raw data throughput.

The 'xSPI' primary features are as follows:

- SPI Memory Independent: Device parameters (including command encoding) are run-time programmable Fully configurable SPI interface: x1, x2, x4, x8 SPI, STR and DTR, 4 to 32 bit-word transmission per date line, programmable SPI clock phase & polarity
- Zero software overhead with XIP/AIP and auto-configuration
- SPI Memory Independent: Device parameters (including command encoding) are run-time programmable
- Support proprietary SPI protocols used by the NOR-Flash, NAND-Flash and PSRAM vendors
- SPI memory controller allows SPI memory read (eXecute In Place - XIP) or read/write (Access In Place - AIP) access with standard AHB transactions

The 'xSPI' memory is used in the SR100 Series for:

- Booting from serial memory.
  - The boot support 1-4 bits serial QSPI memories and start with 1-bit boot
- Extending the SRAM for large NN models use

Using FCCSP package option enables two additions on top of WLCSP usage:

- 'xSPI' pins can be extended up to 8 data bit transfer
- 'xSPI' can be connected to two memory devices in parallel via different CS signals.
  - Booting from SPI memory using the first CS followed by changing the setup for SRAM and start working with the 'xSPI' memory

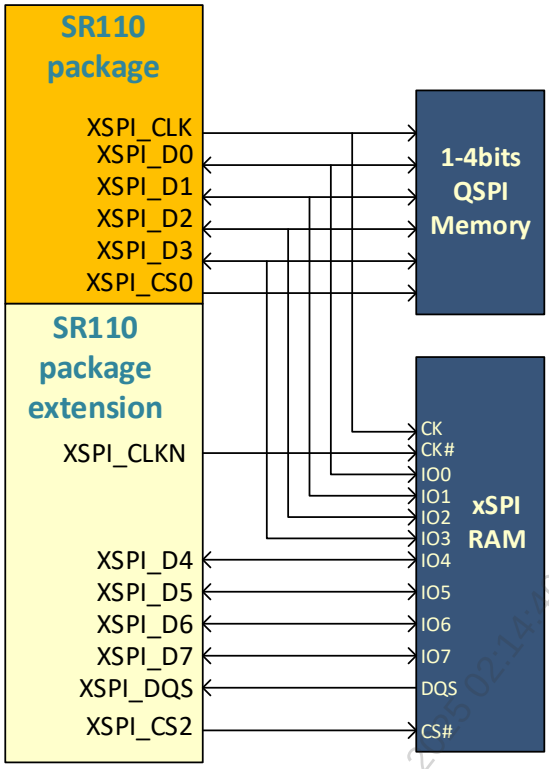


Figure 5. SR100 Series xSPI interfaces

3.3.17. CSI-2 Interfaces

CSI-2 is a high-bandwidth interface between a camera and a host processor. Data is transmitted using differential signals using a clock lane.

The protocol is divided into the following layers:

- Physical Layer (D-PHY)
- Lane Merger Layer
- Low Level Protocol Layer
- Pixel to Byte Conversion Layer
- Application Layer

MIPI CSI-2 interface is a unidirectional differential serial interface with data and clock signals. There can be up to two data lanes for each interface, each transferring data at up to 1.5 Gbps.

The control interface used to configure the image sensor is compatible with the I2C standard and is referred to as Camera Control Interface (CCI). The MIPI CSI-2 controller in the SR100 Series provides these two interfaces and some additional signals that image sensors commonly require.

CSI-2 primary features:

- Two MIPI CSI-2 RX interfaces, two lanes each, with max BW of 1.5Gb/Sec per lane
- One MIPI CSI-2 TX interface, two lanes channel, with max BW of 1.5Gb/Sec per lane
- Support up to resolution of 3840x2160(4K)
- MIPI RX aggregation mode joining two camera input streams to single output stream
- Bypass mode, delivering RX-0 directly to TX channel

3.3.17.1. CSI-2 Bypass mode

In bypass mode the data from camera transferred directly from the SR100 Series CSI-2 input to the SR100 Series CSI-2 output.

Bypass mode can be done inside the aggregator if there is no input from the second camera.

The clock of the CSI-2 RX0 and TX streams during bypass mode and the clock of the CSI-2 output stream and their number of lanes are identical.

The maximum speed of the CSI-2 during bypass mode can reach 1.5Gb/s that fits resolutions of up to 4K@30fps.

3.3.17.2. CSI-2 Aggregation

In aggregation mode two streams of cameras from the CSI-2 RX interfaces packed into single output stream, to reduce the number of output signals.

The aggregation mode can be used only in the FCCSP package that has two CSI-2 RX channels.

Note: The total bandwidth of two input camera streams must not exceed the maximum bandwidth of the TX channel.

3.3.18. Camera Parallel Interface

The Camera Parallel Interface support grabbing pictures using 11-signals parallel bus.

The interface includes 3 control signals and 1-8 data bits. Small package support only 1 data bit.

The SR100 Series parallel interface supports:

- 1, 4, 8 bits data bus
- Up to 60fps@640x480 resolution. (When working in 4,8 bits mode)
- Image can be cropped during transmission for selected region of interest
- The maximum clock frequency of clock during parallel transmission is 36,864 MHz in 4-bits mode and 18.4 MHz in 8-bits mode
- Support input data bus bit order configuration

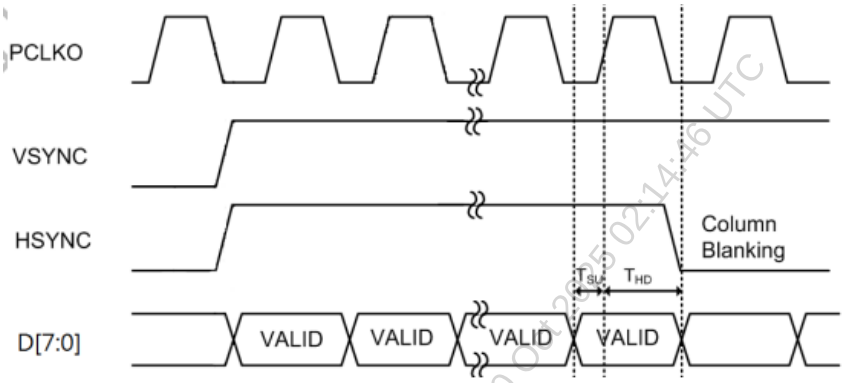


Figure 6. Camera parallel interface

3.3.19. Camera Serial Interface

The SR100 Series supports receiving two pins for SPI interface video input. The SPI video interface is typically used during low-power, low-resolution always on mode.

The two-wire serial interface consisting of the following signals:

- SCLKO – Serial Clock Output
- SDATA – Serial Data (byte base data transmission)

During SPI video transmission, there are two types of packets, control, and data. Every packet has sync code to indicate beginning of packet.

There are two states for the receiver part. One is the SYNC state, which means the receiver is waiting for the sync code, and in this state, the receiver would check the SYNC code per CSK, and the other is the RECV state, once the receiver recognizes the sync code, it enters RECV state. The receiver does not check for the sync code in the RECV state, and it returns to SYNC state once it receives the total amount of the packet.

Following the sync, the SPI can start receiving pixel data via interface.

The serial interface supports multiple camera manufacturer transition format with compatible SYNC words. height data location and width data locations are programmable to fit variety of cameras.

In the frame transmission, there is an optional CRC transmit check code for making sure the data validity.

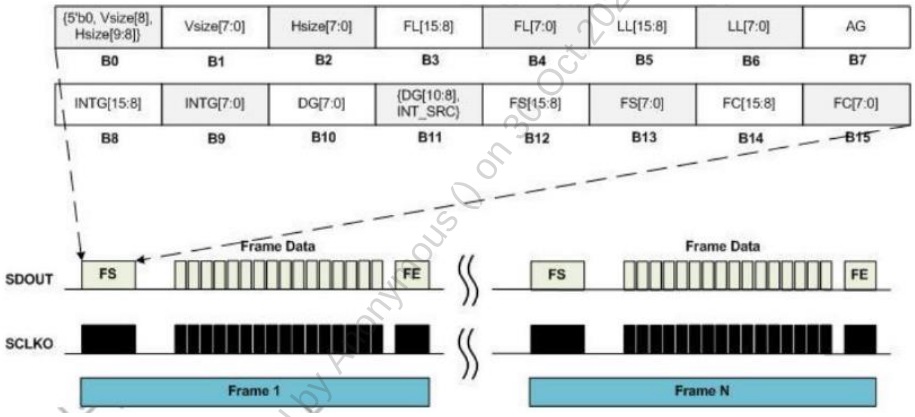


Figure 7. Video transmission using the SPI interface

3.3.20. VIDEO_MUTE pin

VIDEO_MUTE is an HW pin that block SR100 Series video output to the Host processor for security reason, without SW intervention to prevent any possible remote hacking threats.

3.3.21. CDM (Change Motion Detector)

An important part of power processing reduction in the SR100 Series is gained due to an HW Motion Detection. The motion detector is an image activity detection that prevent the SR100 Series to activate high-processing, high-power picture processing algorithm, if there is no change or motion seen in the captured scene from the camera.

Motion detection is the process of detecting a change in position of an object relative to its surroundings or the change in the surroundings relative to an object.

The motion detector has the following features:

- Ignore motion in irrelevant areas inside the scene
- Add scalable trigger of motion
- Gradual and sudden changes in the light conditions
- Adaptive to environmental changes

3.3.22. AON

The always on domain is an ultra-low power logic that stays on and waits for events from sensors, camera, or external Host when other SR100 Series processing domains are turned-off.

During an AON state, the SR100 Series set the minimum required memories in retention mode or leave them-on then turn-off completely the processing domains.

The AON can trigger wakeup to other domains upon:

- AON GPIOs transition change
- Timer interrupt
- I2C wakeup command

The AON clock can be received from external 32K input pins for accurate periodic wakeup events or from internal low-power low-frequency oscillator.

When the SR100 Series exit AON state, it resumes CPUs activity and higher power domains to enable AI processing.

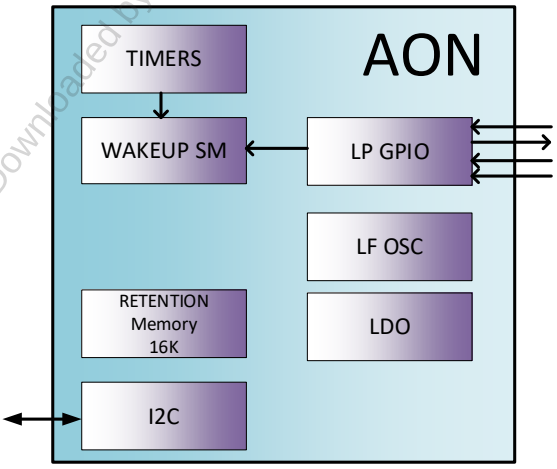


Figure 8. Always-On (AON) domain

Refer to Table 4 for list of AON GPIOs.

3.3.23. Power Management Unit (PMU)

3.3.23.1. Power Generation

The PMU powers the entire SR100 Series, Table 5 details the different power domains and their associated voltage requirements.

The PMU is designed to provide the best power efficiency at any given system power state. The VDD rail is driven by high-efficiency DCDC buck regulator, and the other rails are driven by internal linear regulators or by external supplies, selection between these should be done during the system power design.

Upon power-up, all domains are powered from LDOs. The DCDC switch regulator is turned on after boot is completed by software.

Table 5. PMU Voltage Domain Breakdown

Domain	Voltage Requirements	Description	Maximum Current (mA)
VBAT	3.3V+/-10%	Main supply to the SR100 Series. It can arrive from battery or from external power source.	—
VCC18_OUT	1.8V+/-5%	General purpose 1V8 LDO that can be used to supply all the 1V8 inputs.	100
VDD_AON	0.8V+/-10%	Low power 0V8 LDO output to the AON logic.	2
VDD_BUCK_COIL	0.8/0.9V+/-10%	VDD Buck regulator Inductor output.	250
VDD_CORE	0.7-0.9[1]V	Core logic supply input pin.	250
VDDA	0V8+/-5%	Low power 0V8 LDO output to the MIPI low voltage rail.	100
VDDH_USB	3.3V+/-10%	USB 3.3V supply to the USB transceiver.	30
VCC18_IN	1V8+/-5%	Supply to the AON LDO and to the analog 1.8V.	20
VCCIO	1V8+/-5%	I/O rail supply.	50
CSI0_IN_VP	0V8+/-5%	CSI Receiver 0V8 voltage input.	20
CSI0_IN_VH	1V8+/-5%	CSI Receiver 1V8 voltage input.	20
CSI1_IN_VP	0V8+/-5%	CSI Receiver 0V8 voltage input.	20
CSI1_IN_VH	1V8+/-5%	CSI Receiver 1V8 voltage input.	20
CSI_OUT_VP	0V8+/-5%	CSI Transmitter 0V8 voltage input.	20
CSI_OUT_VH	1V8+/-5%	CSI Transmitter 1V8 voltage input.	20

[1] Core voltage can vary between 0.7-0.9V according to the CPU speed and power modes.

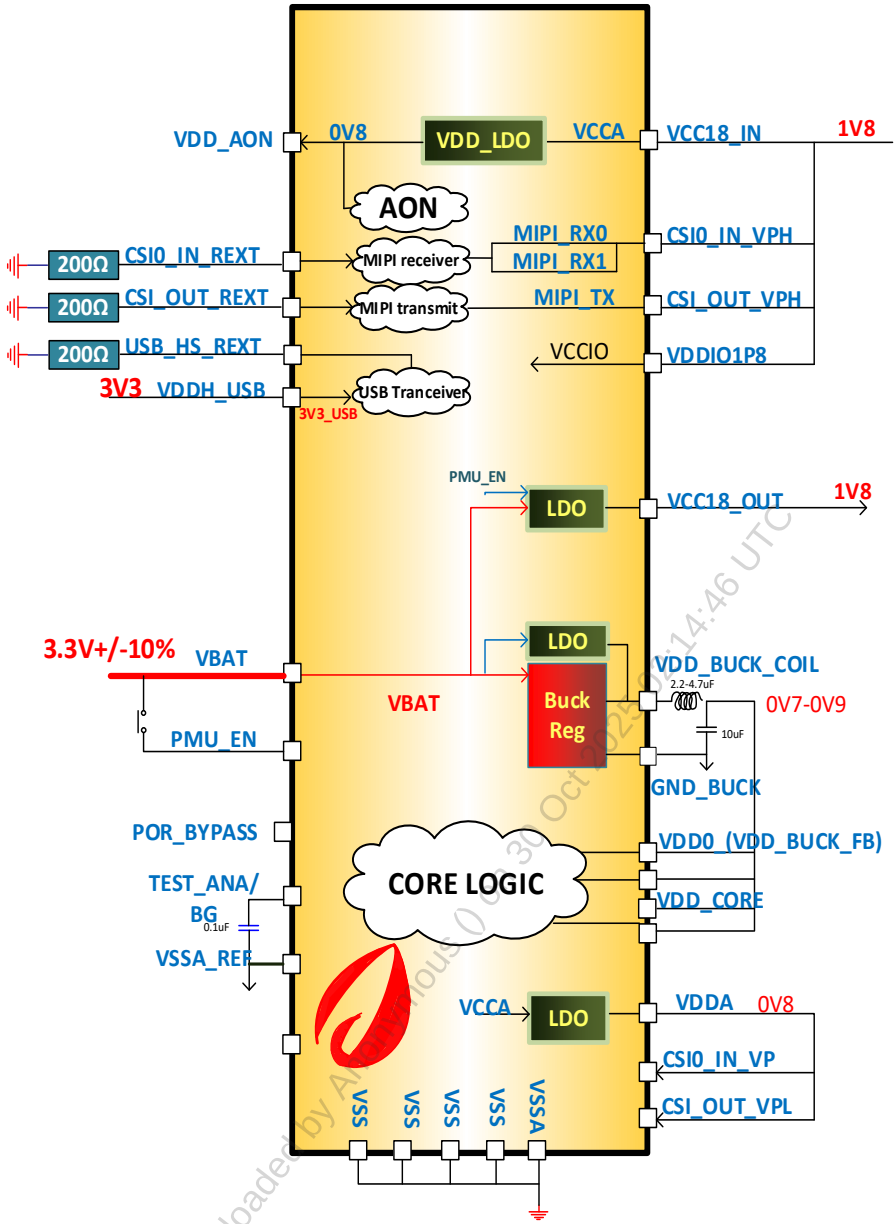


Figure 9. SR100 Series power diagram

3.3.23.2. PMU_EN

Toggling PMU_EN from low to high restarts the power sequence of SR100 Series.

When working with external AP, the AP can use an AP command to turn off the PMU and then turn it on by toggling the PMU_EN signal with GPIO from low to high.

PMU_EN is active high.

Note: PMU_EN only turns PMU on, it does not turn it off, A low on PMU_EN will not disable the PMU, only software can disable the PMU.

4. DC Electrical Characteristics

4.1. Absolute Maximum Ratings

Stresses above those listed in the Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
VBAT	Battery supply	-0.3	—	4.0	V
VDDH_USB	USB and 3V3 Analog supply	-0.3	3.3	3.63	
1V8_OUT	General purpose 1V8 LDO that can be used to supply all the 1V8 inputs	-0.3	—	1.9	
VDD_AON	Low power 0V8 LDO output to the AON logic	-0.3	—	0.9	
VDD_BUCK_COIL	VDD Buck regulator Inductor output	-0.3	—	0.9	
VDD_CORE	Core logic supply input pin.	-0.3	—	0.9	
VDDA	Low power 0V8 LDO output to the MIPI low voltage rail	-0.3	—	0.9	
VCC18_IN	Supply to the AON LDO and to the analog 1.8V	-0.3	—	1.98	
VDDIO1P8	I/O rail supply	-0.3	—	1.98	
CSI0_IN_VP	CSI Receiver 0V8 voltage input	-0.3	—	0.88	
CSI0_IN_VH	CSI Receiver 1V8 voltage input	-0.3	—	1.98	
CSI1_IN_VP	CSI Receiver 0V8 voltage input	-0.1	—	0.88	
CSI1_IN_VH	CSI Receiver 1V8 voltage input	-0.5	—	1.98	
V_{IN}	SLV_SCL, SLV_SDA, SWIRE_CLK, SWIRE_DATA	-0.3	—	1.98	
	Other 1.8V digital IO pins	-0.3	—	1.98 or VDDIO1P8+0.3, whichever is lower	
V_{OUT}	SLV_SCL, SLV_SDA, SWIRE_CLK, SWIRE_DATA	-0.3	—	1.98	
	Other 1.8V digital IO pins	-0.3	—	1.98 or VDDIO1P8+0.3, whichever is lower	
$T_{STORAGE}$	Storage temperature	-55	—	125	°C

4.2. Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VBAT	Battery supply	—	2.97	3.3	3.63	V
VDDH_USB	USB and 3V3 Analog supply	—	3.135	3.3	3.465	
VCC18_OUT	General purpose 1V8 LDO that can be used to supply all the 1V8 inputs	—	1.674	1.8	1.98	
VDD_AON	Low power 0V8 LDO output to the AON logic	—	0.72	0.8	0.99	
VDD_BUCK_COIL	VDD Buck regulator Inductor output	—	0.72	0.8	0.99	
VDD_CORE	Core logic supply input pin.	—	0.72	0.8	0.99	
VDDA	Low power 0V8 LDO output to the MIPI low voltage rail	—	-0.3	—	0.99	
VCC18_IN	Supply to the AON LDO and to the analog 1.8V	—	1.674	—	1.98	
VDDIO1P8	I/O rail supply	—	1.674	1.8	1.98	
CSI0_IN_VP	CSI Receiver 0V8 voltage input	—	0.744	0.8	0.88	
CSI0_IN_VH	CSI Receiver 1V8 voltage input	—	1.674	1.8	1.98	
CSI1_IN_VP	CSI Receiver 0V8 voltage input	—	0.744	0.8	0.88	
CSI1_IN_VH	CSI Receiver 1V8 voltage input	—	1.674	1.8	1.98	
VIN	SLV_SCL, SLV_SDA, SWIRE_CLK, SWIRE_DATA	—	1.674	1.8	1.98	
	Other 1.8V digital IO pins	—	1.674	1.8	1.98 or VDDIO1P8+0.3, whichever is lower	
VOUT	SLV_SCL, SLV_SDA, SWIRE_CLK, SWIRE_DATA	—	1.674	1.8	1.98	
	Other 1.8V digital IO pins	—	1.674	1.8	1.98 or VDDIO1P8+0.3, whichever is lower	
fCLKi	Storage temperature	—	-55	—	125	°C
T_A	Ambient operating temperature	Consumer	0	—	70	°C
		Industrial	-25	—	85	°C
TJ	Maximum junction temperature	Consumer	0	—	105	°C
		Industrial	-25	—	125	°C
RUSB2_REXT	USB 2.0 PHY reference current resistor, connect to VSS	—	—	200± 1%	—	Ohm
RCSI_IN_REXT, RCSI_OUT_REXT	CSI-2 reference current resistor, connect to VSS	—	—	200± 1%	—	Ohm

4.3. Thermal Conditions

The following tables present the thermal characteristics[2] of the FCCSP and WLCSP packages.

Table 8. FCCSP-122 Package Power Dissipation Characteristics

Characteristic	Ambient Temp. (oC)		Unit
	70	85	
Theta JA	26.261	26.079	° C/W
Theta JC	5.184		° C/W
Theta JT	0.03613		0.03796
Power (W)	0.25		W

Table 9. WLCSP-84 Package Power Dissipation Characteristics

Characteristic	Ambient Temp. (oC)		Unit
	70	85	
Theta JA	36.6	34.33	° C/W
Theta JC	0.1177		° C/W
Theta JT	0.067		0.033
Power (W)	0.25		W

[2] For thermal simulation, JEDEC standard PCB model was used, θ_JA (JESD 51-2A) and θ_JB (JESD 51-8). Substrate: 4L, 0.2 mm, 2s2p.

4.4. Crystal Specifications

Table 10. Crystal Specifications

Parameter	Condition	Typical	Unit
Fundamental Frequency	—	24	MHz
Frequency Tolerance and stability	0 – 70 °C	<= ± 50	ppm
Load Capacitance	—	8*	pF
Max. ESR	—	50 Ω (100 Ω, if CL1 and CL2<10pF)	Ohm
Drive Level	—	35	uW
Mode of Oscillation	—	Fundamental	—
Crystal circuit type	—	Parallel resonant	—

* For more design details, contact the Synaptics application engineering team.

4.5. AC and DC Electrical Characteristics

4.5.1. Digital Pins Operating Conditions

4.5.1.1. Digital Pins Operating Conditions for 1.8 V I/Os

Table 11 outlines the operating conditions for 1.8V digital I/Os.

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 11. Digital Operating Conditions for 1.8V I/Os

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	—	0.65*VDDIO1P8	—	VDDIO+0.3	V
V_{IL}	Low level input voltage	—	-0.3	—	0.35*VDDIO1P8	V
V_T	Threshold point	—	0.83	0.9	1	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	—	0.96	1.1	1.12	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	—	0.73	1	0.99	V
V_{TPU}	Threshold point with Pull-up Resistor Enabled	—	0.83	0.9	1	V
V_{TPD}	Threshold Point with Pull-down Resistor Enabled	—	0.84	0.9	1.01	V
V_{TPU+}	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	—	0.95	1	1.12	V
V_{TPU-}	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	—	0.72	1	0.98	V
V_{TPD+}	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	—	0.96	1.1	1.13	V
V_{TPD-}	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	—	0.73	0.8	0.91	V
R_{PU}	Pull-up resistor	—	54k	79k	120k	Ω
R_{PD}	Pull-down resistor	—	49K	84k	162k	Ω
V_{OH}	Output Low Voltage	—	VDDIO - 0.45	—	—	V
V_{OL}	Output High Voltage	—	—	—	0.45V	mA
I_{OL} Low Level Output Current @V_{OL} (max)	(DR1,DSO)='00'	—	7.6	12	17.7	mA
	(DR1,DSO)='01'	—	15.2	25	35	mA
	(DR1,DSO)='10'	—	22.7	37	51.8	mA
	(DR1,DSO)='11'	—	30	48	67.6	mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OH} High Level Output Current @V_{OH} (max)	(DR1,DSO)='00'	—	4.8	11	18.1	mA
	(DR1,DSO)='01'	—	9.4	21	35.9	mA
	(DR1,DSO)='10'	—	14.2	31	53.9	mA
	(DR1,DSO)='11'	—	18.8	41	71.5	mA
Input Capacitance	—	—	—	4	—	pF
I_I	Input Leakage Current	VI=1.8V or 0V	—	—	±10	µA
I_{OZ}	Tri-state Output Leakage Current	VO=1.8V or 0V	—	—	±10	µA

4.5.2. SD, SDIO Timing

4.5.2.1. SD, SDIO Default Mode Timing Parameters

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 12. SD, SDIO Default Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	25	25	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	10	—	—	Ns
t_{WH}	Clock High time	—	10	—	—	Ns
t_{TLH}	Clock Rise time	—	—	—	10	Ns
t_{THL}	Clock Fall time	—	—	—	10	Ns
Inputs CMD, DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	5	—	—	ns
t_{IH}	Input Hold time	—	5	—	—	Ns
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output delay time	Data Transfer Mode	0	—	14	Ns
t_{ODLY}	Output delay time	Identification Mode	0	—	50	ns

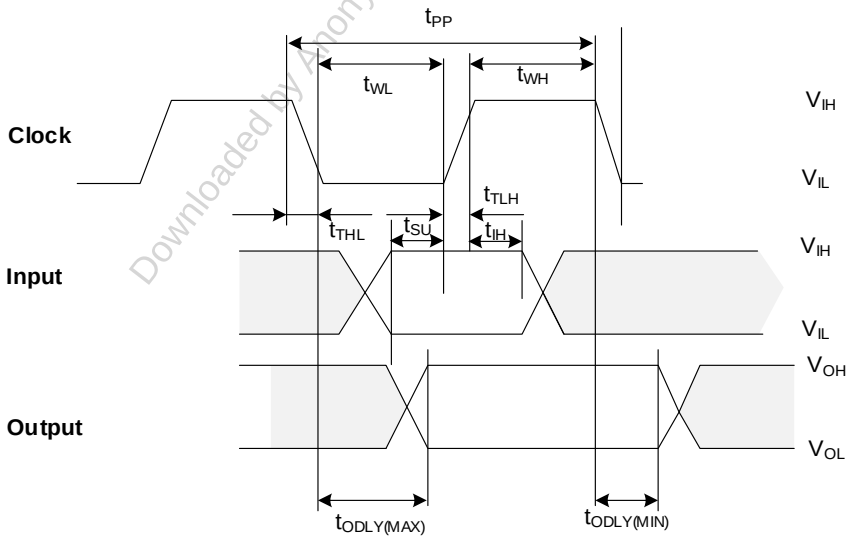


Figure 10. Timing Diagram Data Input/Output Referenced to Clock (Default)

4.5.2.2. SDIO High-Speed Mode Timing Parameters

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 13. SD, SDIO High-Speed Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	50	50	MHz
t_{WL}	Clock Low time	—	6	—	—	ns
t_{WH}	Clock High time	—	6	—	—	ns
t_{TLH}	Clock Rise time	—	—	—	4	ns
t_{THL}	Clock Fall time	—	—	—	4	ns
Inputs DAT (referenced to Clock)						
t_{ISU}	Input Setup time	—	3	—	—	ns
t_{IH}	Input Hold time	—	0.8	—	—	ns
Outputs CMD, DAT (referenced to Clock)						
t_{ODLY}	Output Delay time	Data Transfer mode	0	—	7.5	ns
t_{OH}	Output Hold time	—	1.5	—	—	ns

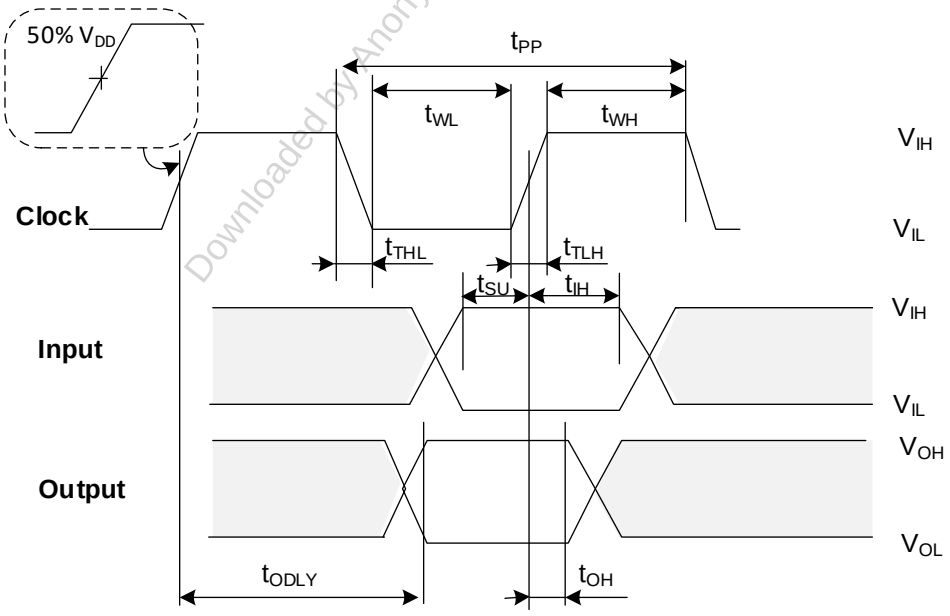


Figure 11. Timing Diagram Data Input/Output Referenced to Clock (High-speed)

4.5.3. I2C Timing

4.5.3.1. I2C and Fast Mode Timing

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 14. TWSI Standard and Fast Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{TWSI_SCL}	SCL Clock Frequency	100 kHz	—	—	100	kHz
		400 kHz	—	—	400	
T_{TWSI_NS}	Noise Suppression Time at SCL, SDA Inputs	100 kHz	—	—	80	ns
		400 kHz	—	—	80	
T_{TWSI_R}	SCL, SDA Rise time	100 kHz	—	—	1.95(1)	ns
		400 kHz	—	—	1.95(1)	
T_{TWSI_F}	SCL, SDA Fall Time	100 kHz	—	—	1.78(1)	ns
		400 kHz	—	—	1.78(1)	
T_{TWSI_HIGH}	Clock High Period	100 kHz	4000	—	—	ns
		400 kHz	600	—	—	
T_{TWSI_LOW}	Clock Low Period	100 kHz	4700	—	—	ns
		400 kHz	1300	—	—	
$T_{TWSI\_SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700	—	—	ns
		400 kHz	1200	—	—	
$T_{TWSI\_HD:STA}$	Start Condition Hold Time	100 kHz	4000	—	—	ns
		400 kHz	600	—	—	
$T_{TWSI\_SU:STO}$	Stop Condition Setup Time	100 kHz	4000	—	—	ns
		400 kHz	600	—	—	
$T_{TWSI\_SU:DAT}$	Data in Setup Time	100 kHz	250	—	—	ns
		400 kHz	100	—	—	
$T_{TWSI\_HD:DAT}$	Data in Hold Time	100 kHz	300	—	—	ns
		400 kHz	300	—	—	
T_{TWSI_BUF}	Bus Free Time	100 kHz	4700	—	—	ns
		400 kHz	1300	—	—	
T_{TWSI_DLY}	SCL Low to SDA Data Out Valid	100 kHz	10	—	N*i2c_core_clk(2)	ns
		400 kHz	10	—	N*i2c_core_clk(2)	

Note (1). SDA/SCL transition TTWSI_R and TTWSI_F is evaluated with 50pF output load.

Note (2). The max T_{TWSI_DLY} can be programed by IC_SDA_HOLD register, by times of I2C core clock cycle.

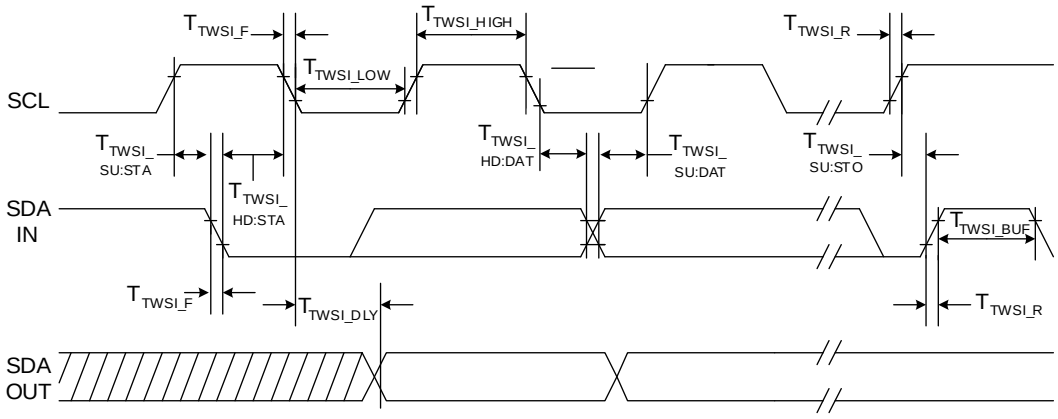


Figure 12. Two-wire serial interface timing

4.5.4. SPI Timing

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 15. SCLK Cycle Time Configurable Range

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SCLK}	SoC SPI SCLK cycle time	100 MHz SoC SPI controller input clock	20	—	655,340	ns

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 16. Motorola SPI Mode 0/2 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	The first SPI cycle in a transfer	—	1.5	—	TSCLK
		Subsequent SPI cycles	—	0.5	—	
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	Other than the last SPI cycle	—	1	—	TSCLK
		The last SPI cycle in a transfer	—	1.0	—	
T_{CH}	SCLK high time	—	—	0.5	—	TSCLK
T_{CL}	SCLK low time	—	—	0.5	—	TSCLK
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0.5	—	TSCLK
		If Tx FIFO is empty	2	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	3.5	—	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	0	—	—	ns
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	TSCLK
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	0.12	—	1.28	ns

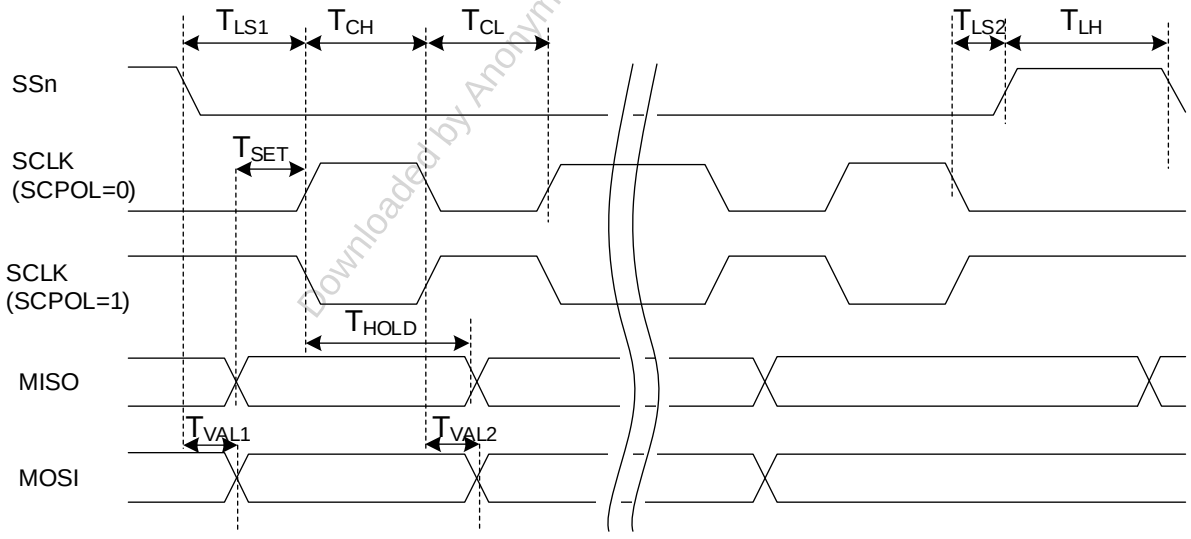


Figure 13. Motorola SPI Mode 0/2 (SCPH = 0)

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 17. Motorola SPI Mode 1/3 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	—	—	1.0	—	TSCLK
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	—	—	1.0	—	TSCLK
T_{CH}	SCLK high time	—	—	0.5	—	TSCLK
T_{CL}	SCLK low time	—	—	0.5	—	TSCLK
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0	—	TSCLK
		If Tx FIFO is empty	1.5	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	3.5	30	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	—	30	—	ns
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	TSCLK
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	—	0.5	—	ns

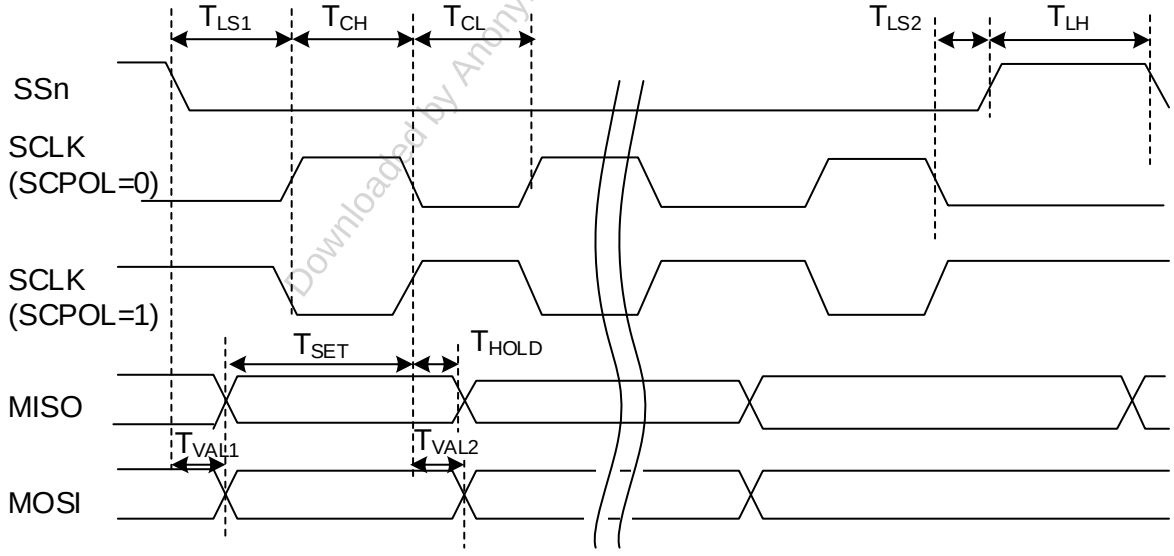


Figure 14. Motorola SPI Mode 1/3 (SCPH = 1)

4.5.5. UART Timing

Table 18. UART Timing

Symbol	Parameter	Condition	Min	Typ[1]	Max	Units
—	Tx bit width	±5%	0.166	8.68	—	µs
—	Rx bit width	±5%	0.166	8.68	—	µs

1.The typical values are 115.2 kbaud. Other baud rates may vary.

4.5.6. JTAG Timing

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 19. JTAG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CLK}	Clock cycle	—	—	42	—	ns
$T_{ISTRSTn}$	Set-up time for TRSTn	—	25%	—	—	Tclk
$T_{IHTRSTn}$	Hold time for TRSTn	—	4	—	—	ns
T_{ISTDI}	Set-up time for TDI	—	30%	—	—	Tclk
T_{IHTDI}	Hold time for TDI	—	4	—	—	ns
T_{OHTDO}	Hold time for TDO	—	0	—	—	ns
T_{OVTDO}	Data valid time for TDO	—	—	—	65%	Tclk
T_{RJT}	Rise time for all I/O	20-80%	3	—	—	ns
T_{FJT}	Fall time for all I/Os	80-20%	3	—	—	ns

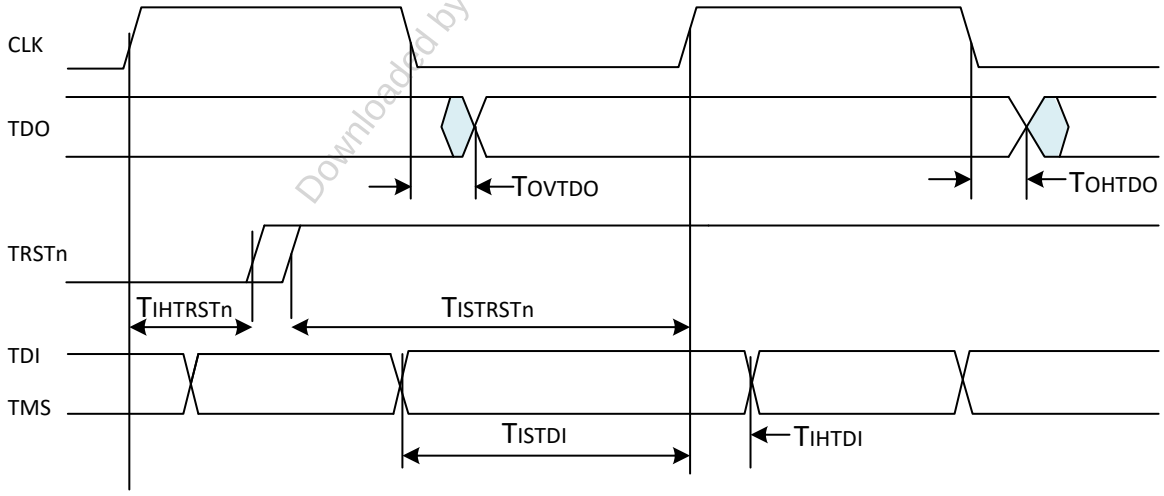


Figure 15. JTAG timing

4.5.7. I^2S Timing

4.5.7.1. I²S Host Mode Timing

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 20. I^2S Host Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	8Fs	—	128Fs	Hz
F_{BCLK_PCM}	BCLK Frequency in PCM Mono mode	—	8Fs	—	128Fs	Hz
F_{BCLK_TDM}	BCLK Frequency in TDM mode	—	8Fs	—	128Fs	Hz
F_S	—	—	—	—	48	kHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{SDPD1}	BCLK rising edge to SDATA output valid	—	—	0.5	—	ns
T_{LRPD}	BCLK rising edge to LRCK valid	—	—	0.5	—	ns
T_{SDS}	Set-up time SDATA input with regard to BCLK rising edge	—	—	6.58	—	ns
T_{SDH}	Hold time SDATA Input with regard to BCLK rising edge	—	—	0	—	ns
F_{MCLK}	MCLK (not shown) output frequency	—	—	—	6.144	MHz
D_{MCLK}	MCLK output duty cycle	—	—	50	—	%

1.BCLK may be inverted for more balanced setup and hold times.

2. Default AIOSYSCLK frequency is 300 MHz.

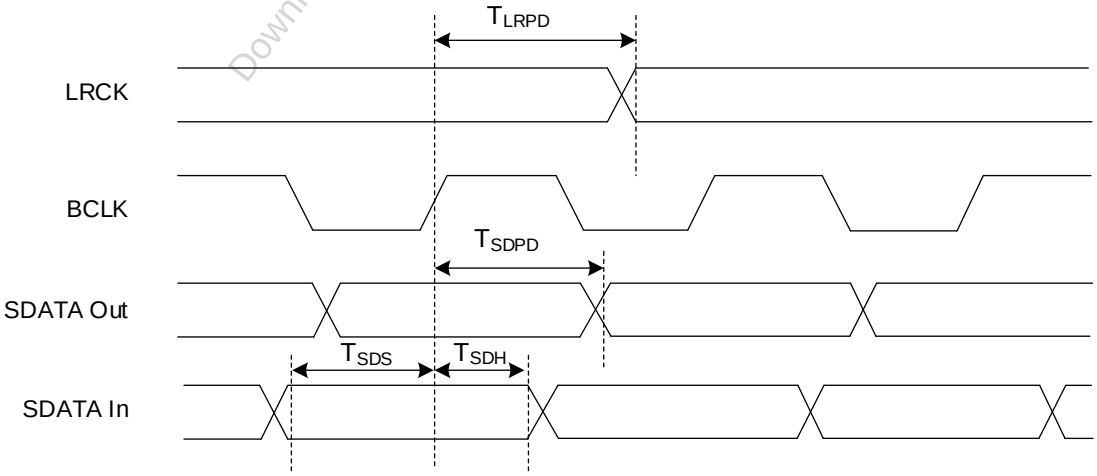


Figure 16. I^2S Host mode timing

4.5.7.2. I²S Target Mode Timing

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 21. I²S Target Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	8Fs	—	128Fs	Hz
F_{BCLK_PCM}	BCLK Frequency in PCM Mono mode	—	8Fs	—	128Fs	Hz
F_{BCLK_TDM}	BCLK Frequency in TDM mode	—	8Fs	—	128Fs	Hz
F_S	—	—	—	—	48	kHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{LRS}	Setup time LRCK input with regard to BCLK active edge	—	—	0.5	—	ns
T_{LRH}	Hold time LRCK input with regard to BCLK active edge	—	—	0.5	—	ns
T_{SDS}	Setup time SDATA Input with regard to BCLK active edge	—	—	2	—	ns
T_{SDH}	Hold time SDATA Input with regard to BCLK active edge	—	—	0	—	ns
F_{MCLK}	MCLK (not shown) input frequency	—	—	—	6.144	MHz
D_{MCLK}	MCLK input duty cycle	—	—	50	—	%

1.Default AIOSYSCLK frequency is 300 MHz.

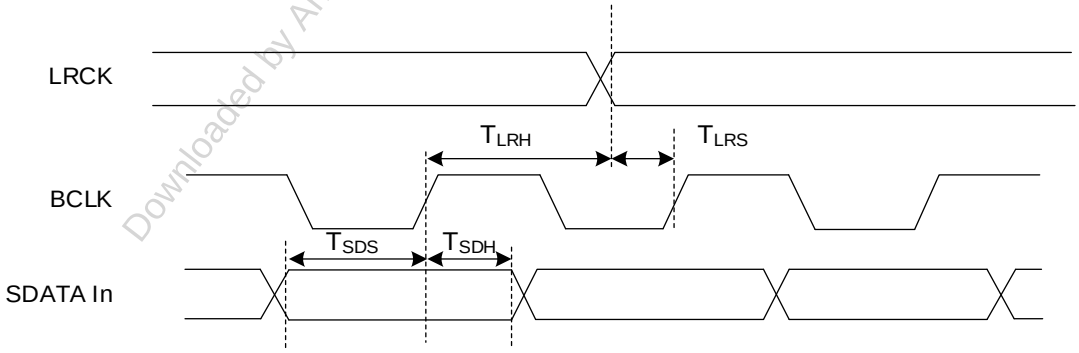


Figure 17. I²S Target mode timing

4.5.8. USB 2.0 Timing

4.5.8.1. USB 2.0 DC Characteristics

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 22. USB 2.0 DC Electrical

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	High (driven)	Note[1]	2.0	—	—	V
V_{IHZ}	High (floating)		2.7	—	3.6	V
V_{IL}	Low		—	—	0.8	V
V_{DI}	Differential Input Sensitivity	|(D+)-(D-)| Note[1]	0.2	—	—	V
V_{CM}	Differential Common Mode Range	Includes VDI range Note[1]	0.8	—	2.5	V
Input Levels for High-speed						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	—	100	—	150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)	—	525	—	625	mV
V_{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	—	-50	—	500	mV
Output Levels for Full-speed						
V_{OL}	Low	Note[1], Note[2]	0.0	—	0.3	V
V_{OH}	High (Driven)	Note[1], Note[3]	2.8	—	3.6	V
V_{OSE1}	SE1	—	0.8	—	—	V
V_{CRS}	Output Signal Crossover voltage	Note[4]	1.3	—	2.0	V
Output Levels for High-speed						
V_{HSOI}	High-speed idle level	—	-10.0	—	10.0	mV
V_{HSOH}	High-speed data signaling high	—	360	—	440	mV
V_{HSOL}	High-speed data signaling low	—	-10.0	—	10.0	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	—	700	—	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	—	-900	—	-500	mV
Input Capacitance for Full-speed						
C_{IND}	Downstream Facing Port	Note[5]	—	—	150	pF
C_{INUB}	Upstream Facing Port (without cable)	Note[6]	—	—	100	pF
C_{EDGE}	Transceiver edge rate control capacitance	—	—	—	75	pF

Symbol	Parameter	Condition	Min	Typ	Max	Units
Terminations						
R_{PU}	Bus pull-up Resistor on Upstream facing port	1.5 kOhm ±5%	1.425	—	1.575	kOhm
R_{PD}	Bus pull-down Resistor on Downstream Facing Port	15 kOhm ±5%	14.25	—	15.75	kOhm
Z_{INP}	Input impedance exclusive of pullup/pull-down (for full-speed)	—	300	—	—	kOhm
V_{TERM}	Termination voltage for upstream facing port pull-up (R_{PU})	—	3.0	—	3.6	V
Termination in High-speed						
V_{HSTERM}	Termination voltage in high-speed	—	-10	—	10	mV

1.Measured at A or B connector.

2. Measured with RL of 1.425 kOhm to 3.6V.3. Measured with RL of 14.25 kOhm to GND.
3. Excluding the first transition from the idle state.
4. Measured at A receptacle.6. Measured at B receptacle.

4.5.8.2. USB 2.0 Source Electrical Characteristics

(Applies across the full range of values listed in Table 7. Recommended Operating Conditions, unless otherwise specified.)

Table 23. USB High-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics						
T_{HSR}	Rise Time (10%–90%)	—	500	—	—	ps
T_{HSF}	Fall Time (10%–90%)	—	500	—	—	ps
Z_{HSDRV}	Driver Output Resistance (which also serves as high speed termination)	—	40.5	—	49.5	Ohm
Clock Timings						
T_{HSDRAT}	High-speed Data Rate	—	479.760	—	480.240	Mbps
T_{HSFRAM}	Microframe Interval	—	124.9375	—	125.0625	µs
T_{HSRFI}	Consecutive Microframe Interval Difference	—	—	—	4 highspeed bit times	—

Table 24. USB Full-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics						
T_{FR}	Rise Time	—	4	—	20	ns
T_{FF}	Fall Time	—	4	—	20	ns
T_{FRFM}	Differential Rise and Fall Time Matching	T_{FR}/T_{FF} Note[1]	90	—	111.11	%
Z_{DRV}	Driver Output Resistance for driver which is not high-speed capable.	—	28	—	44	Ohm
Clock Timings						
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high speed capable.	Average bit rate	11.9940	—	12.0060	Mbps
T_{FDRATE}	Full-speed Data Rate for devices which are high-speed capable.	Average bit rate	11.9700	—	12.0300	Mbps
T_{FRAME}	Frame Interval	—	0.9995	—	1.0005	ms
T_{RFI}	Consecutive Frame Interval Jitter	No clock adjustment	—	—	42	ns
Full-speed Data Timings						
T_{DJ1}	Source Jitter Total (including frequency tolerance): To Next Transition	Note[1] Note[2] Note[3]	-3.5	—	3.5	ns
T_{DJ2}	For Paired transitions	Note[4]	-4	—	4	ns
T_{FDEOP}	Source Jitter for Differential Transition to SE0 Transition	Note[3]	-2	—	5	ns
T_{JR1}	Receiver jitter: To Next Transition	Note[3]	-18.5	—	18.5	ns
T_{JR2}	For Paired Transitions	—	-9	—	9	ns
T_{FEOPT}	Source SE0 interval of EOP	—	160	—	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	Note[5]	82	—	—	ns
T_{FST}	Width of SE0 interval during differential transition	—	—	—	14	ns

1.Excluding the first transition from the idle state.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. For both transitions of differential signaling.
5. Must be accepted as valid EOP.

4.5.10. MIPI-TX Timing

Table 25. HS Line Drivers AC Specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit	Notes
tr	Differential output signal rise time	20% to 80%, RL = 50 Ω	—	—	0.3	UI	For PHY operating at or below 1Gbps
			—	—	0.35	UI	For PHY operating at or below 1G5bps
			100	—	—	ps	For PHY operating below or at 1G5bps
tf	Differential output signal fall time	20% to 80%, RL = 50 Ω	—	—	0.3	UI	For PHY operating at or below 1Gbps
			—	—	0.35	UI	For PHY operating at or below 1G5bps
			100	—	—	ps	For PHY operating below or at 1G5bps

Table 26. LP Line Drivers AC Specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit	Notes
trlp , tflp	Single ended output rise/fall time	15% to 85%, CL < 70 pF	—	—	25	ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
treot		30% to 85%, CL < 70 pF	—	—	35	ns	The rise-time of treot starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive. With an additional load capacitance CCM between 0 and 60 pF on the termination center tap at RX side of the Lane
∂V/∂tSR	Slew rate @ CLOAD = 0pF	15% to 85%, CL < 70 pF	—	—	500	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Measured as average across any 50 mV

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit	Notes
							segment of the output signal transition This value represents a corner point in a piece-wise linear curve. When the output voltage is in the range specified by VPIN(absmax).
	Slew rate @ CLOAD = 5pF		—	—	300	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Measured as average across any 50 mV segment of the output signal transition This value represents a corner point in a piece-wise linear curve. When the output voltage is in the range specified by PIN(absmax).
	Slew rate @ CLOAD = 20pF	—	—	—	250	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Measured as average across any 50 mV segment of the output signal transition This value represents a corner point in a piece-wise linear curve. When the output voltage is in the range specified by VPIN(absmax).
	Slew rate @ CLOAD = 70pF	—	—	—	150	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. he distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Measured as average across any 50 mV segment of the output signal transition This value represents a corner point in a piece-wise linear curve. When the output voltage is in the

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit	Notes
							range specified by PIN(absmax).
	Slew rate @ CLOAD = 0 to 70pF(Falling edge only)	—	25	—	—	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. When the output voltage is between 400 mV and 930 mV. Measured as average across any 50 mV segment of the output signal transition
	Slew rate @ CLOAD = 0 to 70pF(Rising Edge Only	—	25	—	—	mV/ns	Measured as average across any 50 mV segment of the output signal transition. When the output voltage is in the range specified by VPIN(absmax) When the output voltage is between 400 mV and 550 mV.
	Slew rate @ CLOAD = 0 to	—	—	—	—	—	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts. When the output voltage is between 550 mV and 790 mV Measured as average across any 50 mV segment of the output signal transition
	70pF	—	0	—	70	pF	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit	Notes
							50pF for a transmission line with 2ns delay

Table 27. HS Line Receiver AC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
ΔVCMRX(HF	Common mode interference beyond 450 MHz	—	—	—	50	mV	ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
ΔVCMRX(LF)	Common mode interference between 50 MHz and 450 MHz	—	-25	—	25	mV	—
CCM	Common mode termination	—	—	—	60	pF	—

4.5.11. MIPI-RX Timing

Table 28. HS Line Drivers AC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
	Maximum Serial Data rate (forward direction)	On DATAP/N outputs. 80 Ω ≤ RL ≤ 125 Ω	80	—	1500	Mbps	—
FDDRCLK	DDR CLK frequency	On CLKP/N outputs	40	—	750	Mbps	—
TDDRCLK	DDR CLK period	—	1.33	—	25	ns	—
UIINST	UI instantaneous	—	0.5	—	12.5	ns	This value corresponds to a minimum Mbps data rate.
ΔUI	UI variation	—	-10%	—	10%	UI	When UI ≥ 1ns, within a single burst.
		—	-5%	—	5%	UI	When 0.667ns < UI < 1ns, within a single burst.
tCDC	DDR CLK duty cycle	tCDC = tCPH / TDDRCLK	—	50	—	%	—
tCPH	DDR CLK high time	—	—	1	—	UI	—
tCPL	DR CLK low time	—	—	1	—	UI	—
—	DDR CLK/DATA Jitter	—	—	—	—	ps pk->pk	When UI < 1ns, withing a single burst.

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
tSKEW[PN]		—	-0.15	—	0.15	UI	For PHY operating at or below 1G5bps
tSKEW[TX]	Intra-Pair skew	—	0.15	—	—	UI	For PHY operating at or below 1Gbps
tSKEW[TLIS]	Data to Clock Skew	—	0.2	—	—	UI	For PHY operating above 1Gbps and below or at 1G5bps

Table 29. Clock Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
THOLD[RX]	Data to Clock Hold Time (RX)	—	0.15	—	—	UI	For PHY operating at or below 1Gbps
		—	0.2	—	—	UI	For PHY operating above 1Gbps and below or at 1G5bps
tSKEW[TLIS] static	—	—	-0.1	—	0.1	UI	For PHY operating above 1Gbps and below or at 1G5bps

Table 30. LP Line Drivers AC Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
trlp , tflp	Single ended output rise/fall time	15% to 85%, CL < 70 pF	—	—	25	ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
reot	30% to 85%, CL < 70 pF	—	—	—	35	ns	The rise-time of treot starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive. With an additional load capacitance CCM between 0 and 60 pF on the termination center tap at RX side of the Lane.
∂V/∂tSR	Slew rate @ CLOAD = 0pF	—	—	—	500	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Measured as average across any 50mV segment of the output signal transition. This value represents a corner point in a piece-wise linear curve. When the output voltage is in the range specified by VPIN (absmax)
	Slew rate @ CLOAD = 5pF	—	—	—	300	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Measured as average across any 50mV segment of the output signal transition This value represents a corner point in a piecewise linear curve. When the output voltage is in the range specified by VPIN (absmax).

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
∂V/∂tSR	Slew rate @ CLOAD = 20pF	—	—	—	250	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Measured as average across any 50mV segment of the output signal transition This value represents a corner point in a piecewise linear curve. When the output voltage is in the range specified by VPIN (absmax).
	Slew rate @ CLOAD = 70pF	—	—	—	150	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Measured as average across any 50mV segment of the output signal transition This value represents a corner point in a piecewise linear curve. When the output voltage is in the range specified by VPIN (absmax).
	Slew rate @ CLOAD = 0 to 70pF(Falling Edge Only)	—	25	—	—	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. When the output voltage is between 400mV and 930mV.

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
							Measured as average across any 50mV segment of the output signal transition.
∂V/∂tSR	Slew rate @ CLOAD = 0 to 70pF(Rising Edge Only)	—	25	—	—	mV/ns	Measured as average across any 50mV segment of the output signal transition. When the output voltage is in the range specified by VPIN (absmax). When the output voltage is between 400mV and 550mV
	Slew rate @ CLOAD = 0 to 70pF	—	25-0.0625 * (VO,INST - 550)	—	—	mV/ns	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts. When the output voltage is between 550mV and 790mV Measured as average across any 50mV segment of the output signal transition.
CL	Load capacitance	—	0	—	70	pF	CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay

Table 31. LP Line Receiver AC Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
eSPIKE	Input pulse rejection	—	—	300	—	V.ps	Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state. eSpike generation will ensure the spike is crossing both VIL,max and VIH,min levels. An impulse less than this will not change the receiver's state. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferer.
TMIN	Minimum pulse response	20	—		—	ns	An input pulse greater than this shall toggle the output.
VINT	Peak interference voltage	—	—	200	—	mV	—
fINT	Interference frequency	450	—		—	MHz	—

5. Application Information

5.1. Power Management

The SR100 Series power-up sequence follows these steps:

1. When power rises and exceeds 2.7V at VBAT pin, the power-up sequence is enabled.
2. Detection of VBAT reaches 2.7V+/-5%; the internal VBAT_OK signal is asserted.
3. The PWR_EN must be driven high or asserted externally at this stage.
4. The VCC18_OUT LDO starts operating.
5. When VCC18_IN and VCCIO exceed 1.6V (either shorted to VCC18_OUT or supplied externally) and VBAT > 2.7+/-5%, PWR_OK is asserted.
6. The PWR_OK signal turns ON the VDD_CORE buck regulator.
7. The XTAL oscillator starts operating or 24 MHz digital clock must be supplied to the XTAL_IN input pin.
8. After 20 ms, the RESET_N pin can be de-asserted. Note that RSTN must remain low for at least $PORRST_L$ us after the power levels reach their minimum values.
9. The boot ROM starts execution.
10. Based on the selected boot strap option, the Boot ROM either continues booting from external flash memory or waits for the external AP to send the boot image via SPI Target, UART, I3C Target, or I2C Target.

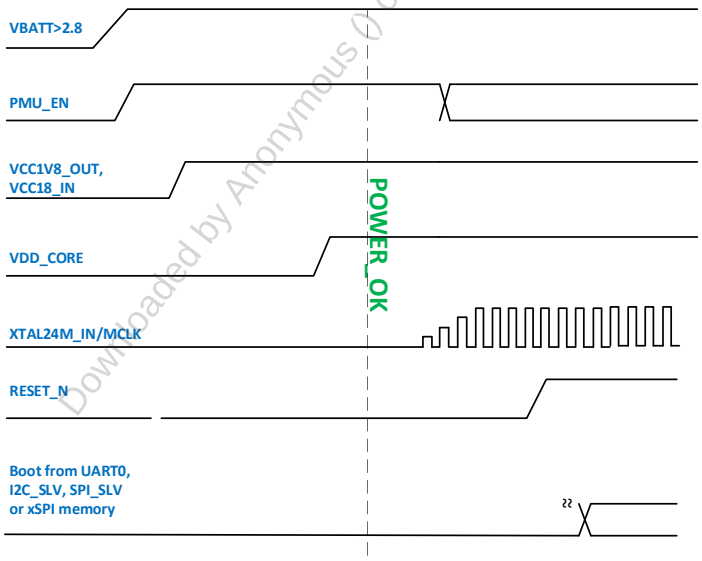


Figure 18. Power-up sequence

5.2. Boot Sequence

5.2.1. Determining the Boot Source

Table 32 outlines the high-level boot procedure. The boot source is defined according to two straps: STRAP0 and STRAP1. For strap pin configuration options corresponding to the selected interface, refer to Table 32.

The boot ROM implements various procedures based on the boot source. It first downloads a bootloader to configure the system, followed by downloading the complete code.

Table 32. Strap Pin Configuration

TEST_N (Default 1)	STRAP0 (Default 0)	STRAP1 (Default 0)	SR100 Series Mode of Operation
1	0	0	PLL (200 MHz) + QSPI
1	0	1	PLL (200 MHz) + External Host
1	1	0	PLLBYP (24 MHz)+ QSPI
1	1	1	PLLBYP (24 MHz) + External Host
0	0	0	test_en=1, jtag_sel=1
0	0	1	test_en=0, jtag_sel=1*
0	1	0	RSVD
0	1	1	RSVD

* Test = 1, JTAG 1 => Scan mode with JTAG enabled
Test = 0, JTAG 1 => Non-Scan mode with JTAG enabled

6. PCB and Layout Guidelines

6.1. Ground

Place the device in an area with a continuous ground plane, ensuring all ground balls are properly connected to it.

6.2. Digital and I/O Supplies

- The digital supply can be connected directly to the main digital supply rail if the noise levels are low. Otherwise, use a ferrite bead and a capacitor to create a low-pass (LP) filter.
- Place a 2.2uF ceramic capacitor close to the digital/I/O supply pin and connect it properly to VSS.
- If a large capacitor is not present on the VDD rail near the device, add a 1uF low-ESR capacitor (tantalum, ceramic, or electrolytic).
- If a dedicated digital supply layer exists, connect the digital supply directly to it. Otherwise, use wide traces for power delivery.

6.3. Analog Supply

- The SR100 Series has several analog supply balls that must be connected to a low-noise analog supply rail, ideally from a low-noise linear regulator.
- Place a 2.2uF ceramic capacitor close to the analog supply pins and connect it properly to VSS.

6.4. Buck Regulator Layout

- Minimize parasitic inductance in the DCDC input capacitor loop, ensuring a direct path from the VBAT pin to the capacitor's positive terminal and from the GND pin to the capacitor's negative terminal.
- Similarly, minimize the parasitic inductance in the DCDC output pins, ensuring a direct path from the capacitor's positive terminal to the VDD_BUCK_COIL inductor.
- Use wide traces for inductor connections to minimize resistance. Keep traces short and wide.
- Connect the inductor using multiple vias to the VCC_CORE power plane and the capacitor's positive terminal, ensuring a strong electrical connection.

6.4.1. CSI-2

- **Trace Length Matching:** Ensure each differential pair of CSI-2 traces has closely matched lengths to maintain signal integrity and prevent skew.
- **Impedance Matching:** Use a controlled impedance stack-up (typically 50 ohms) to minimize signal reflections. Adjust trace width and spacing accordingly.
- **Differential Pair Routing:** Route the CSI-2 differential pairs as tightly coupled traces with consistent spacing. Follow routing guidelines from the camera module manufacturer.
- **Grounding and Power Distribution:** Maintain a solid ground plane to provide a low-impedance return path. Use decoupling capacitors to minimize voltage fluctuations and noise.
- **Clock and Data Pair Separation:** Maximize separation between clock and data pairs to reduce electromagnetic coupling and crosstalk. Keep clock traces shorter than data traces to prevent skew.
- **Via Placement:** Minimize vias, as they introduce impedance discontinuities and signal reflections. Place ground vias around the high-speed traces for shielding and a uniform return path.

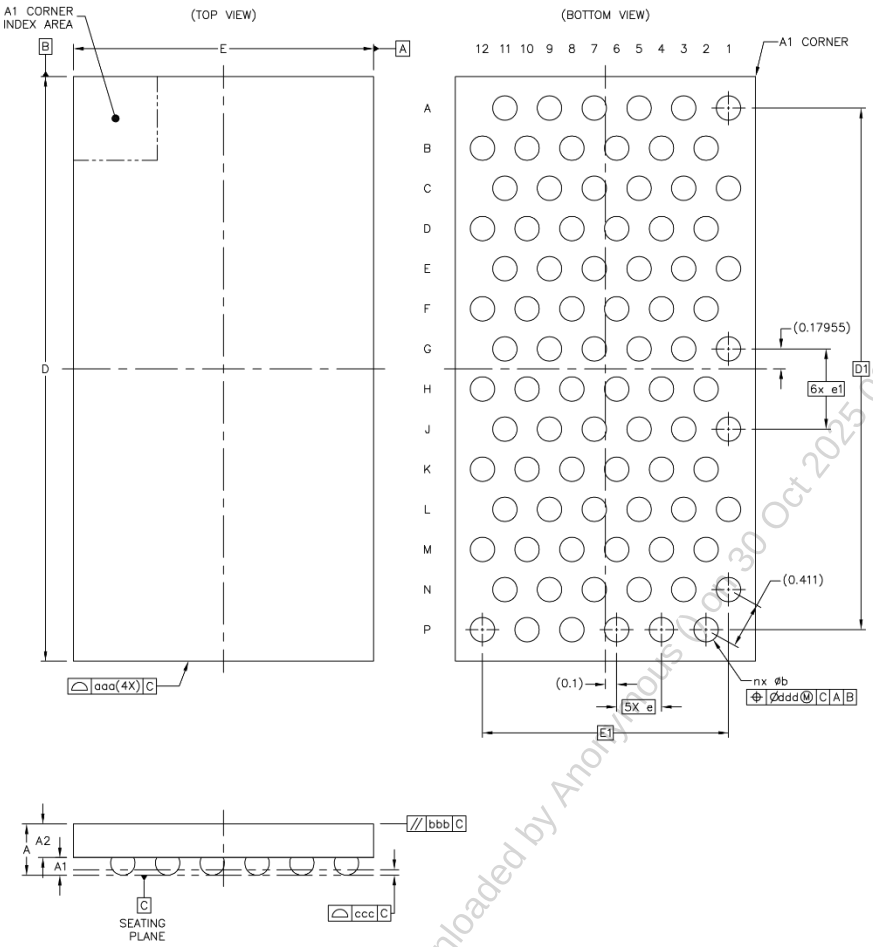
6.4.2. XTAL (Crystal Oscillator)

- Keep component leads and traces short to minimize parasitic effects and stray capacitance.
- Use a solid ground plane to reduce ground loops and noise coupling.
- Use a 24 MHz crystal for optimal performance.
- Select capacitors with low ESR and high Q factors for the feedback network.
- Ensure feedback capacitors are stable over temperature and frequency.
- Decouple power supply lines with bypass capacitors to prevent noise from affecting the oscillator's performance.

7. Mechanical Drawings

7.1. WLCSP-84 Package

Figure 19 illustrates the WLCSP-84 package drawing.

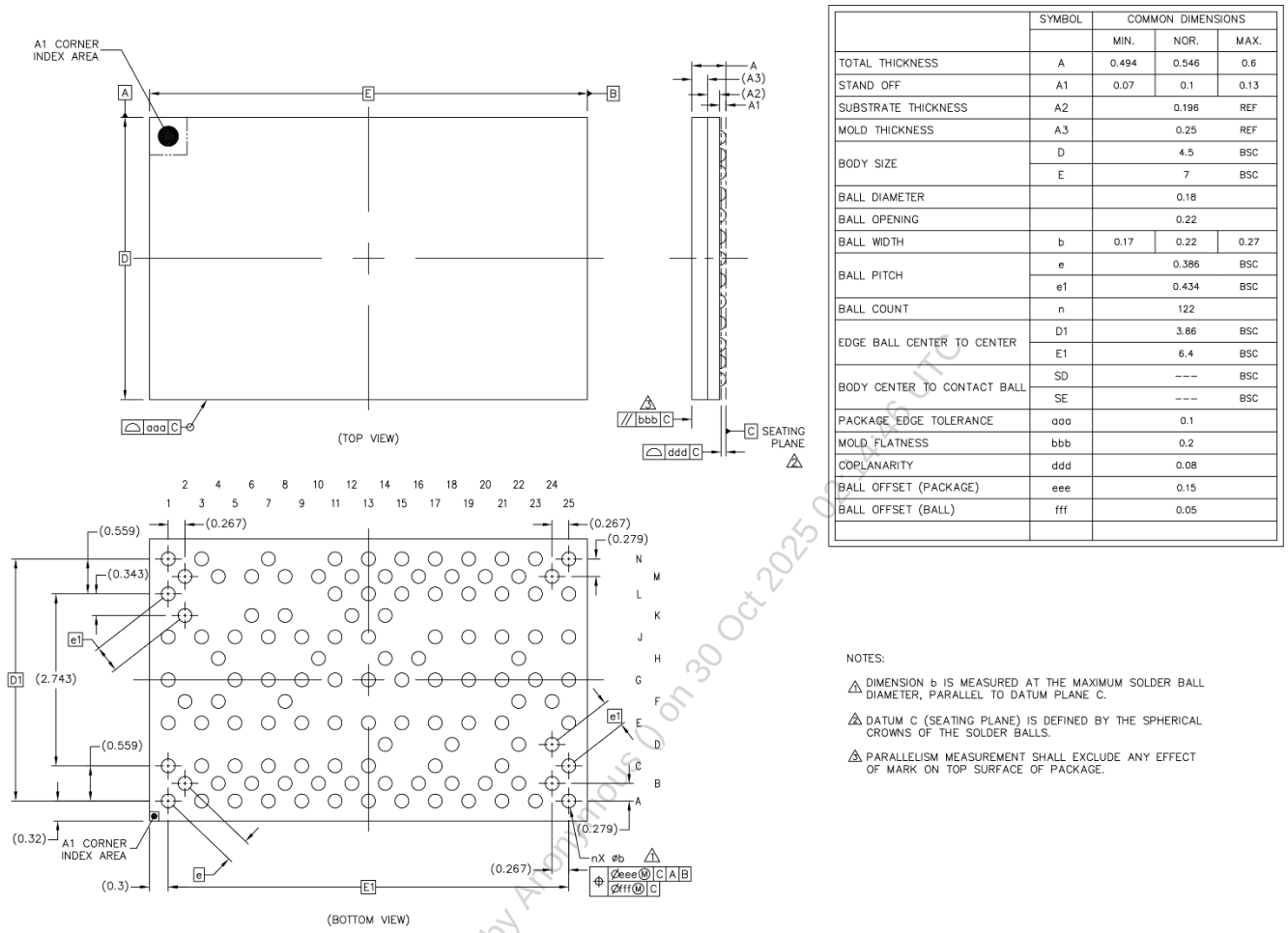


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.435	0.46	0.485
STAND OFF		A1	0.14	---	0.18
WAFER THICKNESS		A2	0.285	0.3	0.315
FILM THICKNESS		A3	---	---	---
BODY SIZE	X	E	2.6832		
	Y	D	5.2334		
BALL/BUMP PITCH	X	SE	---		BSC
	Y	SD	---		BSC
EDGE BALL CENTER TO CENTER	X	E1	2.2		BSC
	Y	D1	4.6683		BSC
PITCH		e	0.4		BSC
		e1	0.7182		BSC
BALL DIAMETER (SIZE)			0.2		
BALL/BUMP WIDTH		b	0.19	---	0.25
BALL/BUMP COUNT		n	84		
PACKAGE EDGE TOLERANCE		aaa	0.03		
WAFER FLATNESS		bbb	0.06		
COPLANARITY		ccc	0.05		
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015		

Figure 19. WLCSP-84 package drawing

7.2. FCCSP-122 Package

Figure 20 illustrates the FCCSP-122 package drawing.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.494	0.546	0.6
STAND OFF	A1	0.07	0.1	0.13
SUBSTRATE THICKNESS	A2		0.196	REF
MOLD THICKNESS	A3		0.25	REF
BODY SIZE	D		4.5	BSC
	E		7	BSC
BALL DIAMETER			0.18	
BALL OPENING			0.22	
BALL WIDTH	b	0.17	0.22	0.27
BALL PITCH	e		0.386	BSC
	e1		0.434	BSC
BALL COUNT	n		122	
EDGE BALL CENTER TO CENTER	D1		3.86	BSC
	E1		6.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.05	

Figure 20. FCCSP-122 package drawing

8. Part Order Numbering / Package Marking

8.1. Part Order Numbering

Table 33 lists the SR100 Series part numbers and their corresponding applications.

Table 33. SR100 Series Part Order Options

Product Name	Applications	Cores	Package Type	Part Number[1]
SR110 ULP, dual core, audio & vision microprocessor	Audio & vision tiered inferencing, smart appliances, home control and automation, security sensors, robotics	M55, Helium DSP, Ethos U55 NPU, M4, uNPU, ISP, JPEG, Vision & audio always-on sensing	FCCSP-122	SR110B0-BA0000-A000-T/R
				SR110B0-BA0000-H000-R
				SR110B0-BA0000-T000-R
			WLCSP-84	SR110B1-WA0000-A000-R
				SR110B1-WA000-H000-R
				SR110B1-WA000-T000-R
SR105 Single core AI microprocessor	High-performance compute & AI, audio processing. advanced IoT sensors, metering, portable speakers, appliances	M55, Helium DSP, Ethos U55 NPU	FCCSP-122	SR105B0-BA0000-H000-R
				SR105B0-BA0000-T000-R
			WLCSP-84	SR105B1-WA0000-H000-R
				SR105B1-WA0000-T000-R
SR102 Single core microprocessor	Connectivity modules, IoT sensors	M55, Helium DSP	FCCSP-122	SR102B0-BA0000-H000-R
				SR102B0-BA0000-T000-R
			WLCSP-84	SR102B1-WA0000-H000-R
				SR102B1-WA0000-T000-R

1.T=Tray, R=Tape & Reel

8.2. Package Marking

Figure 21 illustrates a sample package marking and Pin 1 location for an SR100 Series device.

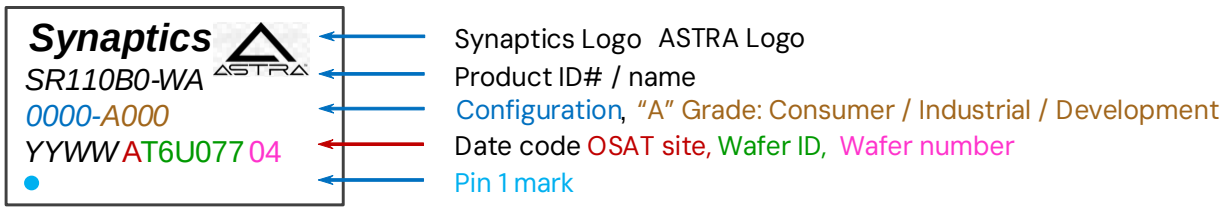


Figure 21. Package Marking and Pin 1 Location

8.3. Part Number Decoder

The following examples illustrate part numbers and their decoding process.

Example 1: SR110B0-BA0000-A000

Example 2: SR110B1-WA0000-A000

SR110: Chip name
B0: Revision name
BA: Package type: FCCSP122
WA: Package type: WLCSP84
0000: Configuration, reserved for future
A000: Full feature engineering sample part
H000: Industrial part
T000: Consumer part

Note: The same decoding method applies to all SR105/102 part numbers.

9. References

The following documents provide reference specifications and standards relevant to the SR100 Series:

- MIPI D-PHY Specification v2
- JESD79-3E Standard
- JEDEC 79-3F and JEDEC 79-3-1A.01 Standard
- JESD209-4A Standard
- JEDEC Standard No. 84-B51

10. Revision History

Revision	Description
1	Initial release.
2	• Updated from SR100 to SR1xx. • Added BGA to Packaging. • Updated Table 1. SR100 Series Chipset Feature Summary. • Added section 2.2 SR100 Series FCCSP Ball-out. • Updated Table 3. Signal Descriptions. • Added BGA to Table 4. Ball Assignment. • Updated VBAT values in Table 7. Recommended Operating Conditions. • Updated Table 11. Digital Operating Conditions for 1.8V I/Os. • Added Figure 20. FCCSP-122 package drawing. • Added Figure 21. Package Marking and Pin 1 Location.
3	• Added ALT5 column to Table 4. Ball Assignment. • Updated 'TBDs' with actual values in Table 7. Recommended Operating Conditions.
4	Updates to the following: • Figure 2. SR100 Series WLCSP top view • Figure 3. SR100 Series FCCSP top view • Table 4. Ball Assignment

5	Changed SR1xx to SR100 Series and updated the following:
	• Description and Features
	• Table 4. Ball Assignment
	• System Description
	• Figure 4. SR100 Series block diagram
	• VBAT voltage requirements in:
	  ○ Table 5. PMU Voltage Domain Breakdown
	  ○ Table 7. Recommended Operating Conditions
	  ○ Figure 9. SR100 Series power diagram
	• Ordering Information
	  ○ Part Number Decoder

Revision	Description
A	Release to production.
B	Updated the following: • Differentiate between Industrial and Consumer in Table 7. Recommended Operating Conditions. • Added part numbers to Table 33. SR100 Series Part Order Options • Updated H000 / T000 in Section 8.3 (Part Number Decoder)
C	Updated Figure 1. SR100 Series block diagram.

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