Application Note

Guidelines for Soldering Surface Mount Devices to PC Boards

Abstract: This document outlines best practices for soldering surface mount devices (SMDs) to PCBs, including reflow profile guidelines, moisture sensitivity management, and land pattern design. The recommendations, based on JEDEC standards, support reliable assembly and performance of Synaptics SoCs.

Contents

1. Introduction

Surface mount devices (SMDs) have replaced older thru-hole device technology in most applications. SMDs help to enable smaller, thinner, lighter, and lower cost devices and printed circuit boards (PCBs). Some applications can also use SMD mounting on both sides of the PCB, further contributing to smaller area and lower cost at the board level.

Since SMD solder reflow heating occurs on the same side of the PCB as the devices, SMDs can be exposed to more heating than older thru-hole devices on boards that were heated from the bottom side (opposite the component side). The widespread adoption of Pb-free SMDs that are reflowed at higher temperatures than older tin/lead (Sn/Pb) SMDs has further added to device heat exposure. Although Synaptics' SMDs use materials, designs, and reliability qualification procedures that ensure consistent performance, care must be taken not to exceed the temperature classifications and floor life for which each SMD is qualified. These and other solder reflow and mounting considerations are discussed in more detail in this document.

Note: Unless otherwise specified, the soldering/reflow guidelines in this document apply to all Synaptics SoCs in surface-mount packages. JEDEC tables (Tables 2 & 3) remain device-agnostic. Device-specific subsections (e.g., SL2610) provide validated examples, not unique limits.

2. Guidelines

2.1. Thru-hole Device versus Surface Mount Device Technology

- Thru-hole device bodies see lower heat exposure than their leads during soldering. Solder reflow heating from the backside of the PCB helps insulate the body (on the board top side) from the temperature extremes of soldering.
- Surface mount devices (SMDs) see more direct heat exposure because solder reflow heating happens on the same side of the PCB as the devices that are mounted. Therefore, care must be taken not to exceed the "Peak Package Body Temperature" noted on the "Moisture Sensitivity Labels" (as on Tape and Reel packing labels).

2.2. Tin/Lead versus Lead-free Soldering

Tin/Lead (Sn/Pb):

- The solder melt temperature is 183 °C.
- Maximum allowable device body temperature during solder reflow is 240 °C for smaller devices and 225 °C for larger/thicker devices (per JEDEC J-STD-020C and
- Table 2 in this application note).

Lead-free (Pb-free):

- The solder melt temperature is 217 °C (34 °C higher than Sn/Pb).
- Maximum allowable device body temperature during solder reflow is 260 °C for smaller devices and 250 °C or 245 °C for larger/thicker devices (per JEDEC J-STD-020C and
- Table 2 in this application note).
- Devices are subjected to increased thermo-mechanical stress due to the higher peak reflow temperatures required for proper solder reflow.
- The real "trick" with implementing Pb-free devices is not just removing the Pb, but rather ensuring the devices are meticulously designed and proven (qualified) to withstand the higher temperatures to which they will be subjected during board mount.
- Synaptics Pb-free devices use material sets, designs, and reliability qualification procedures that ensure this capability.

2.3. Forward Compatibility

Forward compatibility refers to whether or not older Sn/Pb packages can be used with newer, higher temperature Pb-Free board mount reflow processes.

- **Lead-frame type Sn/Pb packages:** Not forward compatible.
- **Ball grid array (BGA) Sn/Pb packages:** Not forward compatible.
  - Why Not?
    - Lead-frame type components have a pre-plated Sn/Pb lead finish, and BGA devices have pre-attached Sn/Pb solder balls, which are not intended for use with higher temperature Pb-free board mount reflow processes.
    - Sn/Pb based components, including the various material sets used in package construction, are reliability-qualified for the lower peak reflow temperature exposures of Sn/Pb board mount processes. They are not qualified to withstand the higher Pb-free reflow temperatures, and thermal cycle fatigue life can be significantly reduced when mixing Sn/Pb and Pb-free solders.

2.4. Backward Compatibility

Backward compatibility refers to whether or not newer Pb-Free packages can be used with older, lower temperature SN/Pb board mount reflow processes.

- **Lead-frame type Pb-free packages:** Are backward compatible.
  - Why?
    - Terminals are typically coated with 100% tin plating, which is compatible with both older Sn/Pb and newer Pb-free solders and board mount reflow processes.
    - Therefore, lead-frame type Pb-free components can be attached to a PCB using Sn/Pb solder paste with a Sn/Pb solder profile.
- **Ball Grid Array (BGA) type packages:** Not backward compatible.
  - Why Not?
    - Pb-free BGAs have pre-applied solder balls made from Pb-free solder alloys with higher melt temperatures (~217 °C) than older Sn/Pb balls (~183 °C).
    - These Pb-free solder balls must be exposed to the higher temperature of Pb-free solder reflow profiles to achieve proper ball reflow.

2.5. Surface Mount Reflow Systems and Processes

The most commonly used industry standard technique for mounting SMDs to PC Boards is forced convection reflow. Less commonly used are Focused Infrared (direct radiant heating of components), Vapor Phase Reflow, and Wave soldering.

Forced convection reflow systems employ heaters to heat the working gas (air or nitrogen) in separate furnace zones, and fans to move the gas in large volumes. The heated gas is circulated over the PCB, transferring its heat to the PCB, components, and solder joints, and is then returned for re-heating to the zone "set temperature" (to repeat the cycle). The "forced" nature of the gas flow ensures higher convection film coefficients that transfer energy more efficiently from the gas to the board and component surfaces. The forced convection system therefore leads to more uniform heating across the board, and more uniform temperature rise and quality of solder joints on components of varying thermal mass and location.

The primary phases of the reflow process are:

1. Evaporate solvents from the solder paste.
2. Activate the flux and allow fluxing action to occur.
3. Pre-heat the components and PC board.
4. Melt the solder and allow proper wetting to occur.
5. Cool the soldered assembly.

2.6. Solder Reflow Profile Development

2.6.1. Reflow Profile Considerations

- **Ramp Rate:** To avoid excessive thermo-mechanical stress on sensitive components, the maximum ramp (heating) rate should be controlled.
- **Preheat Zone:** PCB temperature should be maintained in a preheat zone prior to the final ramp-up past the solder melt temperature. This control helps equalize temperature distribution among the solder joints of the various components.
- **Time above Solder Melting Point:** The solder at the joint should be kept above its melting point for sufficient time to flow and to wet the lands and the leads. Extended duration above the solder melting point may damage the board and sensitive components or allow excessive joint inter-metallic growth that can decrease joint reliability. This value should be minimized but should be sufficient to allow for good solder joint formation across the mix of components on the PCB.
- **Peak Reflow Temperature:** The peak temperature of the solder joint should be just high enough for adequate flux action and solder flow to obtain good wetting on all joints across the mix of components on the PCB. Each component's body also should not exceed the qualified "Peak Package Body Temperature" classifications noted on Moisture Sensitivity Labels of packing materials (Tape and Reel packing labels). In general, these temperatures are based on the "Peak/Classification Temperatures" used during device Reliability Qualification per JEDEC J-STD- 020C. These vary for Sn/Pb and Pb-free and by body size and thickness.
- **Cool-down Rate:** The cool-down rate of the solder joint after reflow is important because the faster the cooling rate, the smaller the grain size of the solder, and the higher the fatigue resistance. However, care should be taken to avoid an excessive temperature gradient resulting in potential damage due to thermo-mechanical stress.

2.7. Solder Reflow Profile Guidelines

The profiles and limits in this section follow JEDEC J-STD-020 and are intended for all Synaptics SoCs. Where a device has been validated with a measured production profile, it is included as a device example; when present, the device datasheet always takes precedence over this application note

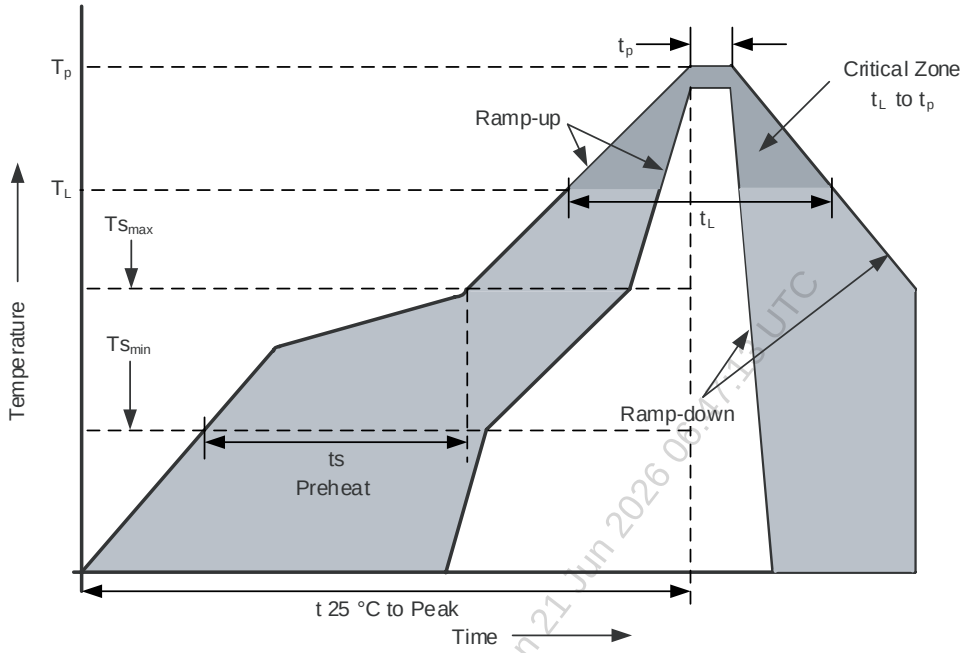

Figure 1. Reflow profile graphic

Table 1. Reflow profile parameter guidelines

Profile Feature	Sn/Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (Ts_{max} to T_p)	3 °C/second maximum	3 °C/second maximum
Preheat: temperature Min (Ts_{min}) Temperature maximum (Ts_{max}) Time (Ts_{min} to Ts_{max})	100 °C 150 °C 60 - 120 seconds	150 °C 200 °C 60 - 180 seconds
Time maintained above: -Temp (T_L) -Time (t_L)	 183 °C 60 - 150 seconds	 217 °C 60 - 150 seconds
Maximum Peak Temp (T_p)	See Table 2	See Note SL2610 mapping (Sn/Pb example): A = 1.31 mm ⇒ use <2.5 mm row; V ≈ 204 mm³ (<350 mm³) ⇒ Tp(max) = 240 °C Table 3
Time within 5 °C of actual peak temperature (t_p)	10 - 30 seconds	20 - 40 seconds
Ramp-down rate	6 °C/second maximum	6 °C/second maximum
Time 25 °C to peak temperature	6 minutes maximum	8 minutes maximum

Note: All temperatures refer to the topside of the package, measured on the package body surface.

Table 2. Sn/Pb eutectic process - maximum peak temperature (T_p)

Package Thickness	Volume, <350 mm^3	Volume, >350 mm^3
<2.5 mm	240 °C	225 °C
≥2.5 mm	225 °C	225 °C

Note SL2610 mapping (Sn/Pb example): A = 1.31 mm ⇒ use <2.5 mm row; V ≈ 204 mm³ (<350 mm³) ⇒ Tp(max) = 240 °C

Table 3. Pb-free process - maximum peak temperature (T_p)

Package Thickness	Volume, <350 mm^3	Volume, 350-2000 mm^3	Volume, >2000 mm^3
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

To limit voiding and to optimize the profile and peak temperature for the flux formulation, the profile recommendations of the specific solder paste manufacturer should be followed. The peak temperature should be minimized. Use the lowest peak temperature needed to maintain good solder joint wetting across the mix of components on each particular PCB.

Note SL2610 mapping (example): A = 1.31 mm nominal (JEDEC <1.6 mm row); body volume V ≈ 204 mm³ (<350 mm³). Validated profile: peak Tp = 232 °C; time above liquidus (TAL, ≥217 °C) ≈ 78 s.

2.8. Moisture Sensitivity Level Ratings

All plastic packages absorb moisture. If not managed properly, damage can occur during the solder reflow process due to internal package cracking or delamination between internal package interfaces. The root cause of this failure mechanism is the rapid heating of the moisture absorbed within the plastic. During typical solder reflow operations, devices are exposed to a rapid change in ambient temperature. Any absorbed moisture is quickly turned into superheated steam. This sudden change in vapor pressure can cause the package to swell. If the pressure exerted exceeds the flexural strength of the plastic mold compound, then it is possible to crack the package.

To ensure proper performance, Synaptics bakes and packs devices for shipment per industry standards and assigns a moisture sensitivity level (MSL) rating dependent on each device's sensitivity to moisture. For each MSL rating, which is displayed on product shipment labels, a specific "floor life" is allowed. Floor life is the maximum allowable time period between the removal of devices from a moisture barrier bag (or dry storage) and the start of the solder reflow process. If the floor life is exceeded, the devices must be re-baked before use.

Table 4. Moisture sensitivity level and floor life

Level	Floor Life	
	Conditions	Time[1]
1	≤ 30 °C/85% RH	Unlimited[2]
2	≤ 30 °C/60% RH	1 year
2A	≤ 30 °C/60% RH	4 weeks
3	≤ 30 °C/60% RH	168 hours
4	≤ 30 °C/60% RH	72 hours
5	≤ 30 °C/60% RH	48 hours
5A	≤ 30 °C/60% RH	24 hours
6	≤ 30 °C/60% RH	Bake before use

1. Time after removing from dry pack in a ≤ 30 °C / 60% RH ambient.
2. Dry pack not required for MSL level 1. Maximum conditions 30 °C / 85% RH.

For further information, refer to:

- IPC/JEDEC J-STD-033-D Joint Industry Standard, "*Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices*."

2.9. PC Board Material and Surface Finish

Board Material

The main consideration is that for higher temperature Pb-free reflow, a board material with a glass transition (Tg) temperature greater than 170 °C is recommended, for plated thru-hole reliability reasons.

Surface Finish

The most common types are:

- Organic solderability preservative (OSP)
- Electroless nickel / immersion gold (ENIG)
- Immersion gold (Au)
- Immersion silver (Ag)
- Immersion tin (Sn)

Suitability of any particular finish depends on the requirements of the reflow process and assembly house, PCB design, cost, and handling and storage considerations.

2.10. PC Board Land Pattern Design Considerations

Major industry Land Pattern standards:

- IPC-SM-782: "*Surface Mount Design and Land Pattern Standard*" (1987).
- IPC-7351: "*Generic Requirements for Surface Mount Design and Land Pattern Standards*" (2005 - Successor to IPC-SM-782).

These are good references for land pattern design across a broad variety of SMD components.

2.11. Solder Mask Design

Sn/Pb versus Pb-free: The PCB footprint design does not need to change for Pb- free assembly. The same pad size and solder mask opening can be used for SnPb or Pb-free processes.

Types of land patterns: Two types are used for surface mount components (refer to Figure 2):

- Non-solder mask defined (NSMD): Solder mask openings larger than metal pads.
- Solder mask defined (SMD): Solder mask openings smaller than metal pads.

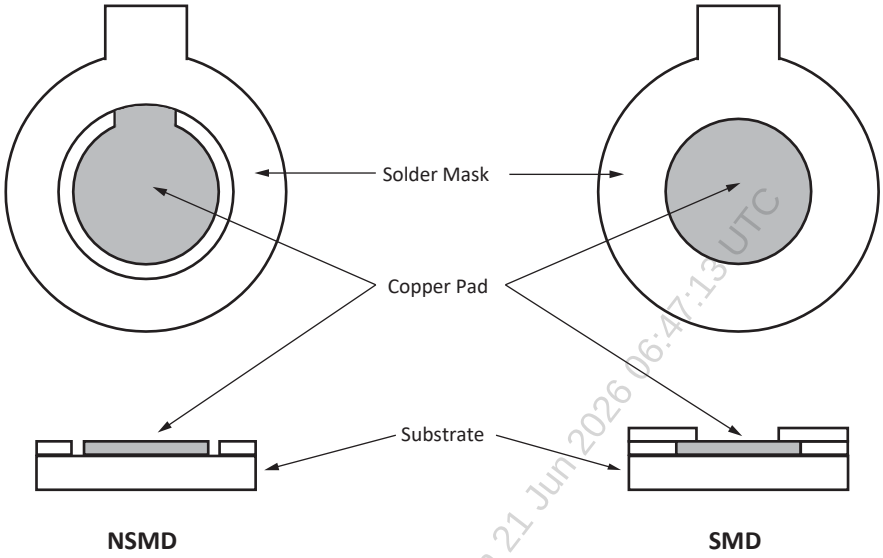

Figure 2. NSMD versus SMD land pad

Better control of the copper etching process as compared to the solder masking process makes NSMD preferable. Also, the SMD pad definition can introduce stress concentrations near the solder mask overlap region that can result in solder joints cracking under extreme fatigue conditions. Using NSMD instead improves the reliability of solder joints as solder is allowed to “wrap around” the sides of the metal pads on the board. For these reasons, NSMD is recommended.

2.12. PC Board Land Pad Design for Ball Grid Arrays

Ball Pad Design: The NSMD type is recommended, with feature size guidelines per Table 5.

Table 5. Guidelines for BGA land pad and opening feature sizes

NSMD Feature		BGA Ball Pitch			
	1.27 mm	1.0 mm	0.8 mm	0.5 mm	0.4 mm
Copper pad diameter	0.61 mm (~24 mils)	0.45 mm (~18 mils)	0.35 mm (~14 mils)	0.28 mm (~11 mils)	0.254 mm (10 mils)
NSMD solder mask opening diameter	0.76 mm (~30 mils)	0.61 mm (~24 mils)	0.48 mm (~19 mils)	0.40 mm (~16 mils)	0.254mm (10 mils)

These values are guidelines only and can be adjusted to accommodate specific PCB design needs. These needs can vary depending on the number of lines between balls, line/space sizes used, solder mask alignment tolerance rules used. Note that via-in-pad technology is often used on PCBs for 0.5 mm pitch BGAs because this negates the need for any fine line escape routing between balls.

Trace (line) exiting the ball pad: The width of the trace metal exiting NSMD pad metal should be less than half of the pad metal diameter. Wider traces increase metal contact area resulting in lower standoff height, which could affect reliability. For pads with particularly small diameters of ~0.3 mm (12 mil) or less, use a ~0.10 mm (4 mil) trace width.

2.13. PC Board Land Pad Design for Quad Flat Packages (LQFP, TQFP)

Peripheral I/O Lands: The I/O lands should be larger on all sides than the package's lead foot. Land pad metal design guidelines are shown in Table 6. The NSMD solder mask opening type should be used.

Table 6. Guidelines for quad flat package land pad sizes

Package Lead Pitch	Metal Land Pad Size
0.80 mm	0.39 x 1.40 mm
0.65 mm	0.34 x 1.40 mm
0.50 mm	0.26 x 1.40 mm
0.40 mm	0.22 x 1.40 mm

Exposed Paddle (Thermal) Land: The exposed paddle, on packages containing one, should be soldered down so that its potential to efficiently transfer heat to the PCB can be realized. The board should also include thermal vias below the thermal land, dropping to a plane (sized as large as feasible) for heat spreading. The thermal land should be about 0.3 mm larger than the exposed die paddle. The recommended solder mask opening type is NSMD.

2.14. PC Board Land Pad Design for Quad Flat No-lead Packages

Due to the newer nature of quad flat no-leads (QFNs), with fewer industry land pattern references, Synaptics has developed a much more extensive document to assist in this area for QFNs. Refer to *PCB Land Pattern Design and Surface Mount Guidelines for QFN (MLFP) Packages* (PN: 506-000921-01).

2.15. Stencil Design Guidelines

2.15.1. Stencil Type and Thickness

A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended. Electro-polishing "smooths" aperture walls, resulting in reduced surface friction, good paste release and void reduction. Using a trapezoidal section aperture (TSA) promotes paste release and forms "brick-like" paste deposits that assist in firm component placement. A 0.125 mm stencil thickness is recommended for finer pitch packages (0.5 mm and smaller), and this may be increased to 0.15 mm to 0.2 mm thickness for greater than 0.5 mm pitch packages.

2.15.2. Stencil Design for I/O Lands

Stencil aperture-to-land size should typically be a 1:1 ratio. For finer pitch parts, especially as tight as 0.4 mm, the aperture width may need to be reduced slightly to help prevent solder bridging between adjacent I/O lands.

2.15.3. Stencil Design for Thermal Land (for "Exposed Pad" Type Packages)

To reduce solder paste volume on the thermal land, an array of smaller apertures should be used instead of one large aperture. The apertures can be circular or square and of various dimensions and array sizes, but the main goal should be a dimensional combination that results in about 50 to 80% solder paste coverage.

The reduced paste volume provides paths for out-gassing and helps regulate joint thicknesses and improve reliability of the perimeter I/O solder joints. Too much solder on the thermal land can cause devices to "float," the result being too much gap between the device's leads or terminals and the PCB's I/O lands.

3. Revision History

Last Modified	Revision	Description
January 2024	A	Initial release.
May 2024	B	Release as public document.
September 2025	C	Updated Introduction and Solder Reflow Profile Guidelines

Contact Us

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