Astra SL1620 Embedded IoT Processor

Electrical Specification Datasheet

Overview

The Synaptics® SL-Series of embedded processors are highly integrated AI-native Linux® and Android™ systems on chip (SoCs) optimized for multi-modal consumer, enterprise, and industrial IoT workloads with hardware accelerators for edge inferencing, security, video, graphics, and audio. The SL1620 is designed and optimized for embedded applications that require powerful processing, advanced AI capability, and 3D graphics. This chip comes with Linux® OS, superior audio algorithms, a variety of peripherals, dual displays, companion Synaptics SoC for connectivity and audio front end.

The SL1620 incorporates high-performance compute engines, including a quad-core Arm® Cortex®-A55 CPU subsystem, a high-efficiency, feature-rich GPU for advanced graphics and AI acceleration, superior audio algorithms, and dual displays.

The SL1620 supports the Synaptics Astra™ IoT platform, delivering a unified experience through standards-based approaches, open software frameworks, full-featured AI toolkits, and market-ready evaluation systems.

In combination with Synaptics' best-in-class wireless connectivity portfolio, the SL1620 enables cost-optimized system solutions with performance-per-watt benefits for the IoT.

Contents

List of Tables

List of Figures

1. Block Diagram

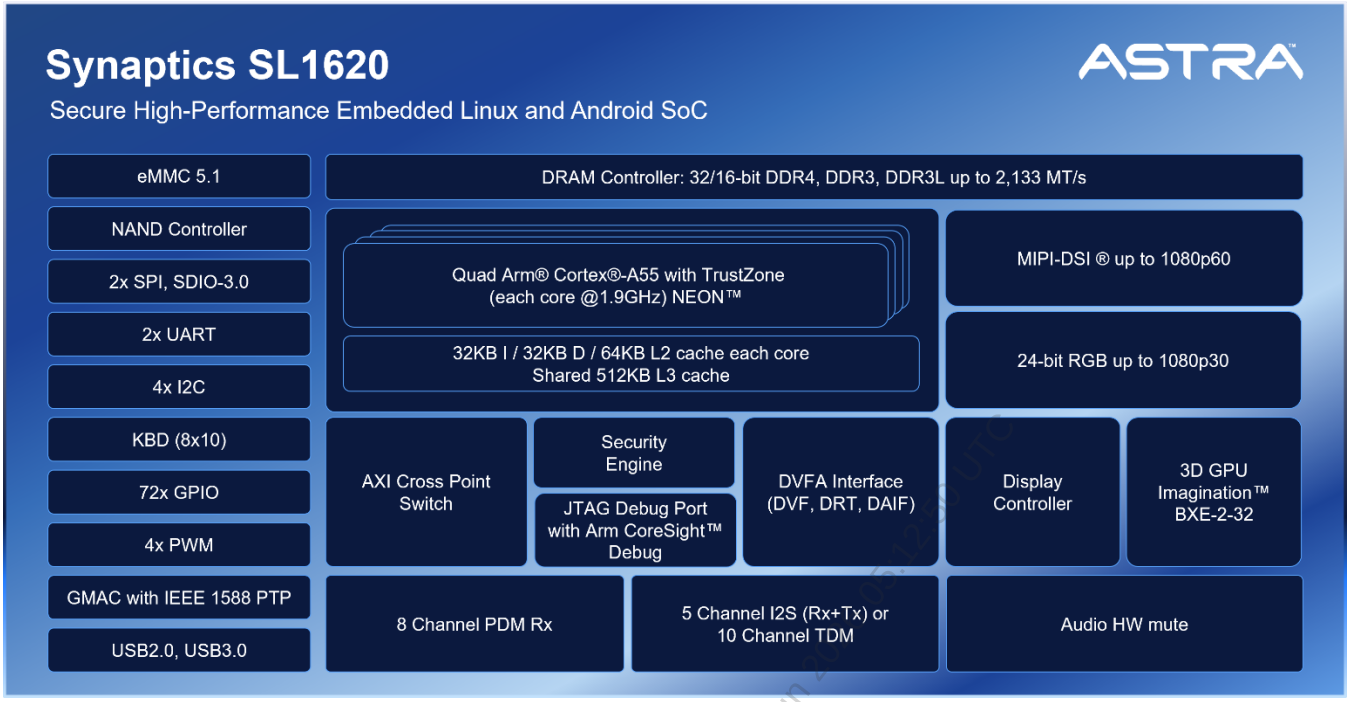


Figure 1. Astra SL1620 high-level block diagram

2. Features

2.1. CPU

- Quad-core Arm® Cortex®-A55 processor
- Up to 1.9GHz for each CPU core
  - Support for power-gating individual cores and dynamic voltage and frequency scaling
- Each processor has 32KB I-Cache / 32KB D-Cache, 64KB L2 Cache; all cores share 512KB L3 cache
- Each processor has dedicated NEON™ technology/FPU
- Arm® CoreSight™ technology-compatible debugging interface
- TrustZone® technology
- Supports standard tool chains (ARM, GNU)

2.2. Security

- Completely firewalled secure CPU
- Secure boot with RSA digital signature verification from eMMC/NAND
- On-chip 32Kbit anti-fuse OTP
- True random number generator
- DRM engine supports
  - AES, DES, 3DES, SHA1/SHA2/MD5, RSA, ECC
- Disable / enable JTAG through authentication
- Memory and I/O space access control

2.3. GPU

- Imagination™ BXE-2-32
- Dual core (2 pixels per clock)
- Clock frequency up to 800 MHz
- Supports OpenGL® ES™ 3.2, OpenCL™ 3.0, EGL™ 1.5, Vulkan® 1.3, Android™ NN API through IMGDNN AP

2.4. Memory Interface

- DRAM controller
  - 32-bit DDR3/DDR3L-1866 / DDR4-2133
    - 16-bit memory configuration supported
- Up to 4 GB memory space (32-bit configuration)
- Supports out-of-order issue of transactions to maximize DRAM utilization rate
- Secure control based on Arm® TrustZone® technology
- NAND controller
  - 8-bit Parallel NAND IF support only
  - SLC (64-bit ECC per 2KB of data)
- eMMC 5.1 Controller
  - x1, x4, or x8-bit interface

2.5. Video/Display Interfaces

- Dual display
  - simultaneously supports dual display with different contents
- MIPI DSI®
  - MIPI Display Serial Interface (DSI) with 4-lane DPHY, supports LP and HS modes
  - Up to 1080p60 screen resolution and refresh rate
- RGB
  - Digital Parallel Interface (DPI)
  - CPU-type Display Bus Interface (DBI)
  - RGB 16bpp (565), 18bpp (666) and 24bpp (888) output formats
  - Up to 1080p30 screen resolution and refresh rate

2.6. Audio

- Interface for DVFA101 support
- TDM/I²S – 5 fully bidirectional interfaces with up to 16 channels each
  - Support of sample frequencies from 8 to 96/192/384 kHz and slot size 8/16/24/32 bit
  - Usage of sample frequency 192 kHz limits the TDM interface to 8 channels
- Supports input of external MCLK to the audio subsystem or generates internally MCLK output for external codec
- Supports up to 8 digital microphones – 4 PDM stereo interfaces
- Dedicated audio DMA with support for TDM/I²S/PDM and DVFA audio
- HW mute – support disable of local audio sources by a dedicated HW input pin

2.7. Peripherals

- One USB 3.0 Host
- One USB 2.0 On-The-Go (OTG) interface
- One SDIO 3.0 port, up to 200 MHz
  - single data rate (SDR104), 1.8V-only
- Four TWSI 2-wire buses (I²C compatible)
- Two high-speed UART interfaces
- Two SPI controllers
  - Up to four target devices supported on each interface
- 72-bit pin-shared GPIOs
- Rectangular Keyboard matrix controller up to 80 keys (8x10)
- 4 PWMs
- On-chip temperature sensor

2.8. Boot Options

- NAND Flash, eMMC, SPI, USB OTG (device mode)

2.9. Ethernet

- 802.3 (G)MAC supports RGMII and RMII
  - 802.1 p/q tagging (VLAN) in hardware
  - IEEE 1588 Precision Time Protocol (PTP) with PPS output signal

2.10. JTAG

- CoreSight™ Debug
- Boundary scan support

2.11. Power Saving

- Power gating for each A55 core
- Support DDR self-refresh

2.12. Package and Layout

- Package:
  - 13mm x 13mm FCBGA, 0.4mm ball pitch
  - Ball pattern allows standard PCB fab rules, (no HDI rules required)

2.13. Related Content

Part Number	Document Title
506-001443-01	Synaptics General Guide for Soldering SMD to PC Boards Application Note
506-001454-01	Synaptics General ESD/EOS Control Methods Application

3. Signal Description

Note: This document is preliminary and subject to change.

Table 1. Pin Type Definitions

Pin Type	Definitions
I	Input only
O	Output only
I/O	Input and output
Analog	Analog Pin
CMOS	Complementary metal oxide semiconductor
SSTL	Stub Series Terminated Logic
PWR	Power Supply
GND	Ground Pin
Iu	Input with internal pull-up
Id	Input with internal pull-down
I/Ood	Input/Output pin, Open-Drain type
I/Ouod	Input/Output pin with internal pull-up, Open-Drain type
I/Odod	Input/Output pin with internal pull-down, Open-Drain type
Ouod	Output pin with internal pull-up, Open-Drain type
Ou	Output pin with internal pull-up

Note: A lowercase n at the end of a signal name indicates an active-low signal.

Table 2. Interface Prefixes

Pin Type	Definitions
DDR4/DDR3/DDR3L memory channel 0	M0_
eMMC	EMMC_
I^2S	I2S1_, I2S2_, I2S3_,I2S4_,I2S5_
PDM	PDM_
SDIO	SDIO_
SPI	SPI1_, SPI2_
TWSI	TW0_, TW1_, TW2_, TW3_
UART	URT0_, URT1_
USB 2.0	USB2_
USB 3.0	USB3_
Power for digital domain	VDD_
Power for analog domain	AVDD_, AVDD2_
Ground for analog domain	AVSS_

3.1. Pinout

This section is preliminary and subject to change.

Note: Due to the large number of pins, the package is depicted graphically over several pages (Figure 2 through Figure 7).

	1	2	3	4	5	6	7	8	9	10	11	
A	VSS	VSS			M0_RSTn	VSS	VDD_CORE_FB	TW0_SCL		FORCE_MUTE		A
B	VSS	VSS		M0_A[11]	M0_NC	VSS		TW0_SDA	POR_EN	TEST_EN	JTAG_SEL	B
C	M0_A[9]	M0_BG	M0_BA[0]	M0_A[0]	VSS	CPUPLL_AVDD1P8		TW1_SCL		VSS	TCK	C
D		M0_BA[1]	M0_ACTn	VSS		CPUTSEN_AVDD1P8		VSS		VSS		D
E												E
F	M0_WEn	M0_A[7]	M0_A[6]	M0_A[8]		VSS		TW1_SDA		RSTIn		F
G		M0_A[5]										G
H	M0_CASn	M0_A[4]	M0_A[13]	VSS		M0_A[1]	VSS	VSS		VSS		H
J		M0_CKE	M0_A[3]									J
K			M0_A[12]	VSS		M0_A[2]	M0_A[10]					K
L	M0_RASn	M0_ODT							VSS	VDDQ		L
M		M0_CSn	M0_CKp	M0_CKn		VSS	M0_CAL					M
N	VSS	M0_DQSn[0]						VSS	VSS	VDDQ		N
P		M0_DQSp[0]	VSS	M0_DQ[4]		M0_DQ[6]	VSS			VSS		P
R		M0_DQ[7]										R
T	M0_DQ[1]	M0_DQ[3]		VSS		M0_DQ[0]	VSS		VSS	VSS		T
U		M0_DQ[5]	M0_DQ[2]	VSS		M0_DQ[8]	VSS					U
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. (Top View 1 of 6)

Note: Due to the large number of pins, the package is depicted graphically over several pages (see Figure 2 through Figure 7).

	1	2	3	4	5	6	7	8	9	10	11	
V	VSS	M0_DM[0]							VSS	VSS		V
W	M0_DQSp[1]	M0_DQSn[1]	M0_DQ[12]	M0_DQ[14]		M0_DM[1]	M0_DQ[10]					W
Y		M0_DQ[11]							VSS	VSS		Y
AA	M0_DQ[9]	M0_DQ[13]	VSS	VSS		VSS	VSS					AA
AB		M0_DQ[15]							VSS	VSS		AB
AC	M0_DQSn[2]	M0_DQSp[2]	VSS	M0_DQ[20]		M0_DQ[18]	M0_DQ[22]					AC
AD		M0_DQ[23]	M0_DQ[19]						M0_AVDD1P8	VSS		AD
AE			M0_DQ[21]	M0_DQ[16]		M0_DQ[26]	VSS					AE
AF	M0_DQ[17]	M0_DM[2]						VSS		VSS		AF
AG		VSS	VSS	M0_DQ[28]		VSS		VSS		VSS		AG
AH	M0_DQSp[3]	M0_DQ[24]										AH
AJ	M0_DQSn[3]	M0_DQ[27]	M0_DQ[30]	VSS		MIPI_DSI_AVDD		MIPI_DSI_AVDD1P8		VSS		AJ
AK		M0_DM[3]				VSS		VSS				AK
AL	VSS	VSS	M0_DQ[25]	M0_DQ[29]	VSS	MIPI_DSI_D0n		MIPI_DSI_D1p	MIPI_DSI_CKn	VSS	MIPI_DSI_D2p	AL
AM	VSS	VSS		M0_DQ[31]	MIPI_DSI_REXT	MIPI_DSI_D0p		MIPI_DSI_D1n	MIPI_DSI_CKp		MIPI_DSI_D2n	AM
	1	2	3	4	5	6	7	8	9	10	11	

Figure 3. (Top View 2 of 6)

Note: Due to the large number of pins, the package is depicted graphically over several pages (see Figure 2 through Figure 7).

	12	13	14	15	16	17	18	19	20	21	22	
A		VSS		SPI1_SSOn			TW2_SDA		SPI2_SCLK			A
B		TDI	TDO	SPI1_SS3n	SPI1_SDO		SPI2_SS1N	SPI2_SDO	SPI2_SDI	TW3_SCL		B
C	TMS		VSS		SPI1_SCLK	TW2_SCL		VSS		TW3_SDA	URT1_RXD	C
D	TRSTn		SPI1_SS1n		VSS	SPI1_SDI		SPI2_SS2n		VSS		D
E												E
F	VSS		SPI1_SS2n		VSS	VSS		SPI2_SSOn		SPI2_SS3n		F
G										VSS		G
H	VSS		VSS		VSS	VSS		VSS		VDDIO1P8		H
J												J
K	VSS		VSS		VDDIO1P8		VDDIO1P8		VSS		VDDIO1P8	K
L	VSS	VDD_CORE	VSS		VSS		VSS		VDD_CORE	VSS	VSS	L
M					VDDIO1P8		VDDIO1P8					M
N	VDDQ		VDD_CORE		VSS		VDD_CORE		VSS		VDD_CORE	N
P	VDDQ		VDD_CORE		VSS		VDD_CORE		VSS		VDDIO1P8	P
R												R
T	VDDQ		VSS		VDD_CORE		VSS		VDD_CORE		VSS	T
U												U
	12	13	14	15	16	17	18	19	20	21	22	

Figure 4. (Top View 3 of 6)

Note: Due to the large number of pins, the package is depicted graphically over several pages (see Figure 2 through Figure 7).

	12	13	14	15	16	17	18	19	20	21	22	
V	VDDQ		VSS		VDD_CORE		VSS		VDD_CORE		VSS	V
W												W
Y	VDDQ		VDD_CORE		VSS		VDD_CORE		VDD_CORE		VDD_CORE	Y
AA												AA
AB	VSS		VDD_CORE		VSS		VSS		VSS		VDD_CORE	AB
AC												AC
AD	VSS		VDD_CORE		VDD_CORE		VDD_CORE		VDD_CORE		VDD_CORE	AD
AE												AE
AF	VSS		VSS		VSS	VSS		VSS		VSS		AF
AG	USB3_REXT		USB3_DVDD		USB3_ID	USB2_DVDD		VSS		USB2_AVDD3P3		AG
AH												AH
AJ	USB3_AVDD3P3		USB3_AVDD		USB3_VBUS	VSS		USB2_VR_AVDD3P3		VSS		AJ
AK	VSS		VSS			VSS				NAND_DATA[1]	NAND_DATA[0]	AK
AL	MIPI_DSI_D3n		USB3_TXp	USB3_Dn	USB3_Dp	USB3_RXp	USB2_VBUS	USB2_ID	USB2_REXT		NAND_DATA[2]	AL
AM	MIPI_DSI_D3p		USB3_TXn			USB3_RXn	USB2_Dn	USB2_Dp				AM
	12	13	14	15	16	17	18	19	20	21	22	

Figure 5. (Top View 4 of 6)

Note: Due to the large number of pins, the package is depicted graphically over several pages (see Figure 2 through Figure 7).

	23	24	25	26	27	28	29	30	31	32	
A	PWM[0]		PWM[3]			VSS		RGMII_CLK_OUT	VSS	VSS	A
B	PWM[1]	PWM[2]	GPIO_A[2]	GPIO_A[3]		NAND_ALE		NAND_CEn	VSS	VSS	B
C	URT1_TXD		VSS	SDIO_CDn	SDIO_WP			RGMII_TXC			C
D	VSS		GPIO_A[1]		RGMII_TXD[0]		VSS	RGMII_TXD[2]	RGMII_TXD[1]		D
E									RGMII_TXD[3]	VSS	E
F	GPIO_A[0]		USB2_DRV_VBUS		VSS	RGMII_RXC		RGMII_TXCTL	RGMII_RXD[0]		F
G			VSS						RGMII_RXD[1]	RGMII_RXD[2]	G
H	VSS		VDDIO1P8		VSS		VSS	RGMII_RXCTL	RGMII_RXD[3]		H
J									VSS	RCLKI	J
K		VSS		VSS	SYSPLL_AVDD1P8	VSS	OSC_VDDIO1P8		VSS	RCLKO	K
L		VSS							I2S1_LRCK		L
M				I2S1_DO	I2S1_DI	VSS	KILOOTP_AVDD1P8	VSS	I2S1_BCLK	I2S1_MCLK	M
N		VSS							I2S2_LRCK		N
P		VSS		VSS	I2S2_BCLK			I2S2_DO			P
R							PDM_DI[1]	I2S2_DI	I2S3_LRCK	I2S3_DO	R
T		VSS		PDM_CLKIO	PDM_DI[0]				I2S3_BCLK		T
U				VSS	VDDIO1P8		VSS	VSS	LCD_D[0]	I2S3_DI	U
	23	24	25	26	27	28	29	30	31	32	

Figure 6. (Top View 5 of 6)

Note: Due to the large number of pins, the package is depicted graphically over several pages (see Figure 2 through Figure 7).

	23	24	25	26	27	28	29	30	31	32	
V		VSS						LCD_D[2]	LCD_D[1]		V
W				VSS	VDDIO1P8		LCD_D[3]	LCD_D[4]			W
Y		VSS							LCD_D[6]	LCD_D[5]	Y
AA				VSS	AVPLL_AVDD1P8		LCD_D[9]	LCD_D[8]	LCD_D[7]		AA
AB		VSS							LCD_D[11]	LCD_D[10]	AB
AC				LCD_D[14]	LCD_D[13]		VSS	LCD_D[12]			AC
AD		VSS						LCD_D[15]	LCD_D[16]		AD
AE				LCD_D[20]	LCD_D[19]		VSS	LCD_VDDIO3P3	LCD_D[18]	LCD_D[17]	AE
AF	VSS		VSS						LCD_D[21]		AF
AG	NAND_VDDIO1P8		NAND_REn		VSS		LCD_D[23]	LCD_GPIO[0]	LCD_D[22]	LCD_CLK	AG
AH											AH
AJ	VSS		NAND_CLE		SDIO_VDDIO1P8		VSS	LCD_GPIO[1]	LCD_GPIO[2]		AJ
AK	VSS		NAND_DATA[6]		NAND_DATA[7]	VSS			LCD_GPIO[3]	LCD_GPIO[4]	AK
AL	NAND_DATA[3]	NAND_WEn	NAND_DATA[4]		SDIO_CLK	SDIO_DATA[3]	SDIO_DATA[1]	SDIO_DATA[0]	VSS	VSS	AL
AM	NAND_RDY		NAND_DATA[5]		SDIO_CMD		SDIO_DATA[2]		VSS	VSS	AM
	23	24	25	26	27	28	29	30	31	32	

Figure 7. (Top View 6 of 6)

3.2. Pin Descriptions

Table 3. SoC Global and Oscillator/Crystal Interfaces

Pin #	Pin Name	Pin Type	Description
F10	RSTIn	Iu, CMOS	SoC Active low reset input with internal pullup.
C11	TCK	Id, CMOS	JTAG Clock.
D12	TRSTn	Id, CMOS	JTAG Reset.
C12	TMS	Iu, CMOS	JTAG Mode select signal (Arm or chip JTAG).
B13	TDI	Iu, CMOS	JTAG SDATA IN.
B14	TDO	Ou, CMOS	JTAG SDATA OUT.
B10	TEST_EN	Id, CMOS	TEST enable. 0: Enable ARM ICE JTAG connections. 1: Enable SCAN or BSCAN tests.
B11	JTAG_SEL	Id, CMOS	JTAG Port selection. 0: Reserved 1: Enable JTAG
A10	FORCE_MUTE	Id, CMOS	FORCEMUTE selection. 0: No mute. 1: Mute local digital microphones and I2S1,I2S2 and I2S3
B9	POR_EN	Id, CMOS	Power-on reset enable. 0: Bypass on-chip power-on reset generator. 1: Enable on-chip power-on reset generator.
J32	RCLKI	I, Analog	Oscillator/Crystal Input 25 MHz.
K32	RCLKO	I/O, Analog	Crystal inverted output.

Table 4. PWM Interface

Pin #	Pin Name	Pin Type	Description
A23	PWM[0]	O, CMOS	Pulse-Width Modulation output data 0.
B23	PWM[1]	O, CMOS	Pulse-Width Modulation output data 1.
B24	PWM[2]	O, CMOS	Pulse-Width Modulation output data 2.
A25	PWM[3]	O, CMOS	Pulse-Width Modulation output data 3.

Table 5. SPI Interface

Pin #	Pin Name	Pin Type	Description
A15	SPI1_SS0n	O, CMOS	SPI1 chip select 0 for first target device with handler.
D14	SPI1_SS1n	O, CMOS	SPI1 chip select 1 for second target device with handler.
F14	SPI1_SS2n	O, CMOS	SPI1 chip select 2 for third target device.
B15	SPI1_SS3n	O, CMOS	SPI1 chip select 3 for fourth target device.
C16	SPI1_SCLK	O, CMOS	SPI1 serial clock.
D17	SPI1_SDI	I, CMOS	SPI1 serial data input.
B16	SPI1_SDO	I/O, CMOS	SPI1 serial data output.
F19	SPI2_SS0n	O, CMOS	SPI2 chip select 0 for first target device.
B18	SPI2_SS1n	O, CMOS	SPI2 chip select 1 for second target device.
D19	SPI2_SS2n	O, CMOS	SPI2 chip select 2 for second target device.
F21	SPI2_SS3n	O, CMOS	SPI2 chip select 3 for fourth target device.
A20	SPI2_SCLK	O, CMOS	SPI2 serial clock.
B20	SPI2_SDI	I, CMOS	SPI2 serial data input.
B19	SPI2_SDO	I/O, CMOS	SPI2 serial data output.

Table 6. SDIO0 Interface

Pin #	Pin Name	Pin Type	Description
AL30	SDIO_DATA[0]	I/O, CMOS	Data[0]. Busy from card; DI in SPI mode.
AL29	SDIO_DATA[1]	I/O, CMOS	Data[1]. Int from card.
AM29	SDIO_DATA[2]	I/O, CMOS	Data[2]. Read wait from card.
AL28	SDIO_DATA[3]	I/O, CMOS	Data[3]. SSn in SPI mode.
AL27	SDIO_CLK	O, CMOS	Output clock. CLK in SPI mode.
AM27	SDIO_CMD	I/O, CMOS	Command/Response. DO in SPI mode.
C26	SDIO_CDn	I, CMOS	Card Detect. 0 = Detect.
C27	SDIO_WP	I, CMOS	Write Protect. 1 = Write protect.

Table 7. DDR4 Mode 0 Interface Configuration

Pin #	Pin Name	Pin Type	Description
C4	M0_A[0]	O, SSTL12	M0_DDR4_A0.
H6	M0_A[1]	O, SSTL12	M0_DDR4_A1.
K6	M0_A[2]	O, SSTL12	M0_DDR4_A2.
J3	M0_A[3]	O, SSTL12	M0_DDR4_A3.
H2	M0_A[4]	O, SSTL12	M0_DDR4_A4.
G2	M0_A[5]	O, SSTL12	M0_DDR4_A5.
F3	M0_A[6]	O, SSTL12	M0_DDR4_A6.
F2	M0_A[7]	O, SSTL12	M0_DDR4_A7.
F4	M0_A[8]	O, SSTL12	M0_DDR4_A8.
C1	M0_A[9]	O, SSTL12	M0_DDR4_A9.
K7	M0_A[10]	O, SSTL12	M0_DDR4_A10.
B4	M0_A[11]	O, SSTL12	M0_DDR4_A11.
K3	M0_A[12]	O, SSTL12	M0_DDR4_A12.
H3	M0_A[13]	O, SSTL12	M0_DDR4_A13.
D3	M0_ACTn	O, SSTL12	M0_DDR4_ACTn.
C3	M0_BA[0]	O, SSTL12	M0_DDR4 Bank select[0].
D2	M0_BA[1]	O, SSTL12	M0_DDR4 Bank select[1].
C2	M0_BG	O, SSTL12	M0_DDR4 Bank Group.
M7	M0_CAL	I, Analog	DDR4/DDR3/DDR3L Calibration pad. Connect to VSS via a 240 ±1% ohm resistor.
H1	M0_CASn	O, SSTL12	M0_DDR4 Column activate or M0_A[15].
M4	M0_CKn	O, SSTL12	M0_DDR4_CKn for 2 x16 chips.
M3	M0_CKp	O, SSTL12	M0_DDR4_CKp for 2 x16 chips.
J2	M0_CKE	O, SSTL12	M0_DDR4 Clock enable.
M2	M0_CSn	O, SSTL12	M0_DDR4 Chip select.
V2	M0_DM[0]	I/O, POD12	M0_DDR4 Data mask BYTE[0].
W6	M0_DM[1]	I/O, POD12	M0_DDR4 Data mask BYTE[1].
AF2	M0_DM[2]	I/O, POD12	M0_DDR4 Data mask BYTE[2].
AK2	M0_DM[3]	I/O, POD12	M0_DDR4 Data mask BYTE[3].
T6	M0_DQ[0]	I/O, POD12	M0_DDR4_DQ0.
T1	M0_DQ[1]	I/O, POD12	M0_DDR4_DQ1.
U3	M0_DQ[2]	I/O, POD12	M0_DDR4_DQ2.
T2	M0_DQ[3]	I/O, POD12	M0_DDR4_DQ3.
P4	M0_DQ[4]	I/O, POD12	M0_DDR4_DQ4.
U2	M0_DQ[5]	I/O, POD12	M0_DDR4_DQ5.
P6	M0_DQ[6]	I/O, POD12	M0_DDR4_DQ6.
R2	M0_DQ[7]	I/O, POD12	M0_DDR4_DQ7.
U6	M0_DQ[8]	I/O, POD12	M0_DDR4_DQ8.

Pin #	Pin Name	Pin Type	Description
AA1	M0_DQ[9]	I/O, POD12	M0_DDR4_DQ9.
W7	M0_DQ[10]	I/O, POD12	M0_DDR4_DQ10.
Y2	M0_DQ[11]	I/O, POD12	M0 DDR4 DQ11.
W3	M0_DQ[12]	I/O, POD12	M0_DDR4_DQ12.
AA2	M0_DQ[13]	I/O, POD12	M0_DDR4_DQ13.
W4	M0_DQ[14]	I/O, POD12	M0_DDR4_DQ14.
AB2	M0_DQ[15]	I/O, POD12	M0_DDR4_DQ15.
AE4	M0_DQ[16]	I/O, POD12	M0_DDR4_DQ16.
AF1	M0_DQ[17]	I/O, POD12	M0_DDR4_DQ17.
AC6	M0_DQ[18]	I/O, POD12	M0_DDR4_DQ18.
AD3	M0_DQ[19]	I/O, POD12	M0_DDR4_DQ19.
AC4	M0_DQ[20]	I/O, POD12	M0_DDR4_DQ20.
AE3	M0_DQ[21]	I/O, POD12	M0_DDR4_DQ21.
AC7	M0_DQ[22]	I/O, POD12	M0_DDR4_DQ22.
AD2	M0_DQ[23]	I/O, POD12	M0_DDR4_DQ23.
AH2	M0_DQ[24]	I/O, POD12	M0_DDR4_DQ24.
AL3	M0_DQ[25]	I/O, POD12	M0_DDR4_DQ25.
AE6	M0_DQ[26]	I/O, POD12	M0_DDR4_DQ26.
AJ2	M0_DQ[27]	I/O, POD12	M0_DDR4_DQ27.
AG4	M0_DQ[28]	I/O, POD12	M0_DDR4_DQ28.
AL4	M0_DQ[29]	I/O, POD12	M0_DDR4_DQ29.
AJ3	M0_DQ[30]	I/O, POD12	M0_DDR4_DQ30.
AM4	M0_DQ[31]	I/O, POD12	M0_DDR4_DQ31.
N2	M0_DQSn[0]	I/O, POD12	M0_DDR4_DQS0 negative.
P2	M0_DQSp[0]	I/O, POD12	M0_DDR4_DQS0 positive.
W2	M0_DQSn[1]	I/O, POD12	M0_DDR4_DQS1 negative.
W1	M0_DQSp[1]	I/O, POD12	M0_DDR4_DQS1 positive.
AC1	M0_DQSn[2]	I/O, POD12	M0_DDR4_DQS2 negative.
AC2	M0_DQSp[2]	I/O, POD12	M0_DDR4_DQS2 positive.
AJ1	M0_DQSn[3]	I/O, POD12	M0_DDR4_DQS3 negative.
AH1	M0_DQSp[3]	I/O, POD12	M0_DDR4_DQS3 positive.
B5	M0_NC	O, SSTL12	This pin is used for DDR3/DDR3L only.
L2	M0_ODT	O, SSTL12	M0_DDR4 On die termination.
L1	M0_RASn	O, SSTL12	M0_DDR4 Row activate.
A5	M0_RSTn	O, SSTL12	M0_DDR4_RSTn. This pin is active low.
F1	M0_WEn	O, SSTL12	M0_DDR4 Write enable or M0_A[14].

Table 8. DDR3 Mode 1 Interface Configuration

Pin #	Pin Name	Pin Type	Description
C4	M0_A[0]	O, SSTL15	M0_DDR3_A11
H6	M0_A[1]	O, SSTL15	M0_DDR3_A2
K6	M0_A[2]	O, SSTL15	M0_DDR3_A6
J3	M0_A[3]	O, SSTL15	M0_DDR3_A15
H2	M0_A[4]	O, SSTL15	M0_DDR3_A0
G2	M0_A[5]	O, SSTL15	M0_DDR3_A12
F3	M0_A[6]	O, SSTL15	M0_DDR3_A5
F2	M0_A[7]	O, SSTL15	M0_DDR3_A4
F4	M0_A[8]	O, SSTL15	M0_DDR3_A9
C1	M0_A[9]	O, SSTL15	M0_DDR3_A7
K7	M0_A[10]	O, SSTL15	M0_DDR3_A3
B4	M0_A[11]	O, SSTL15	M0_DDR3_A8
K3	M0_A[12]	O, SSTL15	M0_DDR3_A10
H3	M0_A[13]	O, SSTL15	M0_DDR3_A1
D3	M0_ACTn	O, SSTL15	M0_DDR3_A13
C3	M0_BA[0]	O, SSTL15	M0_DDR3_BA0 Bank select[0]
D2	M0_BA[1]	O, SSTL15	M0_DDR3_BA1 Bank select[1]
C2	M0_BG	O, SSTL15	M0_DDR3_BA2 Bank select[2]
M7	M0_CAL	I, Analog	DDR4/DDR3/DDR3L Calibration pad. Connect to VSS via a 240 ±1% Ohm resitor.
H1	M0_CASn	O, SSTL15	M0_DDR3_CASn Column active
J2	M0_CKE	O, SSTL15	M0_DDR3_CKE Clock enable
M4	M0_CKn	O, SSTL15	M0_DDR3_CKn Negative for 2x16 chips
M3	M0_CKp	O, SSTL15	M0_DDR3_CKp Positve for 2x16 chips
M2	M0_CSn	O, SSTL15	M0_DDR3_CSn Chip select
V2	M0_DM[0]	O, SSTL15	M0_DDR3_DM0 Data mask BYTE[0]
W6	M0_DM[1]	O, SSTL15	M0_DDR3_DM1 Data mask BYTE[1]
AF2	M0_DM[2]	O, SSTL15	M0_DDR3_DM2 Data mask BYTE[2]
AK2	M0_DM[3]	O, SSTL15	M0_DDR3_DM3 Data mask BYTE[3]
T6	M0_DQ[0]	I/O, SSTL15	M0_DDR3_DQ2
T1	M0_DQ[1]	I/O, SSTL15	M0_DDR3_DQ3
U3	M0_DQ[2]	I/O, SSTL15	M0_DDR3_DQ0
T2	M0_DQ[3]	I/O, SSTL15	M0_DDR3_DQ5
P4	M0_DQ[4]	I/O, SSTL15	M0_DDR3_DQ6
U2	M0_DQ[5]	I/O, SSTL15	M0_DDR3_DQ1
P6	M0_DQ[6]	I/O, SSTL15	M0_DDR3_DQ4
R2	M0_DQ[7]	I/O, SSTL15	M0_DDR3_DQ7
U6	M0_DQ[8]	I/O, SSTL15	M0_DDR3_DQ13

Pin #	Pin Name	Pin Type	Description
AA1	M0_DQ[9]	I/O, SSTL15	M0_DDR3_DQ8
W7	M0_DQ[10]	I/O, SSTL15	M0_DDR3_DQ11
Y2	M0_DQ[11]	I/O, SSTL15	M0_DDR3_DQ12
W3	M0_DQ[12]	I/O, SSTL15	M0_DDR3_DQ15
AA2	M0_DQ[13]	I/O, SSTL15	M0_DDR3_DQ14
W4	M0_DQ[14]	I/O, SSTL15	M0_DDR3_DQ9
AB2	M0_DQ[15]	I/O, SSTL15	M0_DDR3_DQ10
AE4	M0_DQ[16]	I/O, SSTL15	M0_DDR3_DQ18
AF1	M0_DQ[17]	I/O, SSTL15	M0_DDR3_DQ19
AC6	M0_DQ[18]	I/O, SSTL15	M0_DDR3_DQ16
AD3	M0_DQ[19]	I/O, SSTL15	M0_DDR3_DQ21
AC4	M0_DQ[20]	I/O, SSTL15	M0_DDR3_DQ22
AE3	M0_DQ[21]	I/O, SSTL15	M0_DDR3_DQ17
AC7	M0_DQ[22]	I/O, SSTL15	M0_DDR3_DQ20
AD2	M0_DQ[23]	I/O, SSTL15	M0_DDR3_DQ23
AH2	M0_DQ[24]	I/O, SSTL15	M0_DDR3_DQ27
AL3	M0_DQ[25]	I/O, SSTL15	M0_DDR3_DQ24
AE6	M0_DQ[26]	I/O, SSTL15	M0_DDR3_DQ31
AJ2	M0_DQ[27]	I/O, SSTL15	M0_DDR3_DQ28
AG4	M0_DQ[28]	I/O, SSTL15	M0_DDR3_DQ29
AL4	M0_DQ[29]	I/O, SSTL15	M0_DDR3_DQ30
AJ3	M0_DQ[30]	I/O, SSTL15	M0_DDR3_DQ25
AM4	M0_DQ[31]	I/O, SSTL15	M0_DDR3_DQ26
N2	M0_DQSn[0]	I/O, SSTL15	M0_DDR3_DQS0n negative BYTE0
P2	M0_DQSp[0]	I/O, SSTL15	M0_DDR3_DQS0p positive BYTE0
W2	M0_DQSn[1]	I/O, SSTL15	M0_DDR3_DQS1n negative BYTE1
W1	M0_DQSp[1]	I/O, SSTL15	M0_DDR3_DQS1p positve BYTE1
AC1	M0_DQSn[2]	I/O, SSTL15	M0_DDR3_DQS2n negative BYTE2
AC2	M0_DQSp[2]	I/O, SSTL15	M0_DDR3_DQS2p positive BYTE2
AJ1	M0_DQSn[3]	I/O, SSTL15	M0_DDR3_DQS3n negative BYTE3
AH1	M0_DQSp[3]	I/O, SSTL15	M0_DDR3_DQS3p positive BYTE3
B5	M0_NC	O, SSTL15	M0_DDR3_A14
L2	M0_ODT	O, SSTL15	M0_DDR3_ODT One die termination
L1	M0_RASn	O, SSTL15	M0_DDR3_RASn Row active
A5	M0_RSTn	O, SSTL15	M0_DDR3_RSTn RESETn for DDR3/DDR3L
F1	M0_WEn	O, SSTL15	M0_DDR3_WEn Write enable

Table 9. UART Interface

Pin #	Pin Name	Pin Type	Description
C22	URT1_RXD	I, CMOS	UART1 RX location A
C23	URT1_TXD	O, CMOS	UART1 TX location A

Table 10. Two-Wire Serial Interface

Pin #	Pin Name	Pin Type	Description
B8	TW0_SDA	IOod, CMOS	TWSI0 Serial data.
A8	TW0_SCL	IOod, CMOS	TWSI0 Serial clock.
F8	TW1_SDA	IOod, CMOS	TWSI1 Serial data.
C8	TW1_SCL	IOod, CMOS	TWSI1 Serial clock.
A18	TW2_SDA	IOod, CMOS	TWSI2 Serial data.
C17	TW2_SCL	IOod, CMOS	TWSI2 Serial clock.
C21	TW3_SDA	IOod, CMOS	TWSI3 Serial data.
B21	TW3_SCL	IOod, CMOS	TWSI3 Serial clock.

Table 11. Audio Interface (I^2S/TDM)

Pin #	Pin Name	Pin Type	Description
M31	I2S1_BCLK	I/O, CMOS	Interface #1 Audio bit clock.
L31	I2S1_LRCK	I/O, CMOS	Interface #1 Audio WS or LR select.
M32	I2S1_MCLK	I/O, CMOS	Interface #1 Audio Host clock.
M26	I2S1_DO	O, CMOS	Interface #1 Data out.
M27	I2S1_DI	O, CMOS	Interface #1 Data In.
P27	I2S2_BCLK	I/O, CMOS	Interface #2 Audio bit clock.
N31	I2S2_LRCK	I/O, CMOS	Interface #2 Audio WS or LR select.
P30	I2S2_DO	I, CMOS	Interface #2 Data out.
R30	I2S2_DI	I, CMOS	Interface #2 Data in.
T31	I2S3_BCLK	I/O, CMOS	Interface #3 Audio bit clock.
R31	I2S3_LRCK	I/O, CMOS	Interface #3 Audio WS or LR select.
R32	I2S3_DO	O, CMOS	Interface #3 Data out.
U32	I2S3_DI	I, CMOS	Interface #3 Data in.

Table 12. Audio Interface (PDM)

Pin #	Pin Name	Pin Type	Description
T26	PDM_CLKIO	O, CMOS	PDM Clock out.
T27	PDM_DI[0]	I, CMOS	PDM Data in channel 0.
R29	PDM_DI[1]	I, CMOS	PDM Data in channel 1.

Table 13. USB 2.0 Interface

Pin #	Pin Name	Pin Type	Description
AM19	USB2_Dp	I/O, Analog	USB 2.0 Port Data Positive.
AM18	USB2_Dn	I/O, Analog	USB 2.0 Port Data Negative.
AL19	USB2_ID	I, Analog	USB 2.0 OTG ID.
AL20	USB2_REXT	I, Analog	USB external reference resistor. Connect a 200 ohm ±1% resistor to VSS.
AL18	USB2_VBUS	I, Analog	Connect an external 30 kohm ±1% series resistor to USB 2.0 VBUS.
F25	USB2_DRV_VBUS	O, CMOS	USB OTG requires this signal. It enables 5V to be driven onto VBUS. 0: Do not drive VBUS. 1: Drive 5V on VBUS. DRV_VBUS must be connected to an external PMIC or power switch to provide power for USB VBUS. There is no on-chip power switch for VBUS.

Table 14. USB 3.0 Interface

Pin #	Pin Name	Pin Type	Description
AL14	USB3_TXp	I, Analog	USB 3.0 SS Transmit Port Data Positive.
AM14	USB3_TXn	I, Analog	USB 3.0 SS Transmit Port Data Negative.
AL17	USB3_RXp	I, Analog	USB 3.0 SS Receive Port Data Positive.
AM17	USB3_RXn	I, Analog	USB 3.0 SS Receive Port Data Negative.
AL16	USB3_Dp	I/O, Analog	USB 3.0 Port Data Positive.
AL15	USB3_Dn	I/O, Analog	USB 3.0 Port Data Negative.
AG16	USB3_ID	I, Analog	USB 3.0 ID pin . This pin should be connected to VSS or left floating.
AG12	USB3_REXT	I, Analog	USB 3.0 Calibration pad. This pin should be connected to VSS via a 200 ohm resistor.
AJ16	USB3_VBUS	I, Analog	This pin is not 5V tolerant and must not connect directly to the 5V VBUS voltage on USB link. This pin must be isolated by an external 30 kOhm resistor so it could see a lower voltage.

Table 15. NAND Interface

Pin #	Pin Name	Pin Type	Description
B30	NAND_CEn	O, CMOS	NAND active low Chip Enable.
B28	NAND_ALE	O, CMOS	NAND active high Address Latch Enable.
AL24	NAND_WEn	O, CMOS	NAND active low Write Enable.
AM23	NAND_RDY	Iu, CMOS	NAND active high ready (active low busy) input from NAND.
AK22	NAND_DATA[0]	I/O, CMOS	NAND Data 0.
AK21	NAND_DATA[1]	I/O, CMOS	NAND Data 1.
AL22	NAND_DATA[2]	I/O, CMOS	NAND Data 2.
AL23	NAND_DATA[3]	I/O, CMOS	NAND Data 3.
AL25	NAND_DATA[4]	I/O, CMOS	NAND Data 4.
AM25	NAND_DATA[5]	I/O, CMOS	NAND Data 5.
AK25	NAND_DATA[6]	I/O, CMOS	NAND Data 6.
AK27	NAND_DATA[7]	I/O, CMOS	NAND Data 7.
AG25	NAND_REn	O, CMOS	NAND Read Enable.
AJ25	NAND_CLE	O, CMOS	NAND active high Command Latch Enable.

Table 16. eMMC 5.1 Interface

Pin #	Pin Name	Pin Type	Description
AL24	EMMC_CLK	O, CMOS	Output clock.
AM23	EMMC_CMD	I/O, CMOS	Command/Response.
AJ25	EMMC_STRB	I, CMOS	Read Strobe
AG25	EMMC_RSTn	O, CMOS	Hardware reset.
AK22	EMMC_DATA[0]	I/O, CMOS	Data[0].
AK21	EMMC_DATA[1]	I/O, CMOS	Data[1].
AL22	EMMC_DATA[2]	I/O, CMOS	Data[2].
AL23	EMMC_DATA[3]	I/O, CMOS	Data[3].
AL25	EMMC_DATA[4]	I/O, CMOS	Data[4].
AM25	EMMC_DATA[5]	I/O, CMOS	Data[5].
AK25	EMMC_DATA[6]	I/O, CMOS	Data[6].
AK27	EMMC_DATA[7]	I/O, CMOS	Data[7].

Table 17. RGMII Interface, 1.8V Interface

Pin #	Pin Name	Pin Type	Description
D27	RGMII_TXD[0]	O, CMOS	TX Data 0.
D31	RGMII_TXD[1]	O, CMOS	TX Data 1.
D30	RGMII_TXD[2]	O, CMOS	TX Data 2.
E31	RGMII_TXD[3]	O, CMOS	TX Data 3.
F31	RGMII_RXD[0]	I, CMOS	RX Data 0.
G31	RGMII_RXD[1]	I, CMOS	RX Data 1.
G32	RGMII_RXD[2]	I, CMOS	RX Data 2.
H31	RGMII_RXD[3]	I, CMOS	RX Data 3.
C30	RGMII_TXC	O, CMOS	TX Clock Output.
F30	RGMII_TXCTL	O, CMOS	TX Control.
F28	RGMII_RXC	I, CMOS	RX Clock Input.
H30	RGMII_RXCTL	I, CMOS	RX Control.
A30	RGMII_CLK_OUT	O, CMOS	RGMII PHY Clock Reference Output.

Table 18. LCDC (RGB) Interface, 3.3V Interface

Pin #	Pin Name	Pin Type	Description
U31	LCD_D[0]	IO, CMOS	LCD Data 0.
V31	LCD_D[1]	IO, CMOS	LCD Data 1.
V30	LCD_D[2]	IO, CMOS	LCD Data 2.
W29	LCD_D[3]	IO, CMOS	LCD Data 3.
W30	LCD_D[4]	IO, CMOS	LCD Data 4.
Y32	LCD_D[5]	IO, CMOS	LCD Data 5.
Y31	LCD_D[6]	IO, CMOS	LCD Data 6.
AA31	LCD_D[7]	IO, CMOS	LCD Data 7.
AA30	LCD_D[8]	IO, CMOS	LCD Data 8.
AA29	LCD_D[9]	IO, CMOS	LCD Data 9.
AB32	LCD_D[10]	IO, CMOS	LCD Data 10.
AB31	LCD_D[11]	IO, CMOS	LCD Data 11.
AC30	LCD_D[12]	IO, CMOS	LCD Data 12.
AC27	LCD_D[13]	IO, CMOS	LCD Data 13.
AC26	LCD_D[14]	IO, CMOS	LCD Data 14.
AD30	LCD_D[15]	IO, CMOS	LCD Data 15.
AD31	LCD_D[16]	IO, CMOS	LCD Data 16.
AE32	LCD_D[17]	IO, CMOS	LCD Data 17.
AE31	LCD_D[18]	IO, CMOS	LCD Data 18.
AE27	LCD_D[19]	IO, CMOS	LCD Data 19.
AE26	LCD_D[20]	IO, CMOS	LCD Data 20.
AF31	LCD_D[21]	IO, CMOS	LCD Data 21.
AG31	LCD_D[22]	IO, CMOS	LCD Data 22.
AG29	LCD_D[23]	IO, CMOS	LCD Data 23.
AG32	LCD_CLK	O, CMOS	Clock Output.
AG30	LCD_GPIO[0]	IO, CMOS	LCD GPIO 0.
AJ30	LCD_GPIO[1]	IO, CMOS	LCD GPIO 1.
AJ31	LCD_GPIO[2]	IO, CMOS	LCD GPIO 2.
AK31	LCD_GPIO[3]	IO, CMOS	LCD GPIO 3.
AK32	LCD_GPIO[4]	IO, CMOS	LCD GPIO 4.

Table 19. MIPI TX Interface

Pin #	Pin Name	Pin Type	Description
AM5	MIPI_DSI_REXT	O, CMOS	MIPI TX Analog Test Bus Out.
AM9	MIPI_DSI_CKp	O, CMOS	MIPI TX Clock lane +ve line.
AL9	MIPI_DSI_CKn	O, CMOS	MIPI TX Clock lane -ve line.
AM6	MIPI_DSI_D0p	O, CMOS	MIPI TX Data lane 0 +ve line.
AL6	MIPI_DSI_D0n	O, CMOS	MIPI TX Data lane 0 -ve line.
AL8	MIPI_DSI_D1p	O, CMOS	MIPI TX Data lane 1 +ve line.
AM8	MIPI_DSI_D1n	O, CMOS	MIPI TX Data lane 1 -ve line.
AL11	MIPI_DSI_D2p	O, CMOS	MIPI TX Data lane 2 +ve line.
AM11	MIPI_DSI_D2n	O, CMOS	MIPI TX Data lane 2 -ve line.
AM12	MIPI_DSI_D3p	O, CMOS	MIPI TX Data lane 3 +ve line.
AL12	MIPI_DSI_D3n	O, CMOS	MIPI TX Data lane 3 -ve line.

Table 20. General Dedicated Purpose I/O Interface

Pin #	Pin Name	Pin Type	Description
F23	GPIO_A[0]	I/O, CMOS	General purpose I/O.
D25	GPIO_A[1]	I/O, CMOS	General purpose I/O.
B25	GPIO_A[2]	I/O, CMOS	General purpose I/O.
B26	GPIO_A[3]	I/O, CMOS	General purpose I/O.

Table 21. Power - 1.8V

Pin #	Pin Name	Pin Type	Description
AA27	AVPLL_AVDD1P8	PWR	Analog VDD 1.8V AVPLL supply.
C6	CPUPLL_AVDD1P8	PWR	Analog VDD 1.8V CPU PLL supply.
D6	CPUTSEN_AVDD1P8	PWR	Analog VDD 1.8V for temperature sensor.
M29	KILOOTP_AVDD1P8	PWR	Analog VDD 1.8V Kilopass OTP supply.
AG23	NAND_VDDIO1P8	PWR	NAND/EMMC 1.8V Supply.
AJ27	SDIO_VDDIO1P8	PWR	SDIO 1.8V Supply.
AJ8	MIPI_DSI_AVDD1P8	PWR	Analog VDD 1.8V for MIPI DSI PHY.
AD9	M0_AVDD1P8	PWR	Analog VDD 1.8V for DDR PHY.
K29	OSC_VDDIO1P8	PWR	Power for on-chip crystal oscillator.
K27	SYSPLL_AVDD1P8	PWR	Analog VDD 1.8V SYSPLL supply.
H21 H25 K16 K18 K22 M16 M18 P22 U27 W27	VDDIO1P8	PWR	1.8V VDD I/O.

Table 22. Power - 3.3V

Pin #	Pin Name	Pin Type	Description
AE30	LCD_VDDIO3P3	PWR	VDDIO 3.3V power (for LCDC).
AJ12	USB3_AVDD3P3	PWR	3.3V I/O supply for USB3.
AG21	USB2_AVDD3P3	PWR	3.3V I/O supply for USB2.
AJ19	USB2_VR_AVDD3P3	PWR	Analog VDD (3.3V) for USB2.

Table 23. Power and Ground Pins

Pin #	Pin Name	Pin Type	Description
AG17	USB2_DVDD	PWR	USB 2.0 DVDD 0.8V.
AG14	USB3_DVDD	PWR	USB 3.0 DVDD 0.8V.
AJ14	USB3_AVDD	PWR	USB 3.0 AVDD 0.8V.
AJ6	MIPI_DSI_AVDD	PWR	MIPI Analog VDD 0.8V
L10 N10 N12 P12 T12 V12 Y12	VDDQ	PWR	I/O power: DDR4 1.2V, DDR3 1.5V, DDR3L 1.35V.
AB14 AB22 AD14 AD16 AD18 AD20 AD22 L13 L20 N14 N18 N22 P14 P18 T16 T20 V16 V20 Y14 Y18 Y20 Y22	VDD_CORE	PWR	Core Voltage
A7	VDD_CORE_FB	PWR	Core Voltage feedback compensation.

Pin #	Pin Name	Pin Type	Description
A1 A13 A2 A28 A31 A32 A6 AA26 AA3 AA4 AA6 AA7 AB10 AB12 AB16 AB18 AB20 AB24 AB9 AC29 AC3 AD10 AD12 AD24 AE29 AE7 AF10 AF12 AF14 AF16 AF17 AF19 AF21 AF23 AF25 AF8 AG10 AG19 AG2 AG27 AG3 AG6 AG8 AJ10 AJ17 AJ21	VSS	GND	Core ground.

Pin #	Pin Name	Pin Type	Description
AJ23			
AJ29			
AJ4			
AK12			
AK14			
AK17			
AK23			
AK28			
AK6			
AK8			
AL1			
AL10			
AL2			
AL31			
AL32			
AL5			
AM1			
AM2			
AM31			
AM32			
B1			
B2			
B31	VSS (continued…)	GND	Core ground.
B32			
B6			
C10			
C14			
C19			
C25			
C5			
D10			
D16			
D21			
D23			
D29			
D4			
D8			
E32			
F12			
F16			
F17			
F27			
F6			
G21			
G25			

Pin #	Pin Name	Pin Type	Description
H16 H17 H10 H12 H14 H19 H23 H27 H29 H4 H7 H8 J31 K12 K14 K20 K24 K26 K28 K31 K4 L12 L14 L16 L18 L21 L22 L24 L9 M28 M30 M6 N1 N16 N20 N24 N8 N9 P10 P16 P20 P24 P26 P3 P7 T10	VSS (continued…)	GND	Core ground.

Pin #	Pin Name	Pin Type	Description
T14 T18 T22 T24 T4 T7 T9 U26 U29 U30 U4 U7 V1 V10 V14 V18 V22 V24 V9 W26 Y10 Y16 Y24 Y9	VSS (continued…)	GND	Core ground.

4. Pin Multiplexing

Note: This document is preliminary and subject to change.

4.1. Pin Multiplexing Signal Descriptions

For complete pin multiplexing details, refer to 4.2 Pin Multiplexing Modes.

Table 24. SoC Reset Strapping

Pin #	Pin Mux Name	Primary Pin Name	Pin Type	Description
B19	SOFTWARE_STRAP[0]	SPI2_SDO	PU-boot	Strap for software usage. ROM code will use this strap to decide to boot from USB or not. 0: Boot from USB. 1: Boot from the device selected by BOOT_SRC[1:0].
F19	SOFTWARE_STRAP[1]	SPI2_SS0n	PD-boot	Strap for software usage.
B16	SOFTWARE_STRAP[2]	SPI1_SDO	PD-boot	Strap for software usage.
C16	SOFTWARE_STRAP[3]	SPI1_SCLK	PD-boot	Strap for software usage.
F25	PLLBYPS	USB2_DRV_VBUS	PD-boot	SYS/MEM/CPU PLL bypass. 0: No bypass. 1: All PLL bypassed.
A20	PLLPWRDOWN	SPI2_SCLK	PD-boot	SYS/MEM/CPU PLL power down. 0: Power up. 1: Power down (reserved for factory use).
A23	CPURSTBYPS	PWM[0]	PD-boot	CPU reset bypass strap. 0: Enable reset logic inside CPU partition. 1: Bypass reset logic inside CPU partition.
M26	BOOT_SRC[0]	I2S1_DO	PU-boot	CPU boot source bit 0. BOOT_SRC[1:0]: 00: ROM boot from SPI. 01: ROM boot from NAND . 10: ROM boot from eMMC. 11: Direct boot from SPI (reserved for factory use).
P30	BOOT_SRC[1]	I2S2_DO	PD-boot	CPU boot source bit 1.
R32	LEGACY_BOOT	I2S3_DO	PD-boot	Strap to reduce reset wait time. 0: 2ms. 1: 20ms.

1. PU-boot or PD-boot indicates built-in weak pull-up or pull-down that can be disabled by software after boot up.

4.2. Pin Multiplexing Modes

This section describes the various modes related to the multiplexed pins. The primary pin name reflects the pinout name, while the Mode 0, Mode 1, ..., Mode 4 and Strap multiplex names are located in the respective columns.

Figure 8 shows the multiplexed pin naming scheme that is used for the Multiplexed pins.

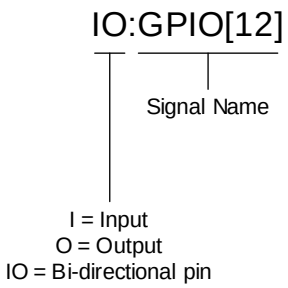


Figure 8. Example of the Multiplexed Pin Naming Scheme

Table 25. I^2S1, I^2S2, I^2S3 and PDM Interface Group Multiplexing

Pin #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Strap Mode
M26	I2S1_DO	IO:GPIO[16] (Output Only)	O:I2S1_DO	—	O:DAIF_IF_CDC_DAT_DA	boot_src[0]
M27	I2S1_DI	IO:GPIO[18]	I:I2S1_DI	—	O:DAIF_IF_DAT_DA	—
L31	I2S1_LRCK	IO:GPIO[14]	IO:I2S1_LRCK	—	I:DAIF_IF_CLK_PLL	—
M31	I2S1_BCLK	IO:GPIO[15]	IO:I2S1_BCLK	—	I:DAIF_IF_CDC_DAT_AD	—
M32	I2S1_MCLK	IO:GPIO[17]	IO:I2S1_MCLK	—	O:DAIF_IF_CLK_IF	—
N31	I2S2_LRCK	IO:GPIO[19]	IO:I2S2_LRCK	I:URT0B_CTSn	I:DAIF_IF_DAT_AD	—
P27	I2S2_BCLK	IO:GPIO[20]	IO:I2S2_BCLK	O:URT0B_RTSn	I:DAIF_IF_EN_AD	—
P30	I2S2_DO	IO:GPIO[21] (Output Only)	O:I2S2_DO	—	O:DAIF_IF_EN_DA	boot_src[1]
R30	I2S2_DI	IO:GPIO[22]	I:I2S2_DI	—	I:DAIF_IF_INT_ANA	—
T26	PDM_CLKIO	IO:GPIO[25]	IO:PDM_CLKIO	IO:I2S2A_MCLK	—	—
T27	PDM_DI[0]	IO:GPIO[24]	I:PDM_DI[0]	—	—	—
R29	PDM_DI[1]	IO:GPIO[23]	I:PDM_DI[1]	—	—	—
R32	I2S3_DO	IO:GPIO[28] (Output Only)	O:I2S3_DO	—	—	legacy_boot
R31	I2S3_LRCK	IO:GPIO[26]	IO:I2S3_LRCK	—	—	—
T31	I2S3_BCLK	IO:GPIO[27]	IO:I2S3_BCLK	—	—	—
U32	I2S3_DI	IO:GPIO[29]	I:I2S3_DI	—	—	—

1. Mode 0 is the default mode after reset.

Table 26. TWSI/SPI Interface Group Multiplexing

Pin #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4	Strap Mode
A8	TW0_SCL	IO:TW0A_SCL	IO:GPIO[10]	I:URT0A_CTSn	IO:I2S4_LRCK	—	—
B8	TW0_SDA	IO:TW0A_SDA	IO:GPIO[11]	O:URT0A_RTSn	IO:I2S4_BCLK	—	—
C8	TW1_SCL	IO:TW1_SCL	IO:GPIO[12]	—	O:I2S4_DO	—	—
F8	TW1_SDA	IO:TW1_SDA	IO:GPIO[13]	O:CLK_25M	I:I2S4_DI	—	—
A15	SPI1_SS0n	O:SPI1_SS0n	IO:GPIO[3]	—	—	—	—
D14	SPI1_SS1n	O:CORE_POR_N	O:SPI1_SS1n	IO:GPIO[4]	I:DSI_TE	I:GPIO_TRIG[1]	—
F14	SPI1_SS2n	I:URT0A_RXD	O:SPI1_SS2n	IO:GPIO[5]	—	I:GPIO_TRIG[2]	—
B15	SPI1_SS3n	O:URT0A_TXD	O:SPI1_SS3n	IO:GPIO[6]	—	—	
B16	SPI1_SDO	O:SPI1_SDO	IO:GPIO[7] (Output Only)	—	—	—	software_strap[2]
D17	SPI1_SDI	I:SPI1_SDI	IO:GPIO[9]	—	—	—	—
C16	SPI1_SCLK	O:SPI1_SCLK	IO:GPIO[8] (Output Only)	—	—	—	software_strap[3]
C17	TW2_SCL	IO:GPIO[37]	IO:TW2_SCL	I:KEY_ROW0	O:RGMIIB_MDC	—	—
A18	TW2_SDA	IO:GPIO[38]	IO:TW2_SDA	I:KEY_ROW1	IO:RGMIIB_MDIO	—	—
F19	SPI2_SS0n	IO:GPIO[30] (output only)	O:SPI2_SS0n	—	—	—	software_strap[1]
B18	SPI2_SS1n	IO:GPIO[31]	O:SPI2_SS1n	—	O:DAIF_IF_CDC_DIR	—	—
D19	SPI2_SS2n	O:IO_POR_N	IO:GPIO[32]	O:SPI2_SS2n	I:DAIF_IF_PWR_OK	I:PDM_DI[2]	—
F21	SPI2_SS3n	I:PWR_OK	IO:GPIO[33]	O:SPI2_SS3n	O:DAIF_IF_NARES	I:PDM_DI[3]	—
B19	SPI2_SDO	IO:GPIO[34] (output only)	O:SPI2_SDO	—	—	—	software_strap[0]
A20	SPI2_SCLK	IO:GPIO[35] (Output Only)	O:SPI2_SCLK	—	—	—	pllPwrDown
B20	SPI2_SDI	IO:GPIO[36]	I:SPI2_SDI	—	—	—	—
B21	TW3_SCL	IO:GPIO[41]	IO:TW3A_SCL	O:URT1A_RTSn	O:IF_DCLS	—	—
C21	TW3_SDA	IO:GPIO[42]	IO:TW3A_SDA	I:URT1A_CTSn	O:IF_DCLS_N	—	—

1. Mode 0 is the default mode after reset. Strap mode is only used during power up reset.
2. Recommended as output only. When used as input, the external driving source shall not interfere with the pin's strap mode or mode 0 function.

Table 27. Global and PWM Interface Group Multiplexing

Pin #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4	Strap Mode
A23	PWM[0]	IO:GPIO[46](Output Only)	O:PWM[0]	O:RGMII_ PTP_PPS_O	—	—	cpuRstByps
B23	PWM[1]	IO:GPIO[45]	O:PWM[1]	—	—	—	—
B24	PWM[2]	IO:GPIO[44]	O:PWM[2]	IO:KEY_COL1	—	—	—
A25	PWM[3]	IO:GPIO[43]	O:PWM[3]	—	IO:IF_DCLS_SCLK	—	—
F23	GPIO_A[0]	IO:GPIO[50]	IO:RGMIIA_MDIO	O:PWM[1]	—	—	—
D25	GPIO_A[1]	IO:GPIO[49]	O:RGMIIA_MDC	O:PWM[2]	—	—	—
B25	GPIO_A[2]	IO:GPIO[48]	—	I:KEY_ROW5	O:URT1B_TXD	—	—
B26	GPIO_A[3]	IO:GPIO[47]	—	I:KEY_ROW4	I:URT1B_RXD	—	—
B13	TDI	I:TDI	IO:GPIO[1]	I:URT0B_RXD	IO:KEY_COL3	I:GPIO_TRIG[0]	—
B14	TDO	O:TDO	IO:GPIO[2]	IO:PDMB_CLKIO	IO:I2S2B_MCLK	—	—
C12	TMS	I:TMS	IO:GPIO[0]	O:URT0B_TXD	IO:KEY_COL2	—	—
F25	USB2_DRV_VBUS	O:USB2_DRV_VBUS	IO:GPIO[51] (Output Only)	—	—	—	pllByps

1. Mode 0 is the default mode after reset.
2. Recommended as output only. When used as input, the external driving source shall not interfere with the pin's strap mode or mode 0 function.

Table 28. UART1 Interface Group Multiplexing

Pin #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4
C22	URT1_RXD	IO:GPIO[39]	—	I:URT1A_RXD	I:KEY_ROW2	I:GPIO_TRIG[3]
C23	URT1_TXD	IO:GPIO[40]	—	O:URT1A_TXD	I:KEY_ROW3	—

1. Mode 0 is the default mode after reset.

Table 29. SDIO Interface Group Multiplexing

Pin #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3
C26	SDIO_CDn	IO:GPIO[54]	I:SDIOA_CDn	IO:KEY_COL0	O:URT1B_RTSn
C27	SDIO_WP	IO:GPIO[55]	I:SDIOA_WP	—	I:URT1B_CTSn

1. Mode 0 is the default mode after reset. Strap mode is only used during power up reset.

Table 30. RGMII/RMII Interface Group Multiplexing

Pin #	Primary Pin Name	RMII Pinmux	Mode 0[1, 2]	Mode 1
A30	RGMII_CLK_OUT	N/A	IO:GPIO_X[53]	O:REFCLK_25MHz
C30	RGMII_TXC	RMII_TXC/Refclk	IO:GPIO_X[43]	O:RGMII_TXC
D27	RGMII_TXD[0]	RMII_TXD0	IO:GPIO_X[19]	O:RGMII_TXD[0]
D31	RGMII_TXD[1]	RMII_TXD1	IO:GPIO_X[20]	O:RGMII_TXD[1]
D30	RGMII_TXD[2]	N/A	IO:GPIO_X[21]	O:RGMII_TXD[2]
E31	RGMII_TXD[3]	N/A	IO:GPIO_X[22]	O:RGMII_TXD[3]
F30	RGMII_TXCTL	RMII_TXEN	IO:GPIO_X[51]	O:RGMII_TXCTL
F28	RGMII_RXC	RMII_RXC	IO:GPIO_X[42]	I:RGMII_RXC
F31	RGMII_RXD[0]	RMII_RXD0	IO:GPIO_X[31]	I:RGMII_RXD[0]
G31	RGMII_RXD[1]	RMII_RXD1	IO:GPIO_X[32]	I:RGMII_RXD[1]
G32	RGMII_RXD[2]	N/A	IO:GPIO_X[33]	I:RGMII_RXD[2]
H31	RGMII_RXD[3]	N/A	IO:GPIO_X[41]	I:RGMII_RXD[3]
H30	RGMII_RXCTL	RMII_CRSDV	IO:GPIO_X[52]	I:RGMII_RXCTL

1. Mode 0 is the default mode after reset. Strap mode is only used during power up reset.
2. GPIO_X[n] designates second location for GPIO[n].

Table 31. NAND Interface Group Multiplexing

Pin #	Primary Pin Name	Mode 0[1]	Mode 1
B28	NAND_ALE	IO:GPIO[52]	O:NAND_ALE
B30	NAND_CEn	IO:GPIO[53]	O:NAND_CEn

1. Mode 0 is the default mode after reset. Strap mode is only used during power up reset.

Table 32. LCDC RGB Interface Group Multiplexing

Pin #	Primary Pin Name	Mode 0[1, 2]	Mode 1	Mode 2	Mode 3
U31	LCD_D[0]	IO:GPIO_X[12]	IO:LCD_D[0]	I:KEY_ROW6	IO:TW3B_SCL
V31	LCD_D[1]	IO:GPIO_X[13]	IO:LCD_D[1]	I:KEY_ROW7	IO:TW3B_SDA
V30	LCD_D[2]	IO:GPIO[56]	IO:LCD_D[2]	—	—
W29	LCD_D[3]	IO:GPIO[57]	IO:LCD_D[3]	—	—
W30	LCD_D[4]	IO:GPIO[58]	IO:LCD_D[4]	—	—
Y32	LCD_D[5]	IO:GPIO[59]	IO:LCD_D[5]	—	—
Y31	LCD_D[6]	IO:GPIO[60]	IO:LCD_D[6]	—	—
AA31	LCD_D[7]	IO:GPIO[61]	IO:LCD_D[7]	—	—
AA30	LCD_D[8]	IO:GPIO_X[0]	IO:LCD_D[8]	IO:KEY_COL6	O:I2S5_DO
AA29	LCD_D[9]	IO:GPIO_X[1]	IO:LCD_D[9]	IO:KEY_COL7	I:I2S5_DI
AB32	LCD_D[10]	IO:GPIO[62]	IO:LCD_D[10]	—	—
AB31	LCD_D[11]	IO:GPIO[63]	IO:LCD_D[11]	—	—
AC30	LCD_D[12]	IO:GPIO[64]	IO:LCD_D[12]	—	—
AC27	LCD_D[13]	IO:GPIO[65]	IO:LCD_D[13]	—	—
AC26	LCD_D[14]	IO:GPIO[66]	IO:LCD_D[14]	—	—
AD30	LCD_D[15]	IO:GPIO[67]	IO:LCD_D[15]	—	—
AD31	LCD_D[16]	IO:GPIO_X[2]	IO:LCD_D[16]	I:KEY_ROW8	IO:I2S5_LRCK
AE32	LCD_D[17]	IO:GPIO_X[39]	IO:LCD_D[17]	I:KEY_ROW9	IO:I2S5_BCLK
AE31	LCD_D[18]	IO:GPIO[68]	IO:LCD_D[18]	—	—
AE27	LCD_D[19]	IO:GPIO[69]	IO:LCD_D[19]	—	—
AE26	LCD_D[20]	IO:GPIO[70]	IO:LCD_D[20]	—	—
AF31	LCD_D[21]	IO:GPIO[71]	IO:LCD_D[21]	—	—
AG31	LCD_D[22]	IO:GPIO_X[40]	IO:LCD_D[22]	—	—
AG29	LCD_D[23]	IO:GPIO_X[14]	IO:LCD_D[23]	—	—
AG32	LCD_CLK	IO:GPIO_X[15]	O: LCD_CLK	—	—
AG30	LCD_GPIO[0]	IO:GPIO_X[16]	O:LCD_GPIO[0]	—	—
AJ30	LCD_GPIO[1]	IO:GPIO_X[17]	O:LCD_GPIO[1]	—	—
AJ31	LCD_GPIO[2]	IO:GPIO_X[18]	O:LCD_GPIO[2]	—	—
AK31	LCD_GPIO[3]	IO:GPIO_X[10]	O:LCD_GPIO[3]	IO:KEY_COL4	I:SDIOB_CDn
AK32	LCD_GPIO[4]	IO:GPIO_X[11]	O:LCD_GPIO[4]	IO:KEY_COL5	I:SDIOB_WP

1. Mode 0 is the default mode after reset. Strap mode is only used during power up reset.
2. GPIO_X[n] designates second location for GPIO[n].

5. Electrical Specifications

5.1. Absolute Maximum Ratings

Stresses above those listed in the Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 33. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
AVPLL_AVDD1P8	AVPLL 1.8V supply voltage	-0.3	—	1.98	
CPUPLL_AVDD1P8	CPU PLL 1.8V supply voltage	-0.3	—	1.98	V
CPUTSEN_AVDD1P8	CPU TSEN 1.8V supply voltage	-0.3	—	1.98	
KILOOTP_AVDD1P8	OTP supply voltage	-0.3	—	1.98	
M0_AVDD1P8	Memory 1.8V supply voltage	-0.3	—	1.98	
OSC_VDDIO1P8	Crystal oscillator	-0.3	—	1.98	
SYSPLL_AVDD1P8	System PLL 1.8V supply voltage	-0.3	—	1.98	
USB2_AVDD3P3	USB 3.3V Analog supply voltage	-0.3	—	3.63	
USB2_DVDD	USB 0.8V core supply voltage	-0.1	—	1.12	
USB2_VR_AVDD3P3	USB2.0 3.3V supply voltage	-0.3	—	3.63	
USB3_AVDD3P3	USB3 3.3V Analog supply voltage	-0.3	—	3.63	
LCD_VDDIO3P3	I/O supply voltage at 3.3V	-0.3	—	3.63	
VDDIO1P8	I/O supply voltage at 1.8V	-0.3	—	1.98	
VDD_CORE	Core supply voltage	-0.1	—	1.12	
VDDQ	DDR3/DDR3L/DDR4 supply voltage	-0.5	—	1.65	
V_{IN}	TW0_SCL, TW0_SDA, TW1_SCL, TW1_SDA, TW2_SCL, TW2_SDA, TW3_SCL, TW3_SDA	-0.3	—	1.98	
	Other 1.8V digital IO pins	-0.3	—	1.98 or VDDIO1P8+0.3, whichever is lower	
V_{OUT}	TW0_SCL, TW0_SDA, TW1_SCL, TW1_SDA, TW2_SCL, TW2_SDA, TW3_SCL, TW3_SDA	-0.3	—	1.98	
	Other 1.8V digital IO pins	-0.3	—	1.98 or VDDIO1P8+0.3, whichever is lower	
$T_{STORAGE}$	Storage temperature	-55	—	125	°C
I_{DIS}	VDD_CORE_FB discharge current [1]	—	—	5	mA

1. Recommend disabling external fast discharge voltage at VDD_CORE_FB.

5.2. Recommended Operating Conditions

Table 34. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
CPUPLL_AVDD1P8	CPU PLL 1.8V supply voltage	—	1.71	1.8	1.89	V
CPUTSEN_AVDD1P8	CPU TSEN 1.8V supply voltage	—	1.71	1.8	1.89	
KILOOTP_AVDD1P8	OTP supply voltage	—	1.71	1.8	1.89	
M0_AVDD1P8	Memory 1.8V supply voltage	—	1.71	1.8	1.89	
OSC_VDDIO1P8	Crystal oscillator	—	1.71	1.8	1.89	
SYSPLL_AVDD1P8	System PLL 1.8V supply voltage	—	1.71	1.8	1.89	
USB2_AVDD3P3	USB 3.3V Analog supply voltage	—	3.135	—	3.465	
USB2_DVDD	USB 0.8V core supply voltage	Consumer	0.744	—	1.0	
		Industrial	0.72	—	1.003	
USB2_VR_AVDD3P3	USB 3.3V supply voltage	—	3.135	—	3.465	
USB3_AVDD3P3	3.3V Analog supply voltage	—	3.135	3.3	3.465	
LCD_VDDIO3P3	I/O supply voltage at 3.3V	—	3.135	3.3	3.465	
VDD_CORE [1]	Core supply voltage	Consumer	0.72	0.8	1.0	
		Industrial	0.72	—	1.003	
VDDIO1P8	I/O supply voltage at 1.8V	—	1.71	1.8	1.89	
VDDQ	I/O supply for DDR3 at 1.5V	—	1.425	—	1.65	
	I/O supply for DDR3L at 1.35V	—	1.283	—	1.49	
	I/O supply for DDR4 at 1.2V	—	1.14	—	1.26	
f_{CLKi}	Reference crystal frequency	—	—	25	—	MHz
T_A [2]	Ambient operating temperature	Consumer	0	—	70	°C
		Industrial	-40	—	85	°C
T_J	Junction temperature	Consumer	0	—	105	°C
		Industrial	-40	—	125	°C
R_{USB2_REXT}	USB 2.0 PHY reference current resistor, connect to AVSS	—	—	200± 1%	—	Ohm
$R_{USB2\_VBUS\_REXT}$	USB 2.0 PHY VBUS external series resistor	—	—	30k± 1%	—	Ohm
R_{M0_CAL}	DDR3/DDR3L/DDR4 reference current resistor, connect to VSS	—	—	240± 1%	—	Ohm

1. The optimum core supply voltage is determined by the individual chip manufacturing process variation. The system software reads an index stored in the on-chip OTP memory and controls the VDD regulator output voltage. The nominal regulation of the VDD regulator should be within ±3%. For details refer to the *PV Compensation Application Note*.
2. The important parameter is maximum junction temperature. The maximum junction temperature needs to be observed in addition to the ambient temperature limits.

5.2.1. Power-up Sequence

Table 35. SL1620 Power-up Requirement

Power-up Timing Parameter	Power Rails	Min	Typ	Max	Units
Slew rate	VDD_CORE	—	—	32	mV/µs
	VDDQ			18	
	M0_AVDD1P8			18	
	USB2_DVDD			18	
	All of AVDD1P8, VDDIO1P8			18	
	All of AVDD3P3/VDDIO3P3			100	
T1-T0	Time duration between VDD_CORE/USB2_DVDD reached 0.8V and all 1.8V power ramp start	0	—	100	ms
T2-T1	Time duration between all 1.8V power rails being stable to all 3.3V ramp start	0	—	—	ms

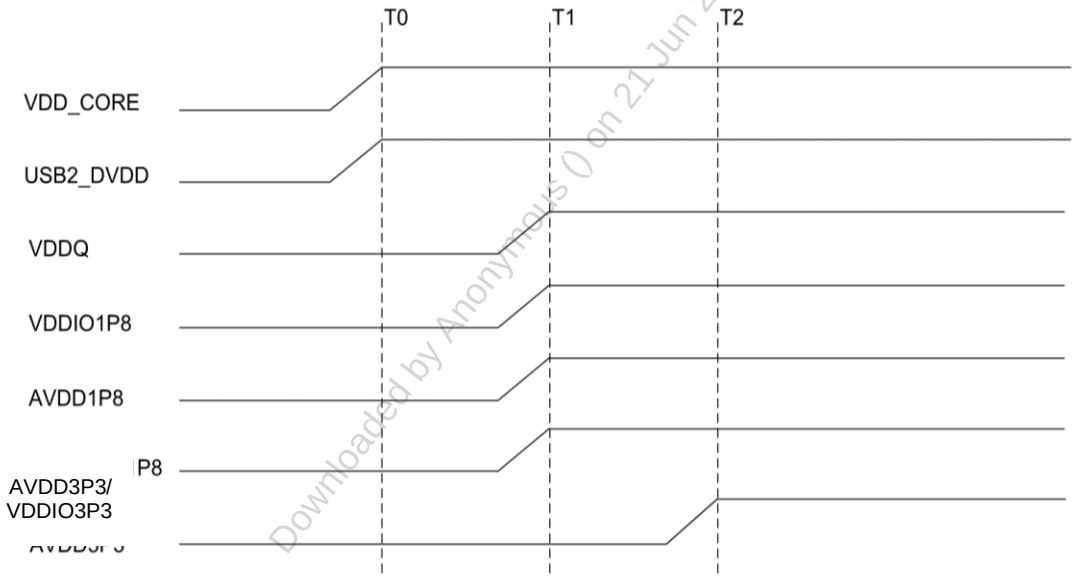


Figure 9. SL1620 Recommended power-up sequence

Notes:

1. All of 1.8V power rails start ramping up (T1) after VDD_CORE/USB2_DVDD reaches its 100% of 0.8V (T0).
2. M0_AVDD1P8, VDDQ and VDDQLP shall follow the power sequence requirement from the DRAM devices if shared with the DRAM. Otherwise, no specific sequence is required between them or relative to other power rails.
3. AVDD3P3/VDDIO3P3 start ramping (T2) after the other SOC power rails have reached their thresholds (T1).

5.3. Crystal Specifications

Table 36. Crystal Specifications

Parameter	Condition	Typical	Unit
Fundamental Frequency	—	25	MHz
Frequency Tolerance	0 – 70 °C (for consumer) -40 – 85 °C (for industrial)	<= ± 50	ppm
Load Capacitance	—	8*	pF
Max. ESR	—	60	Ohm
Drive Level	—	35	uW
Mode of Oscillation	—	Fundamental	—

* For more design details, please contact the Synaptics application engineering team.

5.4. Thermal Conditions for the SL1620 Device 443-pin BGA Package

For more design details, please contact the Synaptics application engineering team.

Table 37. Thermal Conditions[1] for the SL1620 Device

Symbol	Parameter	Condition	Spec.	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1]–junction to ambient of the SL1620 device 443-pin BGA package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	17.001	—	°C/W
			Industrial	—	16.629	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/ sec air flow	Consumer	—	16.564	—	
			Industrial	—	16.564	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/ sec air flow	Consumer	—	14.988	—	
			Industrial	—	14.987	—	
ψ_{JT}	Thermal characteristic parameter[1]–junction to top center of the SL1620 device 443-pin BGA package $\psi_{JT} = (T_J - T_{TOP})/P.$ T_{TOP} = Temperature on the top center of the package	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	0.07684	—	
			Industrial	—	0.0769	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/ sec air flow	Consumer	—	0.07707	—	
			Industrial	—	0.07704	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/ sec air flow	Consumer	—	0.07779	—	
			Industrial	—	0.07777	—	

Symbol	Parameter	Condition	Spec.	Min	Typ	Max	Units
ψ_{JB}	Thermal characteristic parameter[1]–junction to top center of the SL1620 device 443-pin BGA package $\psi_{JB} = (T_J - T_{BOARD})/P$.	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	3.56	—	°C/W
			Industrial	—	3.558	—	
θ_{JC}	Thermal resistance[1]junction to case of the SL1620 device 443-pin BGA package $\theta_{JC} = (T_J - T_C)/ P_{TOP}$ P_{TOP} = Power Dissipation from the top of the package	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	0.318	—	
			Industrial	—	0.318	—	
θ_{JB}	Thermal resistance[1]–junction to board of the SL1620 device 443-pin BGA package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	3.705	—	
			Industrial	—	3.705	—	

1. For definitions and usage of the thermal parameters in this table, refer to *JESD51-12.01*.

5.5. AC and DC Electrical Characteristics

5.5.1. Digital Pins Operating Conditions

5.5.1.1. Digital Pins Operating Conditions for 1.8 V I/Os

Table 38 describes the digital operating conditions for 1.8V I/Os.

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 38. Digital Operating Conditions for 1.8 V I/Os

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	All 1.8V Digital IO pins	—	0.65*VDDIO1P8	—	1.98	V
V_{IL}	Low level input voltage	All 1.8V Digital IO pins	—	-0.3	—	0.35*VDDIO1P8	
V_{T+}	Low to High Threshold Point with Schmitt Trigger enabled	TWO_SCL, TWO_SDA, TW1_SCL, TW1_SDA, TW2_SCL, TW2_SDA, TW3_SCL, TW3_SDA	—	0.98	1.09	1.21	
		POR_EN, RSTIn, TEST_EN, JTAG_SEL, TCK, TRSTn	—	0.95	1.06	1.16	
		SDIO_DATA[3:0] SDIO_CMD	—	1.07	—	—	
		EMMC_DATA[7:0] EMMC_CMD EMMC_STRB	—	1.07	—	—	
V_{T-}	High to Low Threshold Point with Schmitt Trigger enabled	TWO_SCL, TWO_SDA, TW1_SCL, TW1_SDA, TW2_SCL, TW2_SDA, TW3_SCL, TW3_SDA	—	0.76	0.86	0.97	
		POR_EN, RSTIn, TEST_EN, JTAG_SEL, TCK, TRSTn	—	0.68	0.76	0.85	
		SDIO_DATA[3:0] SDIO_CMD					
		EMMC_DATA[7:0]	—	—	—	0.68	

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
		EMMC_CMD EMMC_STRB					
R_{PU}	Pull-up Resistor	TW0_SCL, TW0_SDA, TW1_SCL, TW1_SDA, TW2_SCL, TW2_SDA, TW3_SCL, TW3_SDA	—	32k	48k	79k	Ohm
		POR_EN, RSTIn, TEST_EN, JTAG_SEL, TCK, TRSTn	—	57k	87k	146k	
		Other 1.8V digital IO pins[1]	—	19k	26k	39k	
R_{PD}	Pull-down Resistor	TW0_SCL, TW0_SDA, TW1_SCL, TW1_SDA, TW2_SCL, TW2_SDA, TW3_SCL, TW3_SDA	—	30k	44k	68k	
		POR_EN, RSTIn, TEST_EN, JTAG_SEL, TCK, TRSTn	—	54k	79k	127k	
		Other 1.8V digital IO pins	—	18k	24k	34k	
I_{OL} @ VDDIO-0.45V	DS[3:0]=0000	TW0_SCL TW0_SDA TW1_SCL TW1_SDA TW2_SCL TW2_SDA TW3_SCL TW3_SDA	—	0.7	1.1	1.4	mA
	DS[3:0]=0001			1.1	1.6	2.1	
	DS[3:0]=0010			2.2	3.2	4.1	
	DS[3:0]=0011			3.3	4.8	6.2	
	DS[3:0]=0100			4.4	6.4	8.2	
	DS[3:0]=0101			5.5	7.9	10.2	
	DS[3:0]=0110			6.6	9.5	12.3	
	DS[3:0]=0111			7.7	11.1	14.3	
	DS[3:0]=1000			8.8	12.6	16.2	
	DS[3:0]=1001			9.8	14.2	18.3	
	DS[3:0]=1010			10.9	15.8	20.3	
	DS[3:0]=1011			12	17.4	22.3	
	DS[3:0]=1100			13.1	18.8	24.1	
	DS[3:0]=1101			14.2	20.4	26.1	
	DS[3:0]=1110			15.2	22	28.1	

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
	DS[3:0]=1111			16.3	23.5	30.1	
	DS[2:0]=000	Other 1.8V digital IO pins	—	2.2	3.1	4.1	
	DS[2:0]=001			4.6	6.7	8.7	
	DS[2:0]=010			6.6	9.6	12.5	
	DS[2:0]=011			8.9	12.8	16.7	
	DS[2:0]=100			12.3	17.8	23.1	
	DS[2:0]=101			14.3	20.7	26.8	
	DS[2:0]=110			15.8	22.9	29.6	
	DS[2:0]=111			17.6	25.5	33	
I_{OH} @ VDDIO-0.45V	DS[3:0]=0000	TW0_SCL TW0_SDA TW1_SCL TW1_SDA TW2_SCL TW2_SDA TW3_SCL TW3_SDA	—	0.7	1.1	1.5	mA
	DS[3:0]=0001			1.1	1.7	2.3	
	DS[3:0]=0010			2.2	3.3	4.5	
	DS[3:0]=0011			3.2	5.0	6.7	
	DS[3:0]=0100			4.3	6.6	8.9	
	DS[3:0]=0101			5.4	8.2	11.1	
	DS[3:0]=0110			6.4	9.8	13.2	
	DS[3:0]=0111			7.5	11.5	15.4	
	DS[3:0]=1000			8.5	13.0	17.4	
	DS[3:0]=1001			9.6	14.7	19.6	
	DS[3:0]=1010			10.6	16.3	21.8	
	DS[3:0]=1011			11.7	17.9	23.9	
	DS[3:0]=1100			12.7	19.4	25.9	
	DS[3:0]=1101			13.8	21.0	28.0	
	DS[3:0]=1110			14.8	22.6	30.0	
	DS[3:0]=1111			15.8	24.2	32.2	
	DS[2:0]=000	Other 1.8V digital IO pins	—	1.8	2.8	3.7	
	DS[2:0]=001			3.9	5.9	7.8	
	DS[2:0]=010			5.6	8.4	11.2	
	DS[2:0]=011			7.5	11.2	15.0	
	DS[2:0]=100			10.4	15.5	20.6	
	DS[2:0]=101			12.0	18.1	23.9	
	DS[2:0]=110			13.3	20.0	26.5	
	DS[2:0]=111			14.8	22.2	29.5	
Input Capacitance	—	—	—	—	—	3.2	pF
I_I	Input Leakage Current	—	V_I=1.8V or 0V	—	—	±10	µA
I_{OZ}	Tri-state Output Leakage	—	V_O=1.8V or 0V	—	—	±10	

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
	Current						

5.5.1.2. Digital Pins Operating Conditions for 3.3 V I/Os

Table 39 describes the digital pins operating conditions for 3.3V I/Os (LCD Parallel interface only).

Table 39. Digital Pins Operating Conditions for 3.3 V I/Os

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	All 3.3V Digital IO pins	—	2	—	3.465	V
V_{IL}	Low level input voltage	All 3.3V Digital IO pins	—	-0.3	—	0.8	
V_{OH}	Output high voltage	All 3.3V Digital IO pins	—	2.4	—	3.465	
V_{ol}	Output low voltage	All 3.3V Digital IO pins	—	-0.3	—	0.4	
V_{T+}	Low to High Threshold Point with Schmitt Trigger enabled	All 3.3V Digital IO pins	—	1.23	1.34	1.46	
V_{T-}	High to Low Threshold Point with Schmitt Trigger enabled	All 3.3V Digital IO pins	—	1.02	1.13	1.26	
R_{PU}	Pull-up Resistor	All 3.3V Digital IO pins	—	24k	29k	34k	Ohm
R_{PD}	Pull-down Resistor	All 3.3V Digital IO pins	—	24k	29k	34k	
Input Capacitance	—	All 3.3V Digital IO pins	—	—	—	3.5	pF
I_I	Input leakage current	All 3.3V Digital IO pins	VI=3.3V or 0V	—	—	±10	µA
I_{OZ}	Tri-state Output Leakage Current	All 3.3V Digital IO pins	V_O=3.3V or 0V	—	—	±10	

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{OL} @ VDDIO-0.4V	DS[3:0]=0000	All 3.3V Digital IO pins	—	1.1	1.6	2.1	mA
	DS[3:0]=0001			2.1	3.1	4.1	
	DS[3:0]=0010			3.2	4.7	6.2	
	DS[3:0]=0011			4.2	6.2	8.2	
	DS[3:0]=0100			5.3	7.8	10.3	
	DS[3:0]=0101			6.4	9.3	12.3	
	DS[3:0]=0110			7.4	10.8	14.3	
	DS[3:0]=0111			8.4	12.3	16.2	
	DS[3:0]=1000			12.6	18.2	24.0	
	DS[3:0]=1001			13.6	19.7	26.0	
	DS[3:0]=1010			14.7	21.3	28.0	
	DS[3:0]=1011			15.7	22.7	29.9	
	DS[3:0]=1100			16.7	24.2	31.9	
	DS[3:0]=1101			17.7	25.7	33.8	
	DS[3:0]=1110			18.8	27.2	35.8	
	DS[3:0]=1111			19.8	28.6	37.6	
I_{Oh} @ VDDIO-2.4V	DS[3:0]=0000	All 3.3V Digital IO pins	—	2.1	3.6	5.2	mA
	DS[3:0]=0001			4.1	6.9	10.1	
	DS[3:0]=0010			6.4	10.7	15.7	
	DS[3:0]=0011			8.1	13.5	19.8	
	DS[3:0]=0100			10.4	17.3	25.4	
	DS[3:0]=0101			12.4	20.6	30.3	
	DS[3:0]=0110			14.4	23.9	35.1	
	DS[3:0]=0111			16.1	26.8	39.3	
	DS[3:0]=1000			24.2	40.1	58.6	
	DS[3:0]=1001			26.2	43.4	63.4	
	DS[3:0]=1010			28.5	47.1	68.8	
	DS[3:0]=1011			30.2	49.1	72.9	
	DS[3:0]=1100			32.1	53.1	77.7	
	DS[3:0]=1101			34.1	56.4	82.4	
	DS[3:0]=1110			36.1	59.6	87.2	
	DS[3:0]=1111			37.8	62.4	91.3	

5.5.2. SD, SDIO Timing

5.5.2.1. SD, SDIO Default Mode Timing Parameters

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 40. SD, SDIO Default Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	25	25	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	10	—	—	ns
t_{WH}	Clock High time	—	10	—	—	
t_{TLH}	Clock Rise time	—	—	—	10	
t_{THL}	Clock Fall time	—	—	—	10	
Inputs CMD, DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	5	—	—	ns
t_{IH}	Input Hold time	—	5	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output delay time	Data Transfer Mode	0	—	14	ns
t_{ODLY}	Output delay time	Identification Mode	0	—	50	

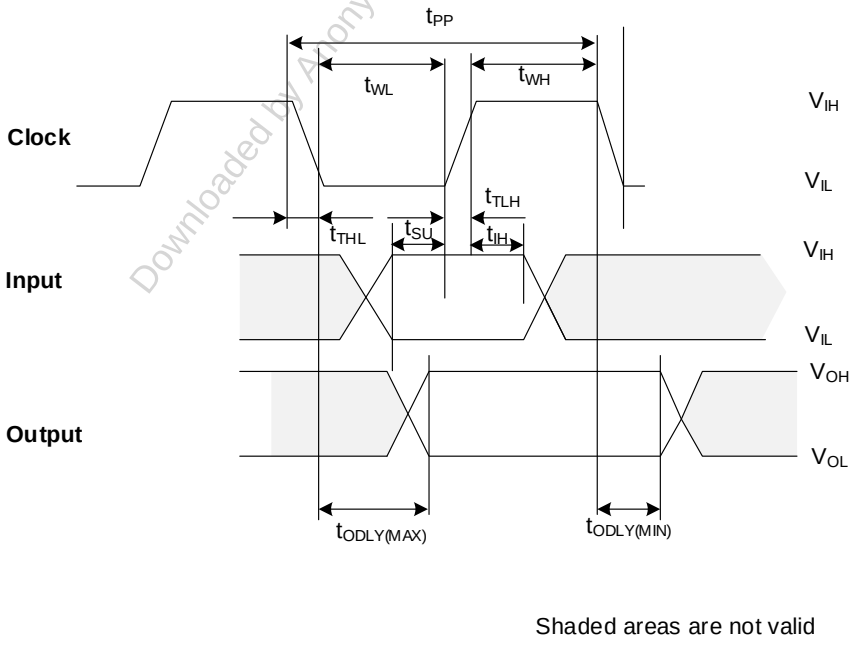


Figure 10. Timing Diagram Data Input/Output Referenced to Clock (Default)

5.5.2.2. SDIO High-Speed Mode Timing Parameters

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 41. SD, SDIO High-Speed Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	50	50	MHz
t_{WL}	Clock Low time	—	7	—	—	ns
t_{WH}	Clock High time	—	7	—	—	
t_{TLH}	Clock Rise time	—	—	—	3	
t_{THL}	Clock Fall time	—	—	—	3	
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	6	—	—	ns
t_{IH}	Input Hold time	—	2	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Delay time	Data Transfer mode	0	—	14	ns
t_{OH}	Output Hold time	—	2.5	—	—	

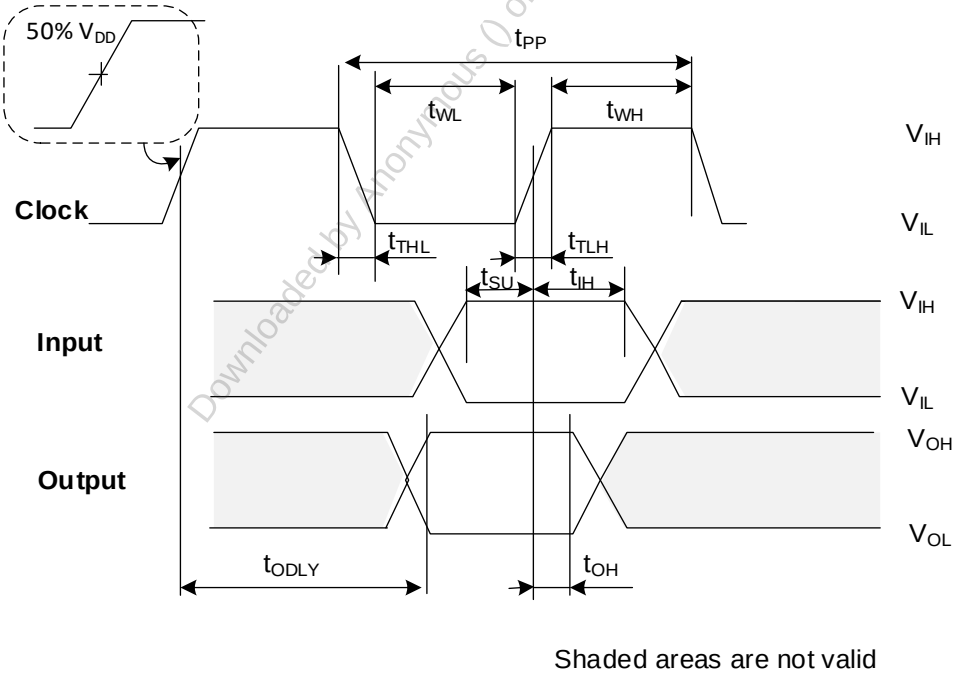


Figure 11. Timing Diagram Data Input/Output Referenced to Clock (High-speed)

5.5.2.3. SDIO SDR104 Mode Timing parameters

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 42. SD, SDIO SDR104 Mode Timing Parameters

Symbol	Parameter		Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	—	0	208	208	MHz
t_{WL}	Clock Low time	—	—	1.44	—	—	ns
t_{WH}	Clock High time	—	—	1.44	—	—	
t_{TLH}	Clock Rise time	—	—	—	—	0.96	
t_{THL}	Clock Fall time	—	—	—	—	0.96	
Inputs DAT (referenced to Clock):							
t_{ISU}	Input Setup time	—	—	—	—	—	ns
t_{IH}	Input Hold time	—	—	—	—	—	

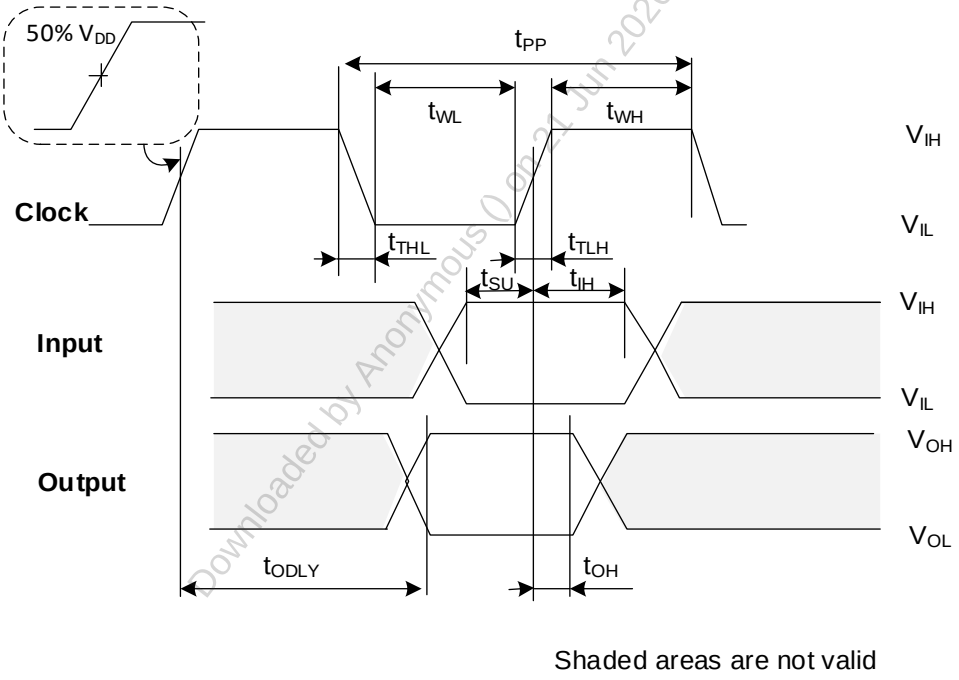


Figure 12. Timing Diagram Data Input/Output Referenced to Clock (High-speed and SDR104 mode)

5.5.3. Two-Wire Serial Interface (TWSI) Timing

5.5.3.1. TWSI Standard and Fast Mode Timing

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 43. TWSI Standard and Fast Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{TWSI_SCL}	SCL Clock Frequency	100 kHz	—	—	100	kHz
		400 kHz	—	—	400	
T_{TWSI_NS}	Noise Suppression Time at SCL, SDA Inputs	100 kHz	—	—	80	ns
		400 kHz	—	—	80	
T_{TWSI_R}	SCL, SDA Rise time	100 kHz	—	—	1000	
		400 kHz	—	—	300	
T_{TWSI_F}	SCL, SDA Fall Time	100 kHz	—	—	300	
		400 kHz	—	—	300	
T_{TWSI_HIGH}	Clock High Period	100 kHz	4000	—	—	
		400 kHz	600	—	—	
T_{TWSI_LOW}	Clock Low Period	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
$T_{TWSI\_SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700	—	—	
		400 kHz	600	—	—	
$T_{TWSI\_HD:STA}$	Start Condition Hold Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
$T_{TWSI\_SU:STO}$	Stop Condition Setup Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
$T_{TWSI\_SU:DAT}$	Data in Setup Time	100 kHz	250	—	—	
		400 kHz	100	—	—	
$T_{TWSI\_HD:DAT}$	Data in Hold Time	100 kHz	300	—	—	
		400 kHz	300	—	—	
T_{TWSI_BUF}	Bus Free Time	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
T_{TWSI_DLY}	SCL Low to SDA Data Out Valid	100 kHz	40	—	200	
		400 kHz	40	—	200	

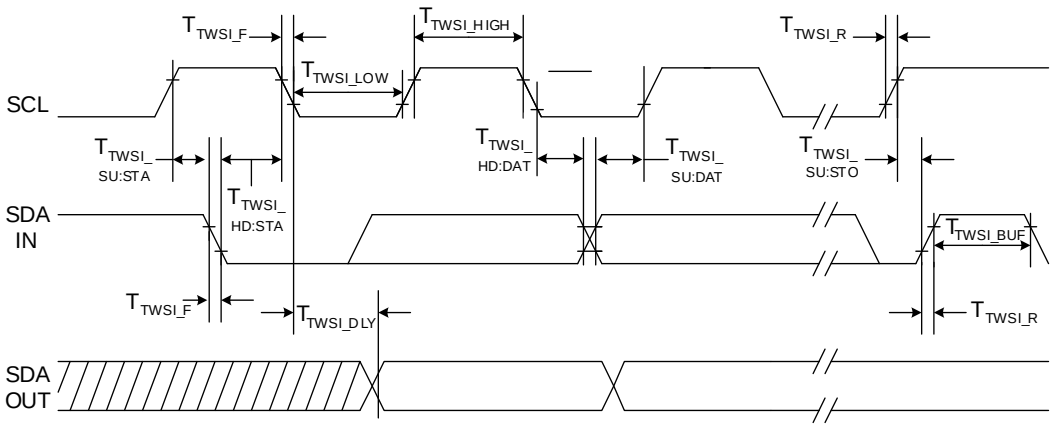


Figure 13. Two-wire serial interface timing

5.5.3.2. TWSI High Speed - transfer rates up to 3.4 Mbits/s

For timing information, refer to the *I2C Bus Specification*.

5.5.4. SPI Timing

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 44. SCLK Cycle Time Configurable Range

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SCLK}	SoC SPI SCLK cycle time	100 MHz SoC SPI controller input clock	20	—	655,340	ns

Table 45. Motorola SPI Mode 0/2 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	The first SPI cycle in a transfer	—	1.5	—	T_{SCLK}
		Subsequent SPI cycles	—	0.5	—	
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	Other than the last SPI cycle	—	0.5	—	
		The last SPI cycle in a transfer	—	1.0	—	
T_{CH}	SCLK high time	—	—	0.5	—	
T_{CL}	SCLK low time	—	—	0.5	—	
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0.5	—	
		If Tx FIFO is empty	2	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	13.8	—	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	0	—	—	
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	T_{SCLK}
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	0.12	—	1.28	ns

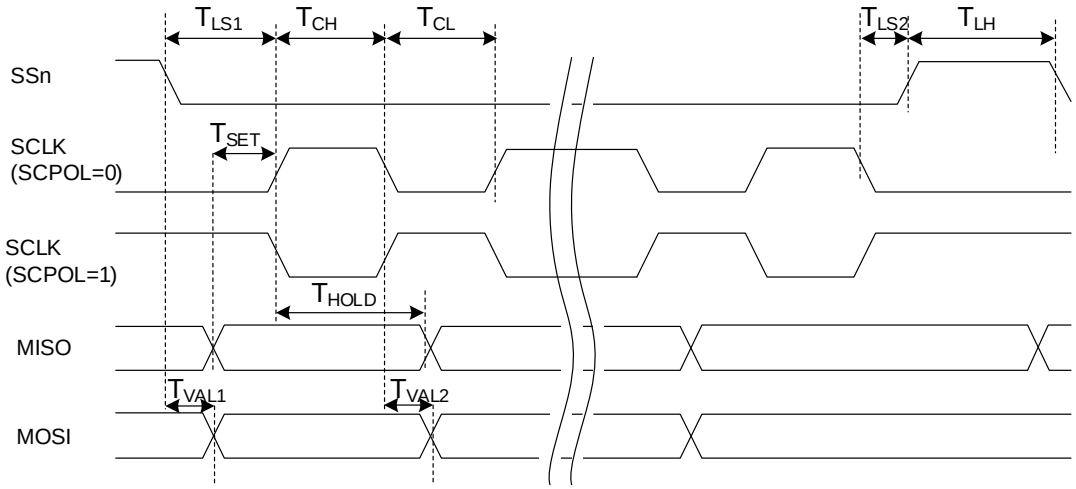


Figure 14. Motorola SPI Mode 0/2 (SCPH = 0)

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 46. Motorola SPI Mode 1/3 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	—	—	1.0	—	TSCLK
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	—	—	1.0	—	
T_{CH}	SCLK high time	—	—	0.5	—	
T_{CL}	SCLK low time	—	—	0.5	—	
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0	—	
		If Tx FIFO is empty	1.5	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	—	30	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	—	30	—	
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	TSCLK
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	—	0.5	—	ns

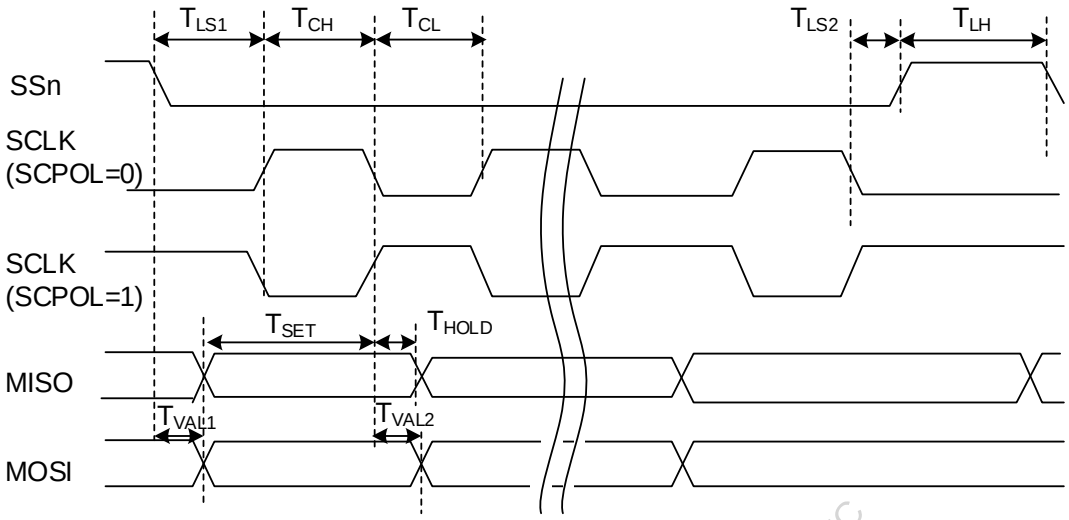


Figure 15. Motorola SPI Mode 1/3 (SCPH = 1)

5.5.5. UART Timing

Table 47. UART Timing

Symbol	Parameter	Condition	Min	Typ[1]	Max	Units
—	Tx bit width	±5%	—	8.68	—	µs
—	Rx bit width	±5%	—	8.68	—	

1. The typical values are for 115.2 kbaud. Other baud rates may vary.

5.5.6. RGMII Timing

Table 48. RGMII Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{skewT}	Data to Clock output Skew (at transmitter)	-500	0	500	ps
T_{skewR}	Clock to Data input Skew (at receiver)	1.0	—	2.6	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T[1]	3.6	4.0	4.4	
T_{RISE}/T_{FALL}	Rise/Fall Time (20–80%)	—	—	0.75	

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{CYCLE} of the lowest speed transitioned between.

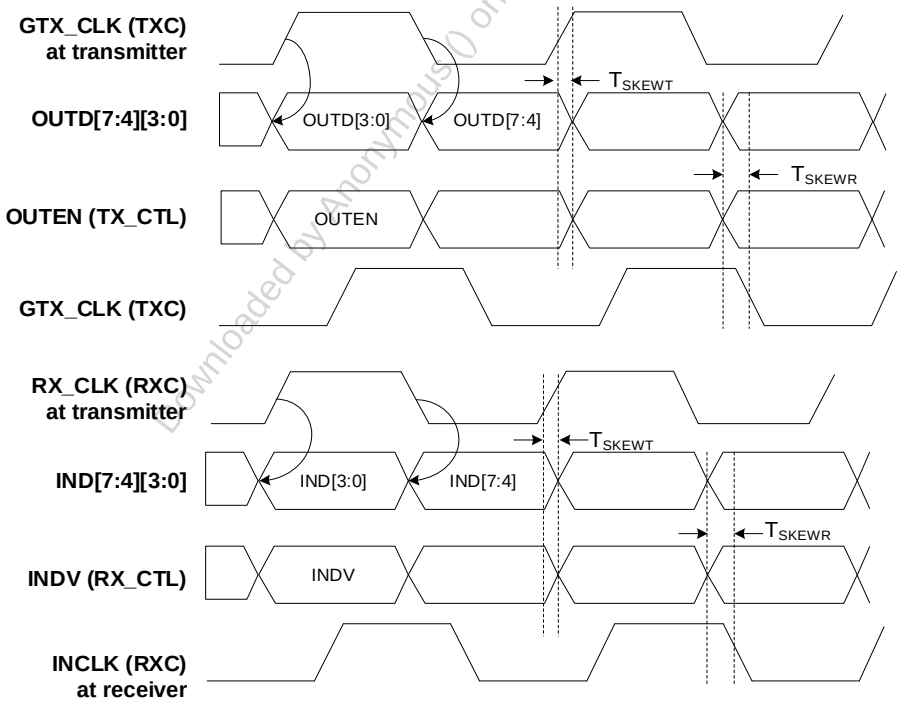


Figure 16. RGMII Timing

5.5.7. JTAG Timing

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 49. JTAG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CLK}	Clock cycle	—	—	200	—	ns
$T_{ISTRSTn}$	Set-up time for TRSTn	—	25%	—	—	Tclk
$T_{IHTRSTn}$	Hold time for TRSTn	—	0	—	—	ns
T_{ISTDI}	Set-up time for TDI	—	30%	—	—	Tclk
T_{IHTDI}	Hold time for TDI	—	0	—	—	ns
T_{OHTDO}	Hold time for TDO	—	0	—	—	ns
T_{OVTDO}	Data valid time for TDO	—	—	—	65%	Tclk
T_{RJT}	Rise time for all I/O	20-80%	10	—	—	ns
T_{FJT}	Fall time for all I/Os	80-20%	10	—	—	ns

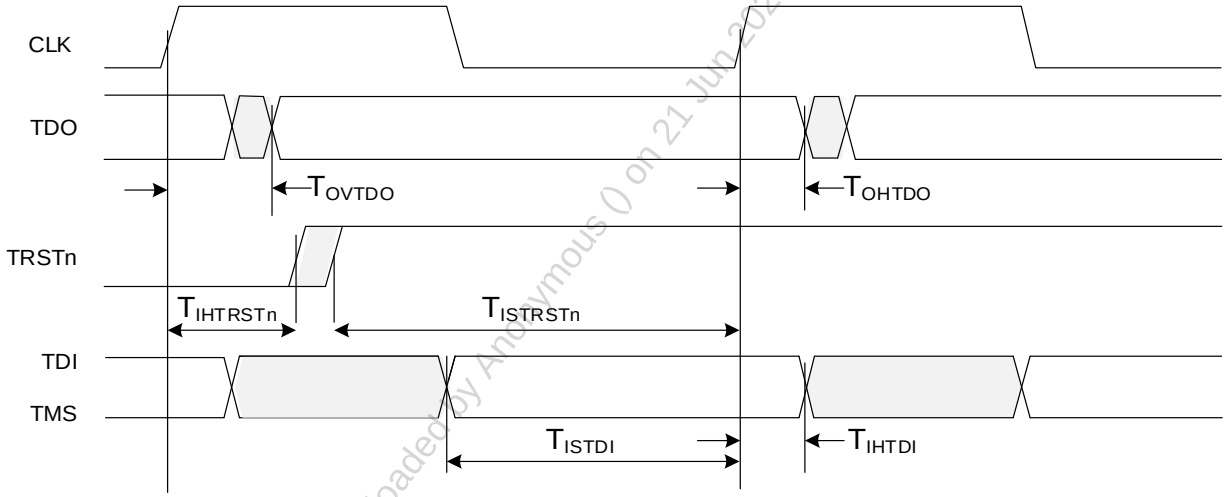


Figure 17. JTAG Timing

5.5.8. I^2S Timing

5.5.8.1. I^2S Host Mode Timing

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 50. I^2S Host Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	16Fs	—	64Fs	Hz
F_{BCLK_PCM}	BCLK Frequency in PCM Mono mode	—	8Fs	—	256Fs	
F_{BCLK_TDM}	BCLK Frequency in TDM mode	—	16Fs	—	256Fs	
F_S	—	—	8	—	192[3]	kHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{SDPD1}	BCLK rising edge to SDATA output valid	—	—	$2^{T}_{AIOSYSCLK}$	—	ns
T_{LRPD}	BCLK rising edge to LRCK valid	—	—	$2^{T}_{AIOSYSCLK}$	—	
T_{SDS}	Set-up time SDATA input with regard to BCLK rising edge	—	—	$-3^{T}_{AIOSYSCLK2}$	—	
T_{SDH}	Hold time SDATA Input with regard to BCLK rising edge	—	—	$4^{T}_{AIOSYSCLK2}$	—	
F_{MCLK}	MCLK (not shown) output frequency	—	6.144	24.576	49.152	MHz
D_{MCLK}	MCLK output duty cycle	—	—	50	—	%

1. BCLK may be inverted for more balanced setup and hold times.
2. Default AIOSYSCLK frequency is 300MHz.
3. 2-channel 384kHz.

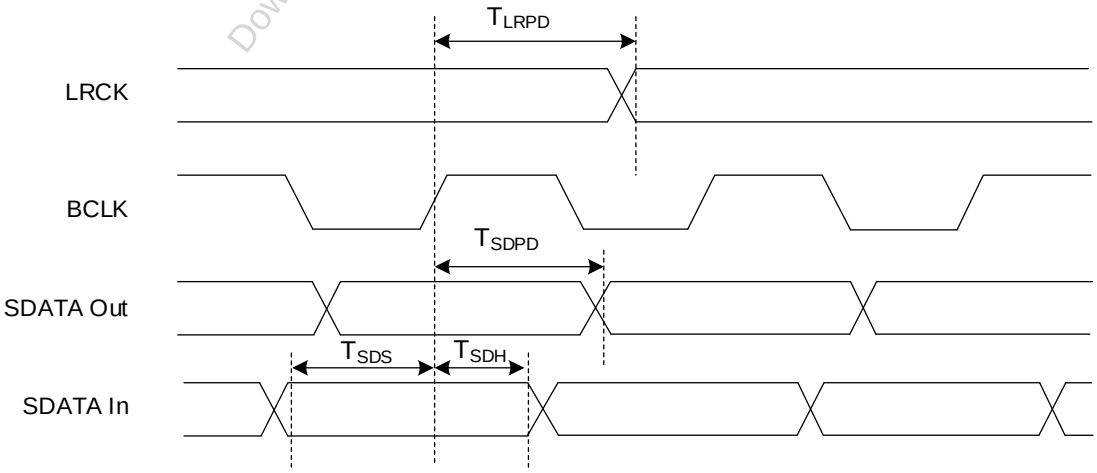


Figure 18. I^2S Host mode timing

5.5.8.2. I²S Target Mode Timing

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 51. I²S Target Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	16Fs	—	64Fs	Hz
F_{BCLK_PCM}	BCLK Frequency in PCM Mono mode	—	8Fs	—	256Fs	
F_{BCLK_TDM}	BCLK Frequency in TDM mode	—	16Fs	—	256Fs	
F_S	—	—	32	—	192	kHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{LRS}	Setup time LRCK input with regard to BCLK active edge	—	—	$-3T_{AIOSYSCLK1}$	—	ns
T_{LRH}	Hold time LRCK input with regard to BCLK active edge	—	—	$4T_{AIOSYSCLK1}$	—	
T_{SDS}	Setup time SDATA Input with regard to BCLK active edge	—	—	$-3T_{AIOSYSCLK1}$	—	
T_{SDH}	Hold time SDATA Input with regard to BCLK active edge	—	—	$4T_{AIOSYSCLK1}$	—	
F_{MCLK}	MCLK (not shown) input frequency	—	—	24.576	49.152	MHz
D_{MCLK}	MCLK input duty cycle	—	—	50	—	%

1. Default AIOSYSCLK frequency is 300MHz.

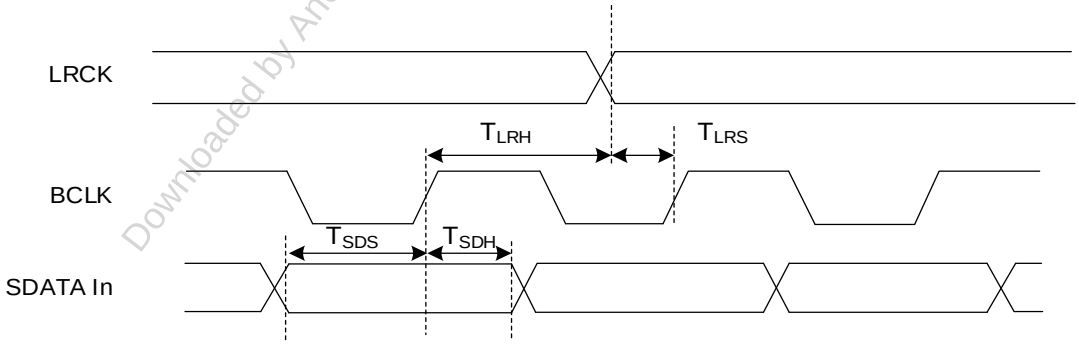


Figure 19. I²S Target mode timing

5.5.9. Pulse-Width Modulation (PWM) Timing

Table 52. PWM Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PERIOD}	PWM	With 2-bit resolution	20 ns	—	81.92 µs	—
		With 16-bit resolution	655.35 µs	—	2.684 s	—
—	PWM Duty Cycle	—	0	—	100	%
—	PWM Duty Cycle Resolution	—	2	—	16	bit

5.5.10. Temperature Sensor

5.5.10.1. Temperature Sensor Electrical Information

Table 53. Temperature Sensor Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Units
ΔT	Temperature Sensing Range[1]	-40		125	°C
	Resolution	—	0.22°C/LSB	—	—
T_{cycle}	Temperature measurement cycle time	—	310	—	µs
	Temperature Sensor IP variation		±5		°C

1. Actual measurement range is limited by the Ambient operating temperature and Maximum junction temperature specified in Table 34. Recommended Operating Conditions.

5.5.11. USB 2.0 Timing

5.5.11.1. USB 2.0 DC Characteristics

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 54. USB 2.0 DC Electrical

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	High (driven)	Note[1]	2.0	—	—	V
V_{IHZ}	High (floating)		2.7	—	3.6	
V_{IL}	Low		—	—	0.8	
V_{DI}	Differential Input Sensitivity	|(D+)-(D-)| Note[1]	0.2	—	—	
V_{CM}	Differential Common Mode Range	Includes VDI range Note[1]	0.8	—	2.5	
Input Levels for High-speed:						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	—	100	—	150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)	—	525	—	625	
V_{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	—	-50	—	500	
Output Levels for Full-speed:						
V_{OL}	Low	Note[1], Note[2]	0.0	—	0.3	V
V_{OH}	High (Driven)	Note[1], Note[3]	2.8	—	3.6	
V_{OSE1}	SE1	—	0.8	—	—	
V_{CRS}	Output Signal Crossover voltage	Note[4]	1.3	—	2.0	
Output Levels for High-speed:						
V_{HSOI}	High-speed idle level	—	-10.0	—	10.0	mV
V_{HSOH}	High-speed data signaling high	—	360	—	440	
V_{HSOL}	High-speed data signaling low	—	-10.0	—	10.0	
V_{CHIRPJ}	Chirp J level (differential voltage)	—	700	—	1100	
V_{CHIRPK}	Chirp K level (differential voltage)	—	-900	—	-500	
Input Capacitance for Full-speed:						
C_{IND}	Downstream Facing Port	Note[5]	—	—	150	pF
C_{INUB}	Upstream Facing Port (without cable)	Note[6]	—	—	100	
C_{EDGE}	Transceiver edge rate control capacitance	—	—	—	75	

Symbol	Parameter	Condition	Min	Typ	Max	Units
Terminations:						
R_{PU}	Bus pull-up Resistor on Upstream facing port	1.5 kOhm ±5%	1.425	—	1.575	kOhm
R_{PD}	Bus pull-down Resistor on Downstream Facing Port	15 kOhm ±5%	14.25	—	15.75	
Z_{INP}	Input impedance exclusive of pullup/pull-down (for full-speed)	—	300	—	—	
V_{TERM}	Termination voltage for upstream facing port pull-up (R_{PU})	—	3.0	—	3.6	V
Termination in High-speed:						
V_{HSTERM}	Termination voltage in high-speed	—	-10	—	10	mV

1. Measured at A or B connector.
2. Measured with RL of 1.425 kohm to 3.6V.3. Measured with RL of 14.25 kohm to GND.
3. Excluding the first transition from the idle state.
4. Measured at A receptacle.6. Measured at B receptacle.

5.5.11.2. USB 2.0 Source Electrical Characteristics

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 55. USB High-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics:						
T_{HSR}	Rise Time (10%–90%)	—	500	—	—	ps
T_{HSF}	Fall Time (10%–90%)	—	500	—	—	
Z_{HSDRV}	Driver Output Resistance (which also serves as high speed termination)	—	40.5	—	49.5	Ohm
Clock Timings:						
T_{HSDRAT}	High-speed Data Rate	—	479.760	—	480.240	Mbps
T_{HSFRAM}	Microframe Interval	—	124.9375	—	125.0625	µs
T_{HSRFI}	Consecutive Microframe Interval Difference	—	—	—	4 highspeed bit times	—

Table 56. USB Full-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics:						
T_{FR}	Rise Time	—	4	—	20	ns
T_{FF}	Fall Time	—	4	—	20	ns
T_{FRFM}	Differential Rise and Fall Time Matching	T_{FR}/T_{FF} Note[1]	90	—	111.11	%
Z_{DRV}	Driver Output Resistance for driver which is not high-speed capable.	—	28	—	44	Ohm
Clock Timings:						
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high speed capable.	Average bit rate	11.9940	—	12.0060	Mbps
T_{FDRATE}	Full-speed Data Rate for devices which are high-speed capable.	Average bit rate	11.9700	—	12.0300	Mbps
T_{FRAME}	Frame Interval	—	0.9995	—	1.0005	ms
T_{RFI}	Consecutive Frame Interval Jitter	No clock adjustment	—	—	42	ns
Full-speed Data Timings:						
T_{DJ1}	Source Jitter Total (including frequency tolerance): To Next Transition	Note[1] Note[2] Note[3]	-3.5	—	3.5	ns
T_{DJ2}	For Paired transitions	Note[4]	-4	—	4	ns
T_{FDEOP}	Source Jitter for Differential Transition to SEO Transition	Note[3]	-2	—	5	ns
T_{JR1}	Receiver jitter: To Next Transition	Note[3]	-18.5	—	18.5	ns
T_{JR2}	For Paired Transitions	—	-9	—	9	ns
T_{FEOPT}	Source SEO interval of EOP	—	160	—	175	ns
T_{FEOPR}	Receiver SEO interval of EOP	Note[5]	82	—	—	ns
T_{FST}	Width of SEO interval during differential transition	—	—	—	14	ns

1. Excluding the first transition from the idle state.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. For both transitions of differential signaling.
5. Must accept as valid EOP.

5.5.12. DDR3 / DDR3L / DDR4 Timing

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

For DDR3 SDRAM specification, refer to *JESD79-3E* standard.

For DDR3L timing specification, refer to *JEDEC 79-3F* and *JEDEC 79-3-1A.01* standard.

For DDR4 SDRAM specification, refer to *JESD209-4A* standard.

5.5.13. eMMC Timing

5.5.13.1. eMMC Timing - Default Bus

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 57. eMMC Timing - Default Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode 3	—	0	—	26	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	10	—	—	ns
t_{WH}	Clock High time	—	10	—	—	
t_{TLH}	Clock Rise time	—	—	—	10	
t_{THL}	Clock Fall time	—	—	—	10	
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	3	—	—	ns
t_{IH}	Input Hold time	—	3	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Delay time	—	3	—	17	ns

5.5.13.2. eMMC Timing - High-Speed Bus

Table 58. eMMC Timing – High-Speed Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	–	0	–	52	MHz
f_{OD}	Clock Frequency Identification Mode	–	0	–	400	kHz
t_{WL}	Clock Low time	–	6.5	–	–	ns
t_{WH}	Clock High time	–	6.5	–	–	
t_{TLH}	Clock Rise time	–	–	–	–	
t_{THL}	Clock Fall time	–	–	–	–	
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	–	2.5	–	–	ns
t_{IH}	Input Hold time	–	2.5	–	–	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Delay time	Data Transfer Mode	3	–	–	ns
t_{RISE}	Signal Rise time	–	–	–	–	
t_{FALL}	Signal Fall time	–	–	–	–	

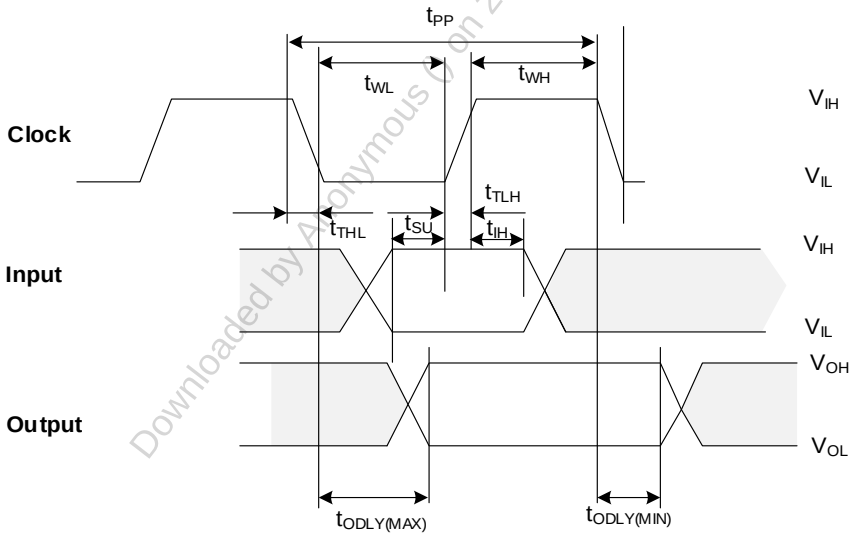


Figure 20. Timing Diagram Data Input/Output Referenced to Clock (Default)

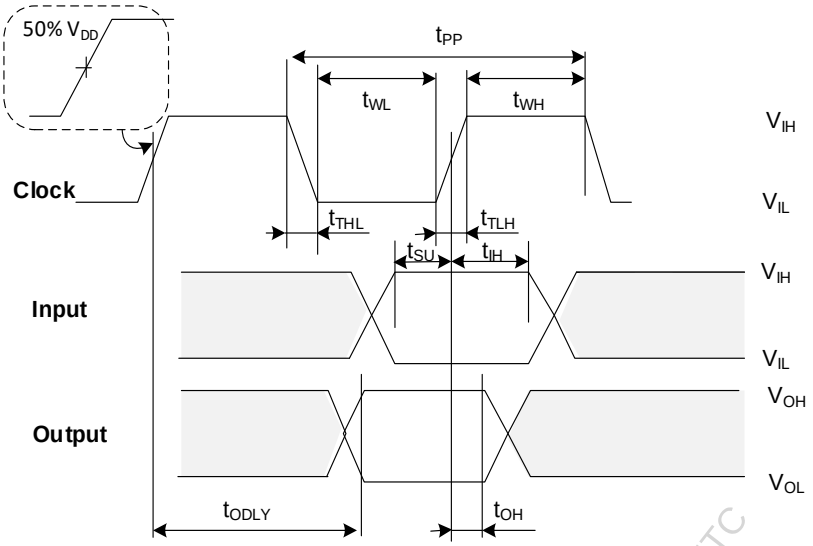


Figure 21. Timing Diagram Data Input/Output Referenced to Clock (High-speed)

5.5.13.3. eMMC Timing - High-Speed Dual Rate Bus

Table 59. eMMC Timing - High-Speed Dual Rate Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
—	Clock Frequency	—	45	—	55	MHz
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	Note[1]	—	—	ns
t_{IH}	Input Hold time	—	Note[1]	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Clock Delay	Data Transfer Mode	Note[1]	—	—	ns
t_{RISE}	Signal Rise Time	—	0.4	—	1.32	
t_{FALL}	Signal Fall Time	—	0.4	—	1.32	

1. Refer to *JEDEC Standard No. 84-B51* for eMMC timing specifications.

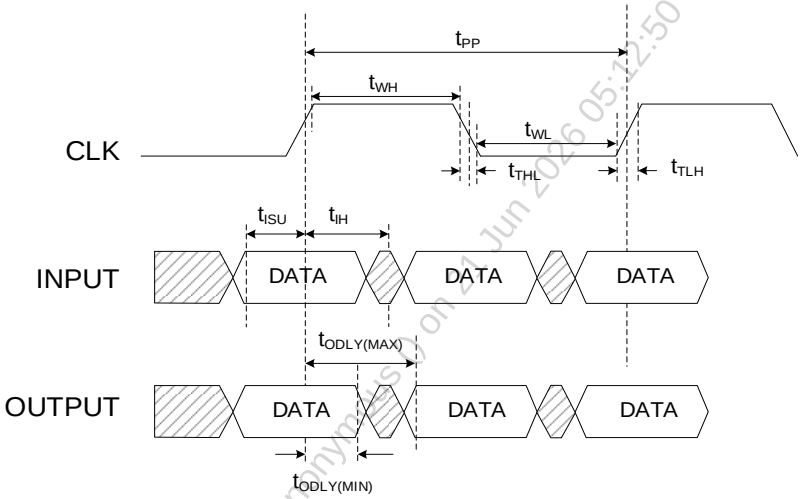


Figure 22. eMMC Timing - High-Speed Dual Rate Interface Timing

5.5.13.4. eMMC Timing - HS200 Mode & HS400 Mode

Refer to JEDEC Standard No. 84-B51 for eMMC timing specifications.

5.5.14. NAND-ONFI Timing

5.5.14.1. NAND-ONFI General Timing

Table 60. NAND-ONFI General Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
—	Output rise time	—	—	—	5	ns
—	Output fall time	—	—	—	5	
—	Peak amplitude for overshoot area	—	—	—	V_{cc}+1.0V	—
—	Overshoot area above Vcc	—	—	—	3.0	—
—	Peak amplitude for undershoot	—	-1.0V	—	—	—
—	Undershoot area below VSS	—	—	—	3.0	V*ns

5.5.14.2. NAND-ONFI Mode 3 Timing

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 61. NAND-ONFI Mode 3 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{ALH}	ALE hold time	—	5	—	—	ns
t_{ALS}	ALE setup time	—	10	—	—	
t_{AR}	ALE to REn delay	—	10	—	—	
t_{CEA}	CEn access time	—	—	—	25	
t_{CH}	CEn hold time	—	5	—	—	
t_{CHZ}	CEn high to output Hi-Z	—	—	—	50	
t_{CLH}	CLE hold time	—	5	—	—	
t_{CLR}	CLE to REn delay	—	10	—	—	
t_{CLS}	CLE setup time	—	10	—	—	
t_{COH}	CEn high to output hold	—	15	—	—	
t_{CS}	CEn setup time	—	25	—	—	
t_{DH}	Data hold time	—	5	—	—	
t_{DS}	Data setup time	—	10	—	—	
t_{IR}	Output Hi-Z to REn low	—	0	—	—	
t_{RC}	REn cycle time	—	30	—	—	
t_{REA}	REn access time	—	—	—	20	
t_{REH}	REn high hold time	—	10	—	—	
t_{RHOH}	REn to output hold	—	15	—	—	
t_{RHW}	REn high to WEn low time	—	—	—	100	
t_{RHZ}	REn high to output Hi-Z	—	100	—	—	
t_{RP}	REn pulse width	—	15	—	—	
t_{RR}	Ready to REn low time (data only)	—	20	—	—	
t_{WB}	WEn to SR[6] low time	—	—	—	100	

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{WC}	WEn cycle time	–	30	–	–	ns
t_{WH}	WEn high hold time	–	10	–	–	
tWHR	WEn high to REn low	–	60	–	–	
tWP	WEn pulse width	–	15	–	–	

5.5.14.3. NAND-ONFI Mode 5 Timing

(Over full range of values listed in Table 34. Recommended Operating Conditions unless otherwise specified.)

Table 62. NAND-ONFI Mode 5 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{ALH}	ALE hold time	–	5	–	–	ns
t_{ALS}	ALE setup time	–	10	–	–	
t_{AR}	ALE to REn delay	–	10	–	–	
t_{CEA}	CEn access time	–	–	–	25	
t_{CH}	CEn hold time	–	5	–	–	
t_{CHZ}	CEn high to output Hi-Z	–	–	–	30	
t_{CLH}	CLE hold time	–	5	–	–	
t_{CLR}	CLE to REn delay	–	10	–	–	
t_{CLS}	CLE setup time	–	10	–	–	
t_{COH}	CEn high to output hold	–	15	–	–	
t_{CS}	CEn setup time	–	15	–	–	
t_{DH}	Data hold time	–	5	–	–	
t_{DS}	Data setup time	–	7	–	–	
t_{IR}	Output Hi-Z to REn low	–	0	–	–	
t_{RC}	REn cycle time	–	20	–	–	
t_{REA}	REn access time	–	–	–	16	
t_{REH}	REn high hold time	–	7	–	–	
t_{RHOH}	REn to output hold	–	15	–	–	
t_{RHW}	REn high to WEn low time	–	100	–	–	
t_{RHZ}	REn high to output Hi-Z	–	–	–	100	
tRP	REn pulse width	–	10	–	–	
tRR	Ready to REn low time (data only)	–	20	–	–	
tWB	WEn to SR[6] low time	–	–	–	100	
tWC	WEn cycle time	–	20	–	–	
tWH	WEn high hold time	–	7	–	–	
tWHR	WEn high to REn low	–	60	–	–	
tWP	WEn pulse width	–	10	–	–	

The requirements for the R/B# signal only apply to commands where R/B# is cleared to zero after the command is issued, as specified in the command definitions.

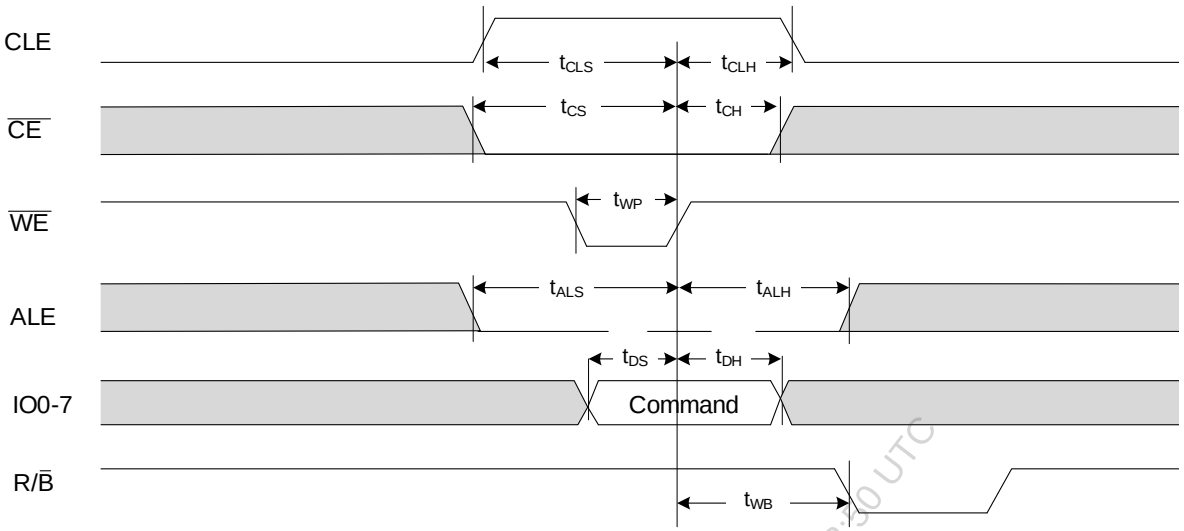


Figure 23. Command latch timing

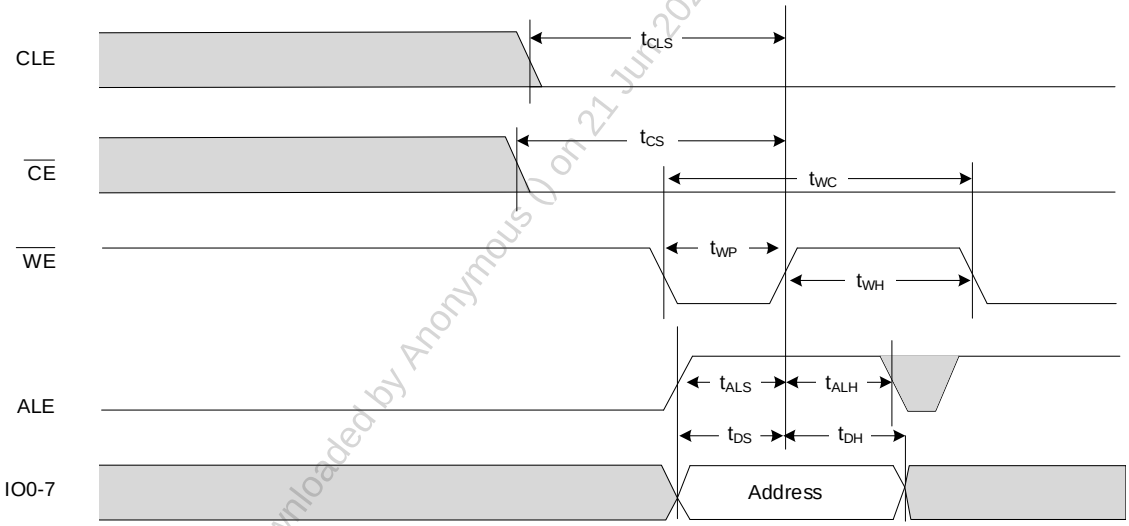


Figure 24. Address latch timing

Data input may be used with CE# don't care. However, if CE# don't care is used, t_{CS} and t_{CH} timing requirements shall be met by the host.

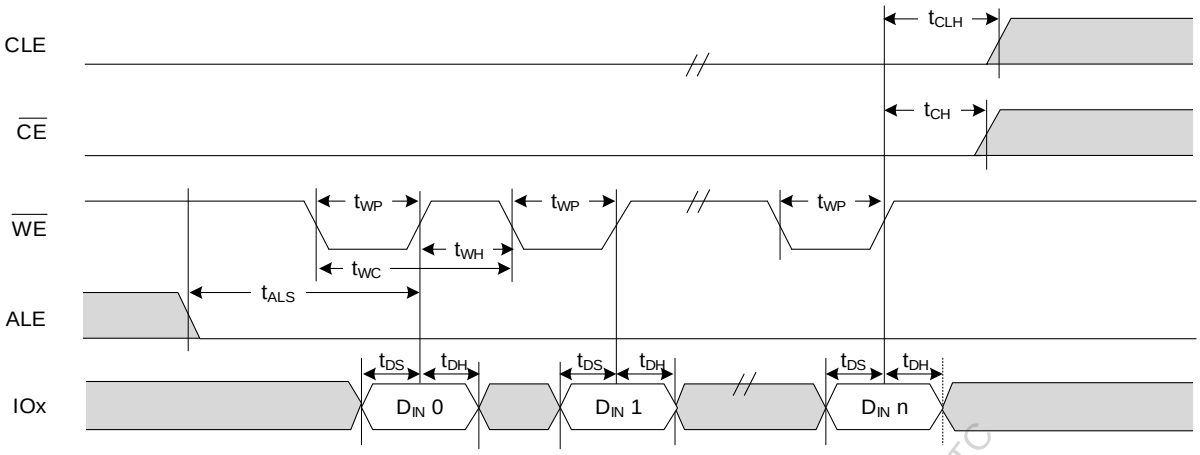


Figure 25. Data Input Cycle Timing

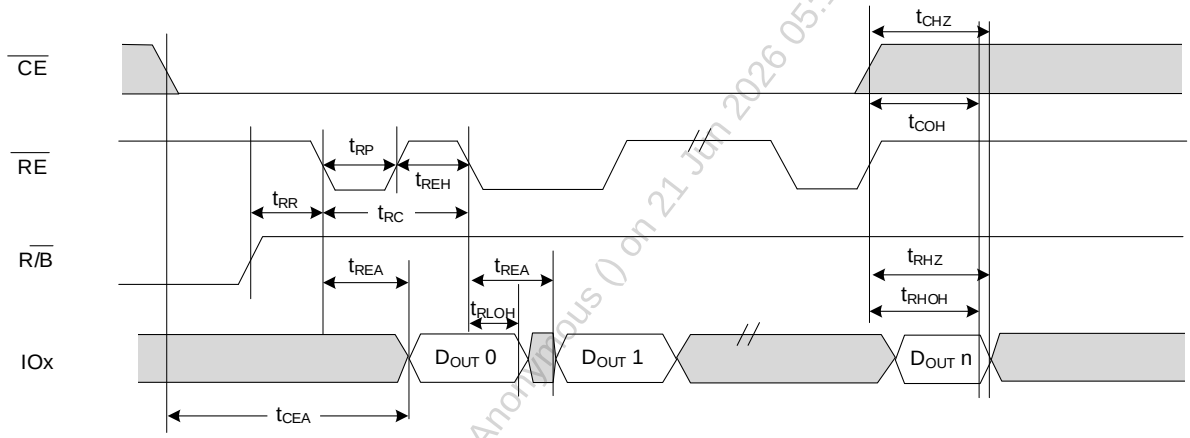


Figure 26. EDO Data Output Cycle Timing

Data output may be used with CE # don't care. However, if CE# don't care is used, t_{CEA} and t_{COH} timing requirements shall be met by the host.

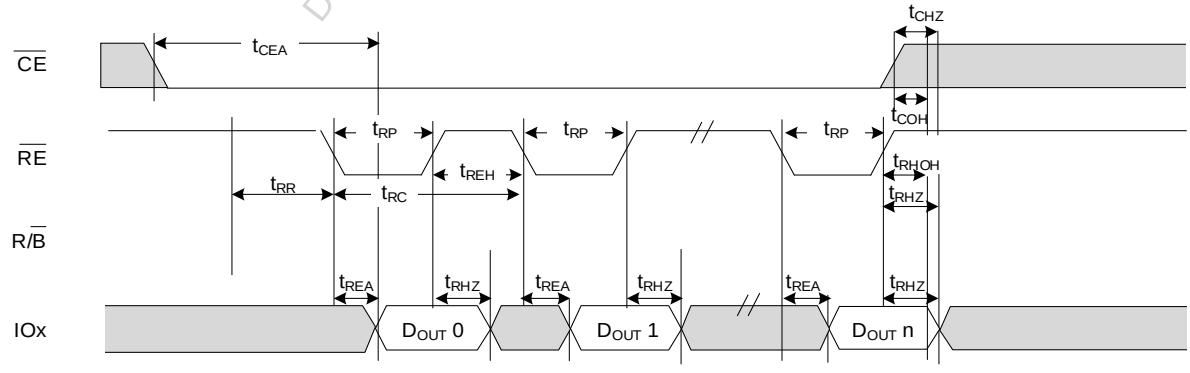


Figure 27. Data Output Cycle Timing

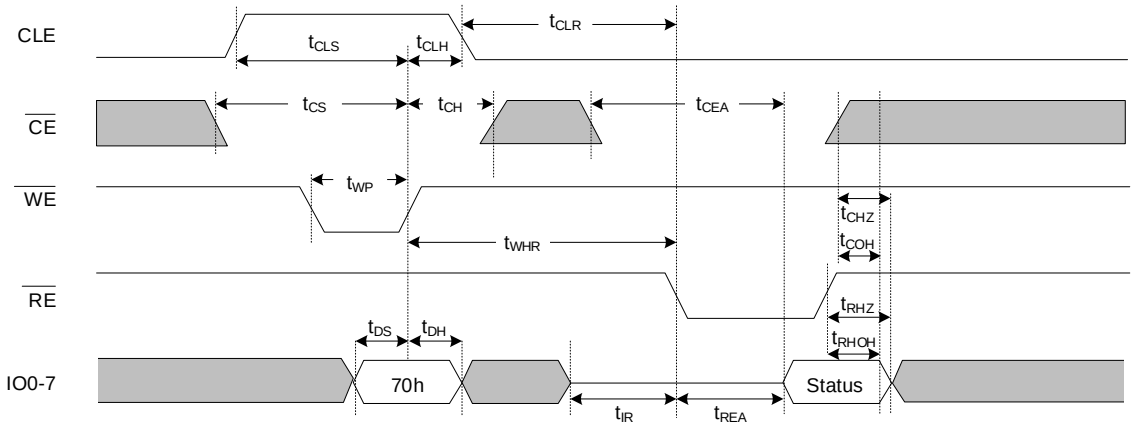


Figure 28. Read Status Timing

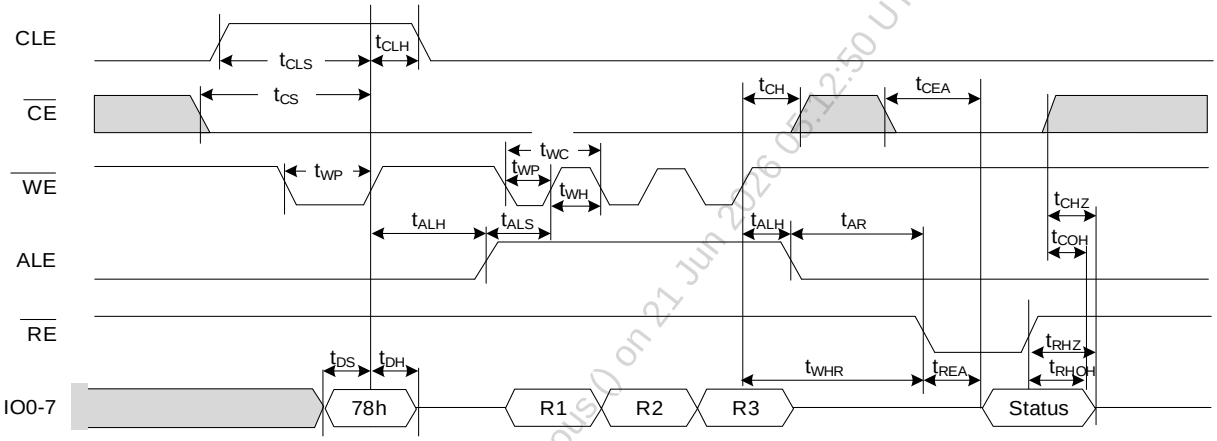


Figure 29. Read Status Enhanced Timing

5.5.15. MIPI DSI Characteristics

5.5.15.1. Input DC Specifications

Table 63 describes the Input DC Specifications.

Table 63. Input DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
Apply to DATAOP/N Inputs:						
V_I	Input signal voltage range	—	-50	—	1350	mV
I_{LEAK}	Input leakage current	$V_{GNDSH(min)} \le V_I \le V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP receive mode	-10	—	10	µA
V_{GNDSH}	Ground shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Transient pin voltage level	—	-0.15	—	1.45	V
$t_{VOH(absmax)}$	Maximum transient time above $V_{OH(absmax)}$	—	—	—	20	ns

5.5.15.2. MIPI DSI HS Line Drivers DC Specifications

Table 64. MIPI DSI HS Line Drivers DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω ≤ R_L ≤ 125 Ω	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω ≤ R_L ≤ 125 Ω	—	—	14	
V_{CMTX}	Steady-state common-mode output voltage	80 Ω ≤ R_L ≤ 125 Ω	150	200	250	
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	80 Ω ≤ R_L ≤ 125 Ω	—	—	5	
V_{OHHS}	HS output high voltage	80 Ω ≤ R_L ≤ 125 Ω	—	—	360	
Z_{OS}	Single-ended output impedance	—	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch	—	—	—	10	%

5.5.15.3. MIPI DSI LP Line Drivers DC Specifications

Table 65. MIPI DSI LP Line Drivers DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Output low-level SE voltage	—	-50	—	50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance	—	110	—	—	Ω
$\Delta Z_{OLP(01,10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$\Delta Z_{OLP(00,11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%

5.5.15.4. MIPI DSI LP Line Receiver DC Specifications

Table 66. MIPI DSI LP Line Receiver DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input low voltage, not in ULPS	—	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULPS	—	—	—	300	
V_{IH}	Input high voltage	—	740	—	—	
V_{HYST}	Input hysteresis	—	25	—	—	

5.5.15.5. MIPI DSI Contention Line Receiver DC Specifications

Table 67. MIPI DSI Contention Line Receiver DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ILF}	Input low fault threshold	—	—	—	200	mV
V_{IHF}	Input high fault threshold	—	450	—	—	

5.5.15.6. MIPI DSI Clock Signal and Data-Clock Timing Specifications

Table 68. MIPI DSI Clock Timing

Symbol	Parameter	Min	Typ	Max	Units	Notes
—	Maximum Serial Data rate (forward direction)	80	—	2500	Mbps	Condition: On DATAP/N outputs. 80 Ω ≤ R_L ≤ 125 Ω
F_{DDRCLK}	DDR CLK frequency	40	—	1250	MHz	Condition: On CLKP/N outputs.
T_{DDRCLK}	DDR CLK period	0.8	—	25	ns	Condition: 80 Ω ≤ R_L ≤ 125 Ω
UI_{INST}	UI instantaneous	0.4	—	12.5	ns	The Max value corresponds to a minimum Mbps data rate.
ΔUI	UI variation	-10%	—	10%	UI	—
t_{CDC}	DDR CLK duty cycle	—	50	—	%	Condition: t_{CDC} = t_{CPH} / T_{DDRCLK}
t_{CPH}	DDR CLK high time	—	1	—	UI	—
t_{CPL}	DDR CLK low time	—	1	—	UI	—

5.5.15.7. MIPI DSI HS Line Drivers AC Specifications

Table 69. MIPI DSI HS Line Drivers AC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_r	Differential output signal rise time	—	—	0.30	UI	Condition: 20% to 80%, R_L = 50 Ω For PHY operating at or below 1Gbps
		—	—	0.35	UI	For PHY operating above 1Gbps and below or at 1.5Gbps
		100	—	—	ps	For PHY operating below or at 1.5Gbps
t_f	Differential output signal fall time	—	—	0.30	UI	Condition: 20% to 80%, R_L = 50 Ω For PHY operating at or below 1Gbps
		—	—	0.35	UI	For PHY operating above 1Gbps and below or at 1.5Gbps
		100	—	—	ps	For PHY operating below or at 1.5Gbps

5.5.15.8. MIPI DSI LP Line Driver and Receiver AC Specifications

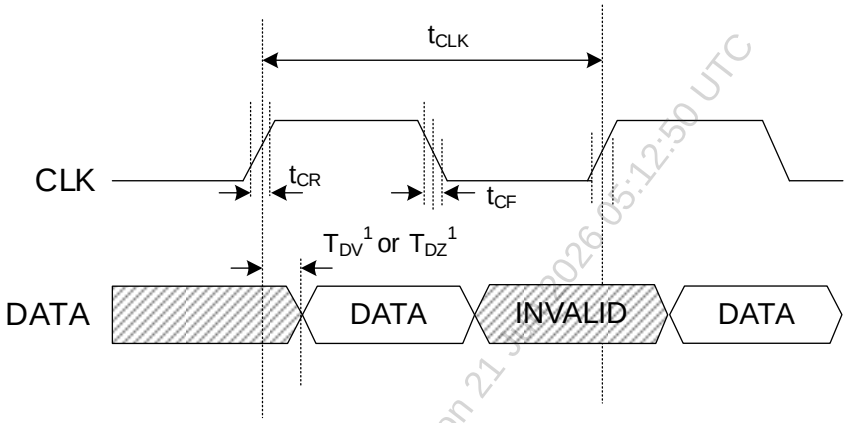
For MIPI DSI LP line driver and receiver AC specifications, refer to the *MIPI D-PHY Specification v2*.

5.5.16. Pulse Density Modulation

Table 70. Pulse Density Modulation (Classic PDM) Timing Parameters – SDR Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{CLK}	PDM Clock	—	—	—	FAIOSYSCLK/ 4[1]	MHz
tD	Clock Duty Cycle	—	—	50	—	%
t_{CR}	Clock Rise Time	10–90%	—	—	TAIOSYSCLK	ns
t_{CF}	Clock Fall Time	90–10%	—	—	TAIOSYSCLK	

1. Default $F_{AIOSYSCLK}$ is 300MHz.



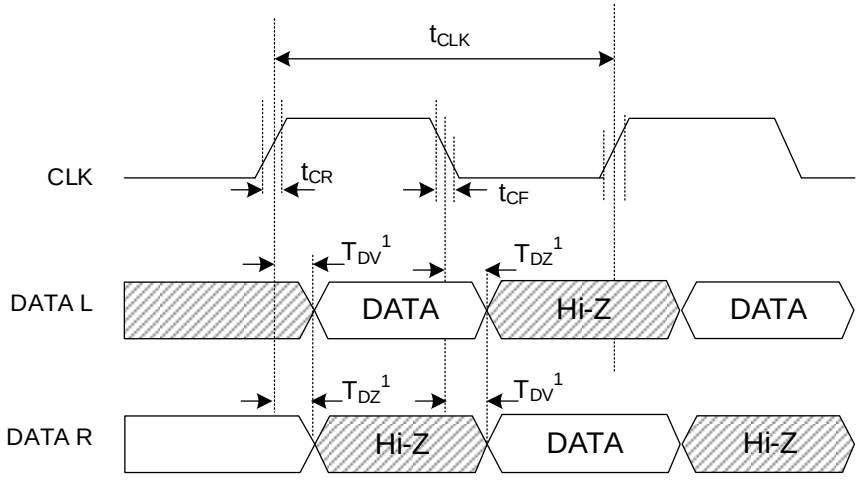
1. PDM data sampling point is configurable across the t_{CLK} period.

Figure 30. PDM Timing – SDR Mode

Table 71. Pulse Density Modulation (Half Cycle PDM) Timing Parameters – DDR Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{CLK}	PDM Clock	—	—	—	$F_{AIOSYSCLK}/4_1$	MHz
tD	Clock Duty Cycle	—	—	50	—	%
t_{CR}	Clock Rise Time	10–90%	—	—	TAIOSYSCLK	ns
t_{CF}	Clock Fall Time	90–10%	—	—	TAIOSYSCLK	

1. Default $F_{AIOSYSCLK}$ is 300MHz.



1. PDM data sampling point is configurable across the t_{CLK} period.

Figure 31. PDM Timing - DDR Mode

6. Display Connection

6.1. LCD with Display Serial Interface (MIPI)

SL1620 supports interfaces for several types of LCD panels. This section describes the hardware connectivity required for each of the supported interfaces .

Figure 32 shows an example of an LCD with DSI connectivity.

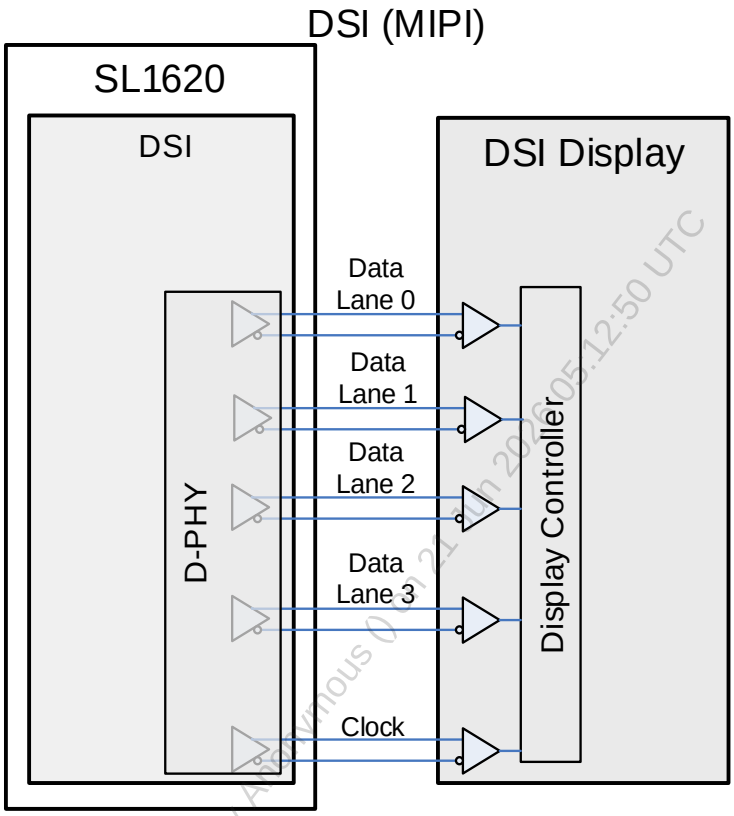


Figure 32. DSI Connectivity

6.2. TFT Interface

Figure 33 shows connectivity for the TFT interface.

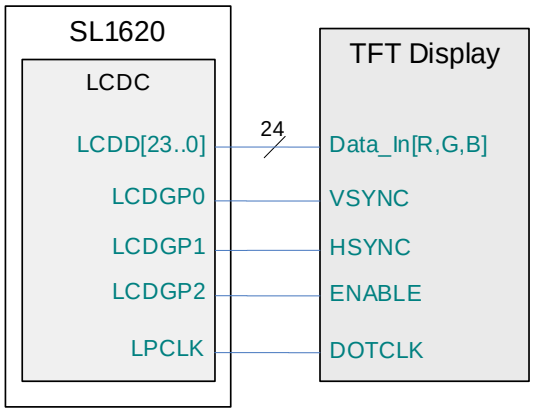


Figure 33. LCDC TFT Interface Connectivity

Table 72 summarizes the data out (LD[23:0]) connectivity for different TFT display configurations.

Table 72. TFT LD[23:0] Connectivity

Interface	BGR	LD[23:0]		
{ GPMUX18B, GPMUX16B }=			2'b1x	2'b00
18-bit Interface (DISPTYPE=0)	BGR = 0	LCDD[23:16] = LCDD[15:8] = LCDD[7:0] =	{ R[7:2], R[7:6] } { G[7:2], G[7:6] } { B[7:2], B[7:6] }	{ 6'd0, R[7:6] } { R[5:2], G[7:4] } { G[3:2], B[7:2] }
	BGR = 1	LCDD[23:16] = LCDD[15:8] = LCDD[7:0] =	{ B[7:2], B[7:6] } { G[7:2], G[7:6] } { R[7:2], R[7:6] }	{ 6'd0, B[7:6] } { B[5:2], G[7:4] } { G[3:2], R[7:2] }
{ GPMUX18B, GPMUX16B }=			2'b01	2'b00
16-bit Interface (DISPTYPE=0)	BGR = 0	LCDD[23:16] = LCDD[15:8] = LCDD[7:0] =	{ R[7:3], R[7:5] } { G[7:2], G[7:6] } { B[7:3], B[7:5] }	Same as 18b I/F above.
	BGR = 1	LCDD[23:16] = LCDD[15:8] = LCDD[7:0] =	{ B[7:3], B[7:5] } { G[7:2], G[7:6] } { R[7:3], R[7:5] }	Same as 18b I/F above.
24-bit Interface (DISPTYPE=1)	BGR = 0	LCDD[23:0] = { R[7:0], G[7:0], B[7:0] }		
	BGR = 1	LCDD[23:0] = { B[7:0], G[7:0], R[7:0] }		

6.3. CPU-Type Interface

Figure 34 and Figure 35 show the connectivity for 68-type and 80-type CPU interfaces.

6.3.1. 68-Type CPU Interface

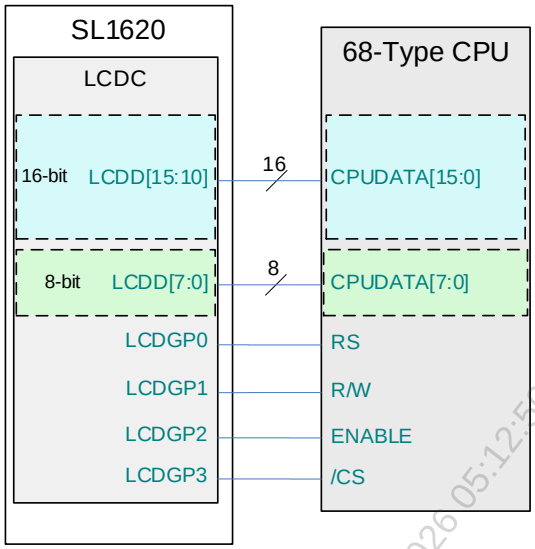


Figure 34. 68-Type CPU Interface, One 16-Bit and One 8-Bit Bus

6.3.2. 80-Type CPU Interface

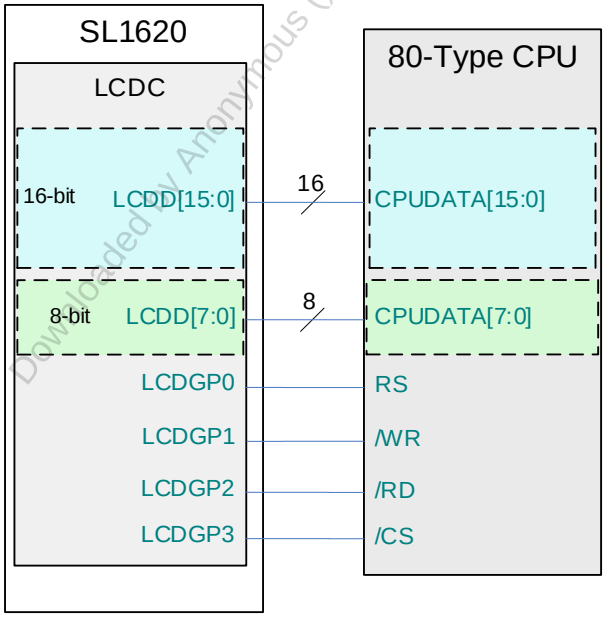


Figure 35. 80-Type CPU Interface, One 16-Bit and One 8-Bit Bus

6.4. LCDC Pinout Mapping Summary

Table 73 summarizes the different output mapping options for each interface.

Table 73. LCDC Pinout Mapping Summary

Name		GP	TFT24	TFT181	TFT162	68-Type CPU	80-Type CPU
LCD_CLK		LCD_CLK	LCD_CLK	LCD_CLK	LCD_CLK	—	—
LCDGP0		GP0	LVSYNC	LVSYNC	LVSYNC	CPU-type GP0	
						RS	
LCDGP1		GP1	LHSYNC	LHSYNC	LHSYNC	CPU-type GP1	
						R/W	/WR
LCDGP2		GP2	LDENA	LDENA	LDENA	CPU-type GP2	
						ENABLE	/RD
LCDGP3		GP3	—	—	—	CPU-type GP3	
						/CS	
LCDGP4		GP4	—	—	—	—	—
LCDD[23:0][3]	LCDD[23:16] LCDD[15:8] LCDD[7:0]	—	R[7:0] G[7:0] B[7:0]	—	—	—	
	LCDD[23:18] LCDD[17:16] LCDD[15:10] LCDD[9:8] LCDD[7:2] LCDD[1:0]	—	—	R[7:2] R[7:6] G[7:2] G[7:6] B[7:2] B[7:6]	—	—	
	LCDD[15:11] LCDD[10:5] LCDD[4:0]	—	—	—	R[7:3] G[7:2] B[7:3]	CPUDATA[15:11] CPUDATA[10:5] CPUDATA[4:0]	
	LCDD[7:0]	—	—	—	—	CPUDATA[7:0]	

1. Assuming GPMUX18B=1.
2. Assuming GPMUX18B=0 and GPMUX16B=1.
3. The name “LCDD” replaces the former name “LD”.

7. Mechanical Drawing

7.1. SL1620 Package Drawing

Note: The drawings in Figure 36, Figure 37, and Figure 38 are not to scale.

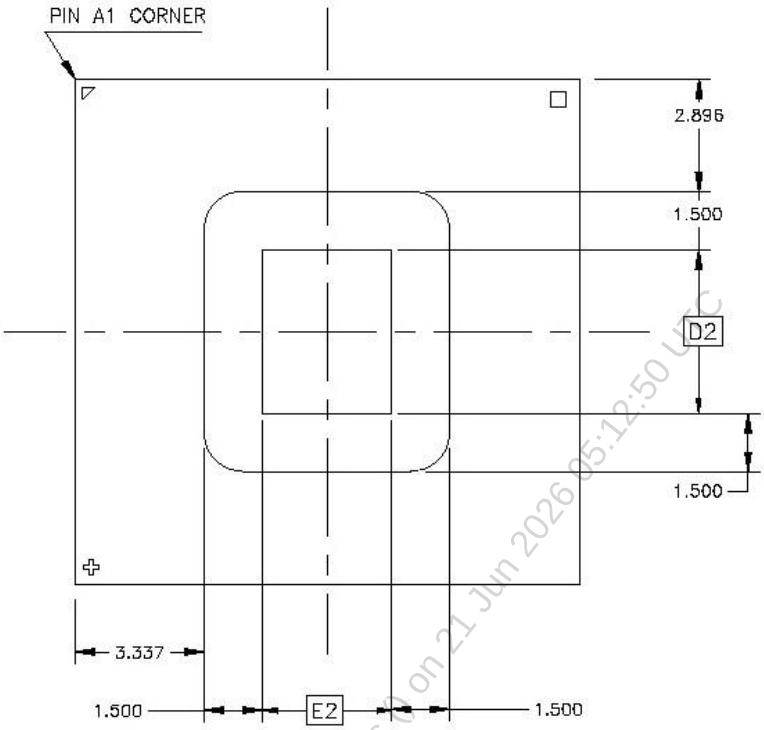


Figure 36. SL1620 Top View

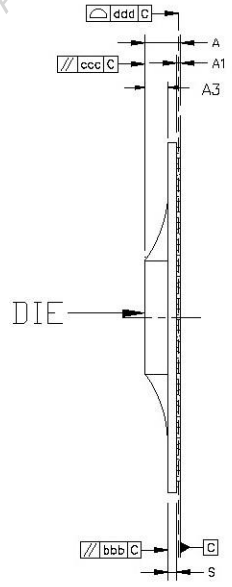


Figure 37. SL1620 Side View

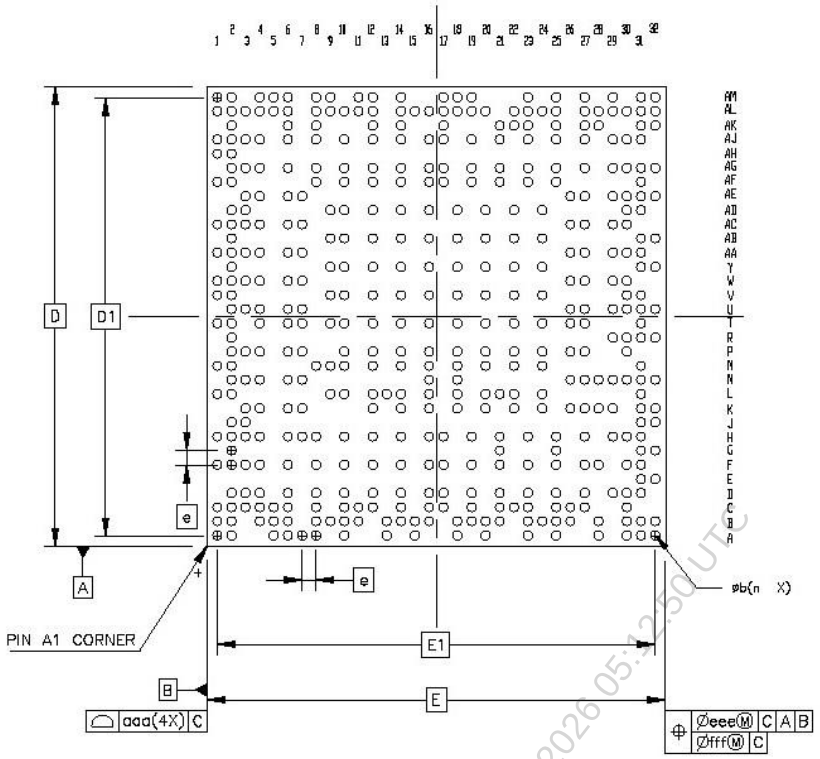


Figure 38. SL1620 Bottom View

Table 74. SL1620 Dimensions (in mm)

Dimension	Symbol	Common Dimensions		
		Min.	Nom.	Max.
Total Thickness	A	1.230	1.320	1.430
Stand Off	A1	0.120	—	0.220
Substrate Thickness	S	0.300 REF		
Thickness from Substrate Surface to Die Backside	A3	0.850 REF		
Body Size	E	13 BSC		
	D	13 BSC		
Ball Diameter		0.250		
Ball Width	b	0.200	—	0.300
Ball Pitch	e	0.400 BSC		
Ball Count	n	443		
Edge Ball Center to Center	E1	12.4 BSC		
	D1	12.4 BSC		
Expose Die Size	E2	3.325 BSC		
	D2	4.207 BSC		
Package Edge Tolerance	aaa	0.100		
Substrate Parallelism	bbb	0.200		
Top Parallelism	ccc	0.200		
Coplanarity	ddd	0.080		
Ball Offset (Package)	eee	0.150		
Ball Offset (Ball)	fff	0.050		

8. Part Order Numbering / Package Marking

8.1. Part Order Numbering

Table 75 provides a list of the available options for ordering.

Table 75. SL1620 Part Order Options

Package Type	Part Number	Description
443-pin FCBGA	SL1620B0-BYOXSZZ-T000-T	Consumer grade: Available now.
443-pin FCBGA	SL1620B0-BYOXSZZ-H000-T	Industrial grade: Available now.
443-pin FCBGA	SL1620B1-BYOXSZZ-T000-T	Consumer grade: Available now.
443-pin FCBGA	SL1620B1-BYOXSZZ-H000-T	Industrial grade: Available now.

8.2. Package Marking

Figure 39 shows a sample package marking and pin 1 location for the SL1620 device.

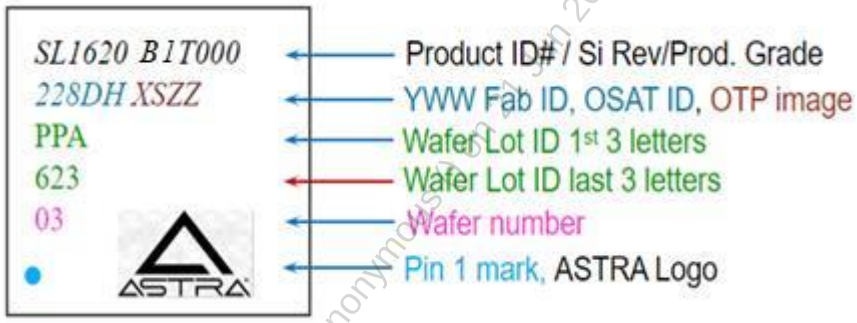


Figure 39. Package Marking and Pin 1 Location

9. References

- MIPI D-PHY Specification v2
- JESD79-3E Standard
- JEDEC 79-3F and JEDEC 79-3-1A.01 Standard
- JESD209-4A Standard
- JEDEC Standard No. 84-B51

10. Revision History

Last Modified	Revision	Description
December 2023	1	Initial release.
January 2023	2	Updated Table 30. RGMII/RMII Interface Group Multiplexing; A30, Mode 1. Added Synaptics documents to References section.
March 2024	A	Release to production.
April 2024	B	Minor update to add chip image to Overview section.
April 2024	C	Updated Table 35 min and max industrial for USB2_DVDD, VDD_CORE
September 2024	D	Minor update to fix typo in Figure 32 and Figure 33.
January 2025	E	Updated industrial parts description in Table 75. SL1620 Part Order Options and aligned to latest Synaptics template.
April 2025	F	Updated part number information in Table 75. SL1620 Part Order Options.
January 2026	G	Updated Figure 1. Astra SL1620 high-level block diagram to align with latest template/design guidelines.

Contact Us

Visit our website at www.synaptics.com to locate the Synaptics office nearest you.

PN: 505-001428-01 Rev G